AC POWER SUPPLY CIRCUITS FOR ENERGY HARVESTING

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ABSTRACT

Passive energy harvesting from mechanical vibration has wide application in wearable and embedded sensors to complement or replace batteries. Energy harvesting efficiency can be increased by eliminating AC/DC conversion. A test chip demonstrating self-timing, power-on-reset circuitry, and memory for energy harvesting AC voltages has been designed in 180 nm CMOS and tested. Circuit operation is confirmed for supply frequencies between 60 Hz and 1 kHz with power consumption below 130 μW.
Keywords: energy harvesting, self-timed, AC power supply, DRAM, power-on-reset.

INTRODUCTION

Energy harvesting from mechanical vibration is a promising alternative to slowly improving battery technology which can reduce embedded system weight and volume, increase operating lifetime, decrease maintenance costs, and open new frontiers for integrating digital computation with sensing and actuation in applications such as wireless sensor networks. Off-chip power electronics increase system cost and volume and limit the effectiveness of vibration-based energy harvesting due to losses incurred when converting from AC to DC voltage (typical efficiencies are between 18%-65% [1]). Interfacing digital circuits directly to the rectified AC energy harvester output avoids the power and cost of complex power electronics. Significant computation can be performed with the AC voltage because the supply frequency (60 Hz - 1 kHz) is orders of magnitude lower than the datapath frequency. This is in sharp contrast to previous work on RFID tags using a high frequency AC supply which also provides the clock [2].

Figure 1 shows the block diagram of a test chip developed to explore circuit design for energy harvesting AC power supplies. The chip combines a novel power-on-reset (POR) circuit, self-timed circuit design, and dynamic memory to implement an energy-scalable programmable FIR filter [3].

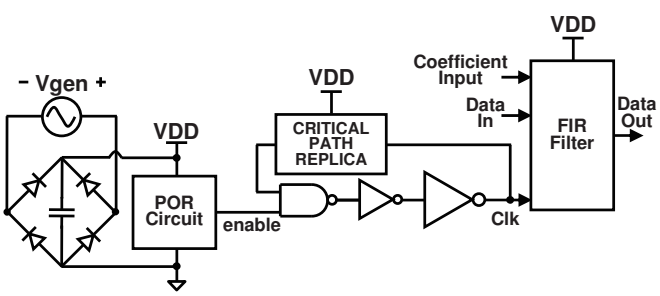


Fig. 1. Test chip block diagram.

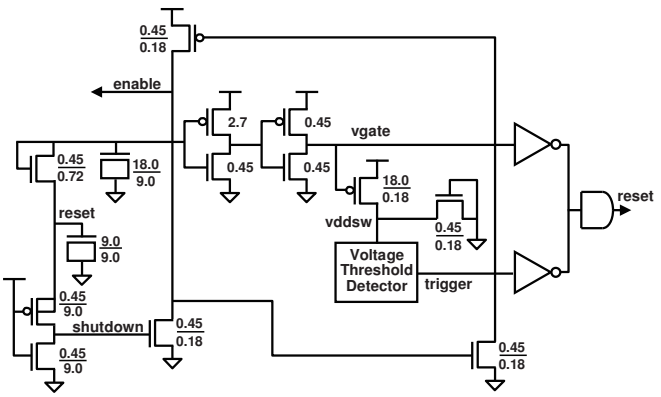


Fig. 2. Power-on-reset circuit.

It also integrates a static CMOS full-wave rectifier [4]. The rectifier filter capacitance due to parasitics and on-chip bypass is too small to smooth low frequency AC ripple to DC.

POWER-ON-RESET AND MEMORY DESIGN

For each energy harvesting power supply cycle, the load circuit must power on, perform computation, and turn off. Circuits must operate correctly over large supply voltage variations. Self-timed circuit design is robust to parameter variations, including supply voltage. Figure 1 shows the self-timed pipelined datapath in which the clock is provided by a ring oscillator tied to AC supply V_{DD} containing a replica of the critical path (a 16-bit ripple carry chain). The oscillator frequency varies with supply, temperature, and process automatically to ensure correct operation. A POR circuit initializes state at the beginning of every power supply cycle and sets an enable signal that controls when circuit operation starts. Between every power supply cycle, the supply voltage reaches a minimum and any state is potentially lost. A dynamic memory cell optimized to store data over short periods without a power supply enables continuous computation by preserving state between power supply cycles.

A POR circuit for AC supplies ideally turns on in deep subthreshold to maximize the fraction of the power supply cycle during which the load circuit is operating. To function correctly with a low turn-on voltage for vibrations between 60 Hz and 1 kHz, the POR circuit must generate a reset pulse independent of power supply frequency. POR circuits typically use an RC delay to partially control the turn-on voltage [5]. The circuit in Figure 2 relies on voltage threshold detection instead. V_{DD} and the POR **enable** voltages identify three different states. The initial state (V_{DD} off, POR circuit on) corresponds to the beginning of a power supply cycle. When

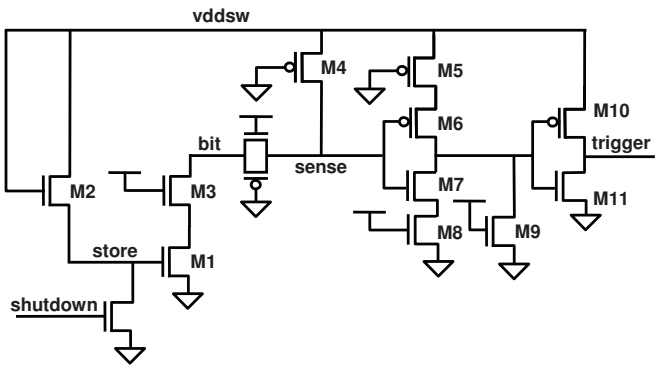


Fig. 3. 3T DRAM cell and sense circuit replica-based POR threshold detector.

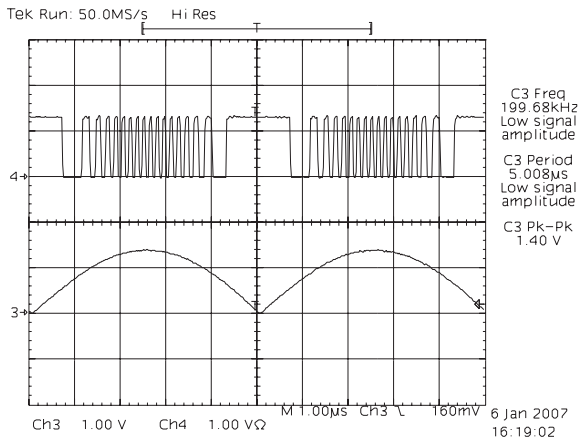


Fig. 4. AC supply and ring oscillator output.

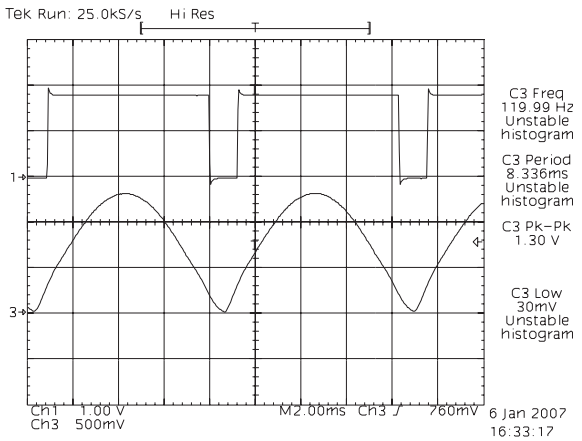
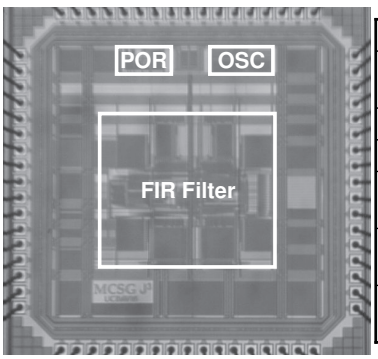


Fig. 5. Rectified waveform and POR output.



Technology	**180 nm CMOS**
Dimensions	**2.6 mm x 2.6 mm**
Transistors	**135K**
I/O V_{DD}	**1.8 V**
AC Supply (V_{PP} = 1.8 V)	**60 Hz – 1 kHz**
Core Freq. (max)	**75.6 MHz**
Power (Core)	**127 – 113 µW**

Fig. 6. Die photo and chip summary.

V_{DD} crosses the threshold, the circuit lowers **trigger** (V_{DD} is sufficiently high) and **reset** is asserted. After a delay, **enable** is asserted and the POR circuit turns off. This state represents the normal operating condition for the chip. A reset circuit asserts **shutdown** when V_{DD} goes low, causing **enable** to go low and reinitializing the POR circuit for the next cycle.

Memory cells for AC supplies must hold state while the supply is low without requiring frequent refreshes which can degrade system performance. A three-transistor DRAM cell with non-destructive read was used along with a single-ended sense circuit consisting of two transmission gates, a precharge transistor, and a tri-state buffer [1]. To ensure correct operation, the POR voltage threshold detection can be made dependent on the DRAM as shown in Figure 3. Transistors M1, M2, and M3 make up the replica memory cell while the other devices replicate the sense circuit. The gate of M1 and the source of M2 comprise the storage node capacitance. M1 has $W/L = 4.59\ \mu\text{m}/9.9\ \mu\text{m}$ while write transistor M2 is minimum sized to minimize leakage and maximize write voltage. The storage capacitance is approximately 300 fF and simulations indicate a valid voltage is held for at least 1.2 ms, the time required to operate with a rectified 60 Hz supply. Two 16×16 memory arrays on the test chip use this DRAM cell.

RESULTS

Figure 4 shows the measured ring oscillator output for a 100 kHz 1.4 V peak-to-peak AC supply from a signal generator (used for clarity). Figure 5 shows the measured fixed-threshold POR output [1] together with the on-chip rectifier output connected to V_{DD}. Figure 6 shows a die photo and summarizes chip parameters. Power consumption is measured for a 16-tap filter response using preprogrammed 16-bit coefficients. More power is consumed at lower supply frequency since the datapath is operating longer at higher V_{DD}. The self-timed datapath and POR circuit operate correctly using a DC supply, which enables a dual-supply system where energy can be harvested from multiple sources such as vibration (AC) or solar (DC).

ACKNOWLEDGMENTS

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