Integrated Solar Energy Harvesting and Storage

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ABSTRACT
To explore integrated solar energy harvesting as a power source for low power systems such as wireless sensor nodes, an array of energy scavenging photodiodes based on a passive-pixel architecture for imagers and have been fabricated together with storage capacitors implemented using on-chip interconnect in a 0.35 μm CMOS logic process. Integrated vertical plate capacitors enable dense energy storage without limiting optical efficiency. Measurements show 225 μW/mm^2 output power generated by a light intensity of 20k LUX.

Categories & Subject Descriptors
B.7 [Integrated Circuits]: General.

General Terms
Design, Experimentation, Measurement.

Keywords
Energy Harvesting, Low Power, Photodiode.

1. INTRODUCTION
Solar energy harvesting has been proposed to extend the lifetime of wireless sensor networks beyond limitations imposed by batteries [1]. To reduce system cost and volume it is desirable to integrate energy harvesting and storage with data processing circuits. Recent advances in very low power signal processing architectures for sensors [2] has created the opportunity to use CMOS photodiodes, similar to those used in digital cameras, for solar energy harvesting. Moreover, the increase in interconnect capacitance as CMOS processes scale provides an opportunity to store the harvested energy without requiring battery materials to be integrated. This paper describes a test chip incorporating an array of photodiodes and storage capacitors developed to explore the maximum energy per area that can be gathered from a solar source and stored in a standard CMOS process.

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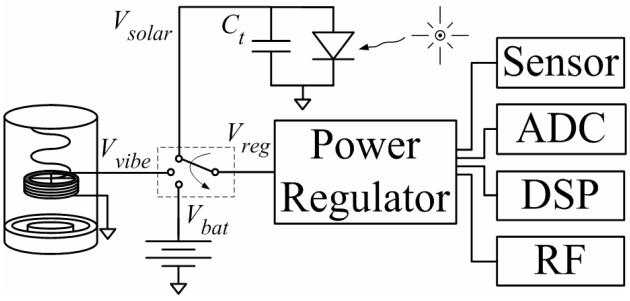

Figure 1: A low power wireless sensor node system powered from energy scavengers and a battery. Energy sources are labeled *Vsolar*, *Vvibe* and *Vbat* for the solar, mechanical vibration and battery, respectively. A mux switches between the unregulated energy sources.

2. ENERGY SCAVENGING PHOTODIODES
Figure 1 shows the block diagram of a typical wireless sensor node powered by light, mechanical vibration, and a battery. Light energy and vibrations are converted to electrical energy by photodiodes [1] and electromechanical transducers [2], respectively. The system's energy gathering ability will depend on environmental conditions which change over time and the scavenged energy needs to be regulated before being used. The sensor node consists of an analog-to-digital converter (ADC) that samples sensor data, a DSP core, and an RF transceiver. For low duty cycles, average power for this system (estimated from the literature [2,3,4]) can be under 5 μW.

The layout and design of an energy scavenging photodiode must balance several competing factors. The charge generated in the depletion region of the photodiode is stored in on-chip capacitors; therefore the physical layout of the diodes should facilitate both the solar energy harvesting and capacitive energy storage. Light reaching the photodiode depletion region must first pass through the passivation layers and around the storage capacitance, which is constructed on top of the diode to reduce area. Optical efficiency (OE), defined as the fraction of incident light onto the chip's surface which reaches the photodiode [5], is influenced by three loss factors: reflection losses, absorption losses, and critical angle losses. Once photons reach the photodiode, the quantum efficiency (QE) determines how many photons will generate electron-hole pairs. The product of OE and QE should be maximized by the geometry of the energy scavenging photodiode and storage capacitances to maximize output power.

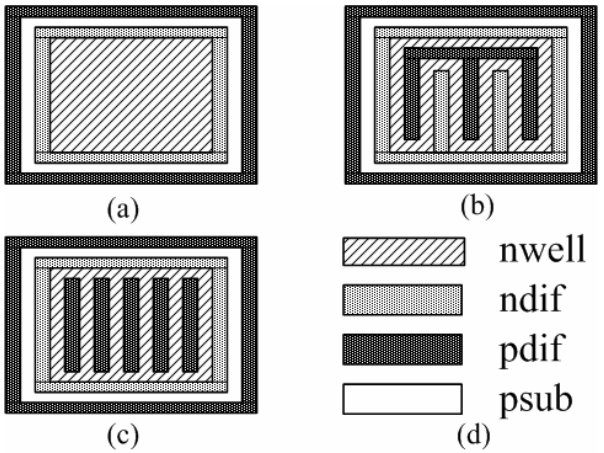

Figure 2: Top view of photodiodes. (a) D1, (b) D2, (c) D3, (d) Layer key.

To explore the photodiode design tradeoffs experimentally, three different geometries were fabricated and tested. The first design (D1) is shown in Figure 2(a) and is similar to a passive pixel structure used for a CMOS imager [6]. The p-substrate and n-well form the diode. The second design (D2) is shown in Figure 2(b). This structure uses fingers of p-diffusion inside the n-well in addition to the n-well to p-substrate junction to form more diodes connected in parallel with the well-substrate diode. The final design (D3) is shown in Figure 2(c). The D2 layout is similar to the D3 layout except every other p-diffusion finger is replaced with an n-diffusion.

A goal of this work is to determine the maximum energy per area that can be gathered from solar energy and stored in a standard CMOS logic process. To determine the energy we must first calculate the capacitance per area. The capacitance analysis will start with the energy relationship, which can then be divided up as the sum of two components: the metal capacitance and the junction capacitance. The total capacitance is given as

$$Ct = \frac{2 \cdot E_v}{\Delta V_{solar}^{\ 2}} = Cm + Cd \tag{1}$$

, where E_v is the energy stored in the capacitor, ΔV_{solar} is the voltage difference between the metal plates, and Ct is the total capacitance, which is made up of the metal capacitance Cm and the diode capacitance Cd.

When the mux in Figure 1 switches to the solar cell the total charge accumulated in the storage capacitance is shared with the capacitance at the input of the regulator. This charge sharing will yield a potential at the input of the regulator which is less then the initial stored potential before the switch. With ideal switching the voltage at the input of the regulator can be written as

$$V_{reg} = \frac{Ct}{Ct + Cr} V_{solar} \tag{2}$$

, where Cr is the input capacitance of the regulator present at the right of the rotating switch in Figure 1. It is seen here that to limit this attenuation factor the storage capacitance should be as large as possible. A capacitor structure that simultaneously enables a high OE and a high capacitance density is the vertical parallel plate structure shown in Figure 3, which passes light through the plates vertically. The fingers forming the n-well p-diffusion junctions of D2 and D3 can align with the vertical plates allowing for easy routing.

Capacitance simulations were carried out using Momentum [7] assuming four metal layers, a minimum vertical parallel plate separation of 0.6 μm, a silicon dioxide dielectric of thickness 0.64 μm, and an average metal thickness of 0.71 μm. D3 has less metal capacitance than the other two designs due to the need to connect the p-diffusion fingers together. For a diode area of 338 μm^2 in the given technology, the theoretical limit on the maximum obtainable capacitance (TL1) is close to 1pF while the semi-empirical upper bound (SEUB) is 0.616pF, determined as in [8]. D2 has a capacitance density close to 41% of SEUB (neglecting diffusion capacitance C_d).

The total pn junction capacitance is the sum of the capacitances from the diffusion-well diode, Dpdif-nw, and the substrate-well diode, Dpsub-nw. This capacitance can be modeled by a particular capacitance per unit area, Cj and a particular side wall capacitance per unit length, Cjw. These capacitances are in general nonlinear (voltage-dependent). The width of the depletion region will shrink with an increase in applied forward bias voltage across the junction. This decrease in depletion width will lead to an increase in the depletion capacitance, which can be modeled using a square root dependence on applied voltage. The pn junction capacitances can be written as

$$Cd = \frac{C_{do}}{\sqrt{1 - \frac{V_{Solar}}{\varphi_o}}} = \sum_{i=1}^{N} \left(C_{sw} P_i + C_j A_i \right) \tag{3}$$

, where φ_o is the built in potential of the junction, Ai is the area and Pi is the perimeter of the i^{th} diode. Table 1 summarizes the simulated capacitive characterization of the three diodes shown in Figure 2. The Cd given here is calculated with a junction voltage of 0.55 V, which is close to the open circuit voltage of the photodiodes under normal indoor lighting conditions.

Table 1: Capacitive Characterization (25°C, Area = 338μm^2).

	D1	D2	D3	TL1	SEUB
Cm (pF)	0.254	0.254	0.216	1.004	0.616
Cdo (pf)	0.070	0.178	0.285	–	–
Cd (pF)	0.113	0.286	0.460	–	–

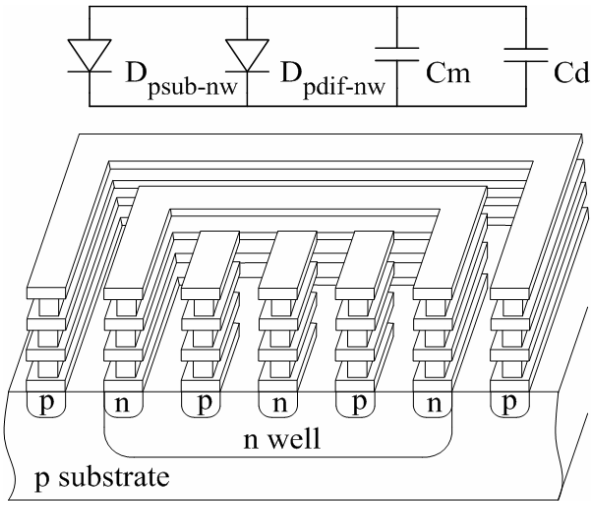

Figure 3: Side view cutaway of D2. Metal connected to p- and n- diffusions correspond to top and bottom capacitor plates, respectively.

3. EXPERIMENTAL RESULTS

Figure 4(a-c) shows the measured output power plotted versus light intensity and load resistance for the three photodiodes. The experimental light source was a typical tungsten filament incandescent bulb chosen to model indoor environmental conditions. At high light intensities, D3 generates more power per area than the other designs. However, D3 shows the highest sensitivity of output power to varying load resistance. For all three diodes, the optimal load resistance is a function of light intensity, with high intensity yielding lower optimal load resistance. D1 is least sensitive to light intensity and load resistance. No significant power loss was observed from the blocking of light by the storage capacitance.

To verify the operation of the photodiodes, a ring oscillator was constructed on-chip that uses the scavenged energy. Figure 5 shows a schematic of the prototype. It consists of a light source, integrated energy scavenging photodiodes, storage capacitance (Ct), a ring oscillator and buffers to drive the signal off chip. The nine stage ring oscillator employs current starving techniques with both pmos and nmos transistors to enable frequency tuning of the oscillator. A level shifting output buffer was used so that the oscillator's operation could be observed with little loading. Bias voltages V_p, V_n and the power for the output buffer was generated off-chip for testing purposes. In a single-well p-type substrate process, photodiodes working under forward bias drive the n-well below ground, potentially causing unwanted substrate currents to flow. Therefore, two test chips are required to demonstrate the oscillator. In a twin- or triple-well process this limitation can be eliminated. Figure 6 plots the ring oscillator frequency and the open circuit voltage (V_{OC}) versus light intensity. With one series diode, $V_{Solar} = 0.55$ V and the oscillator dissipates 67.3 pW (0.48 fJ per cycle) at a maximum frequency of 140 kHz.

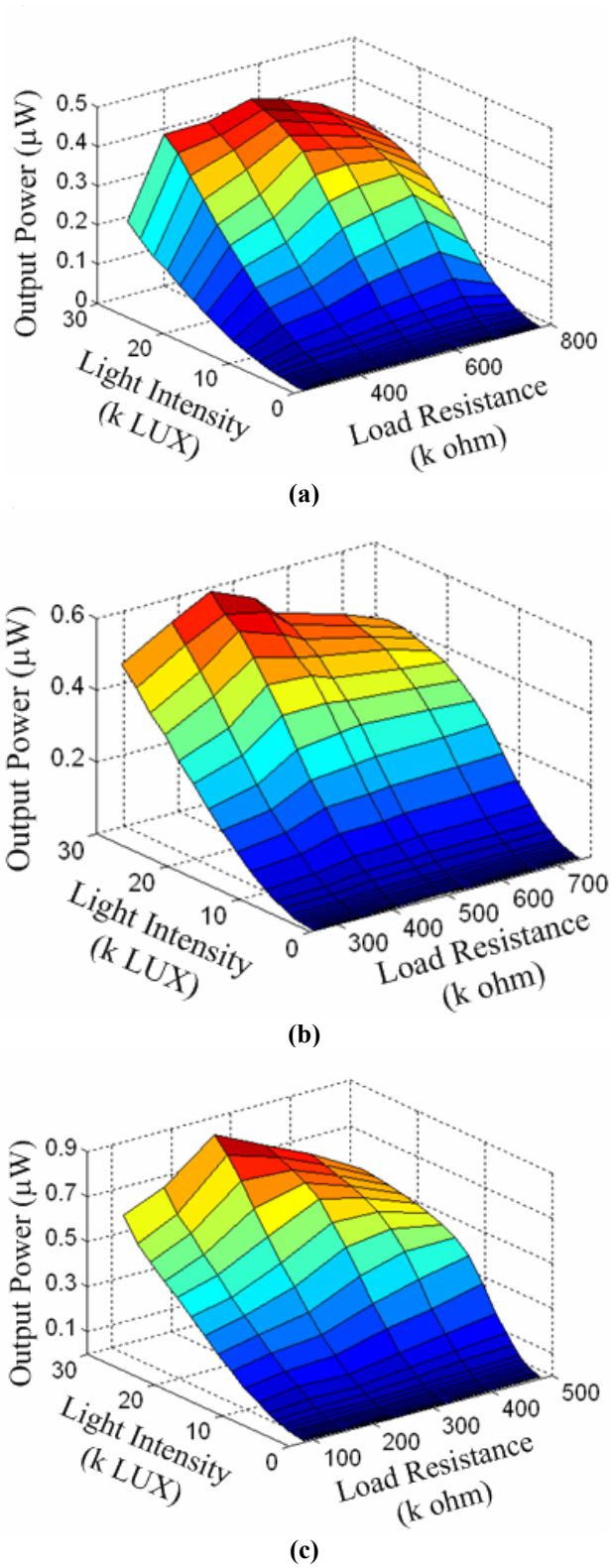

Figure 4: Output power vs. incident light intensity and load resistance, active area = 3000 µm^2, (a) D1, (b) D2, (c) D3.

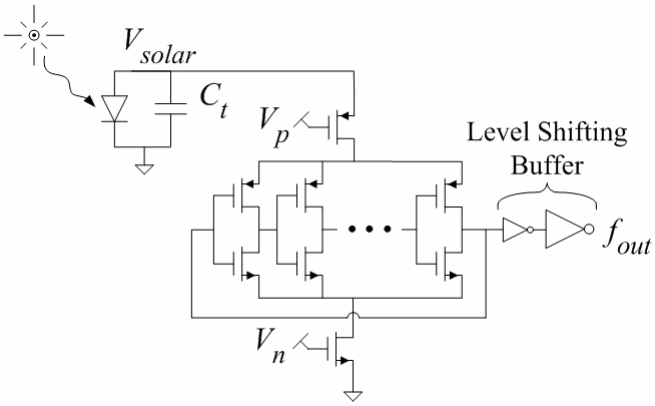

Figure 5: Test setup showing photodiode, current starved ring oscillator and level shifting output buffer.

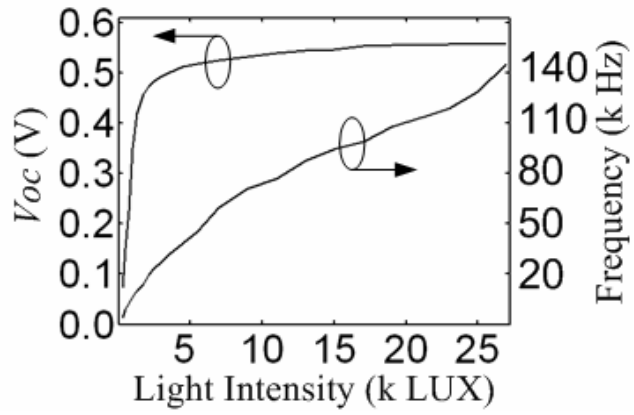

Figure 6: Measured plots of D3 showing V_{OC} and ring oscillator frequency.

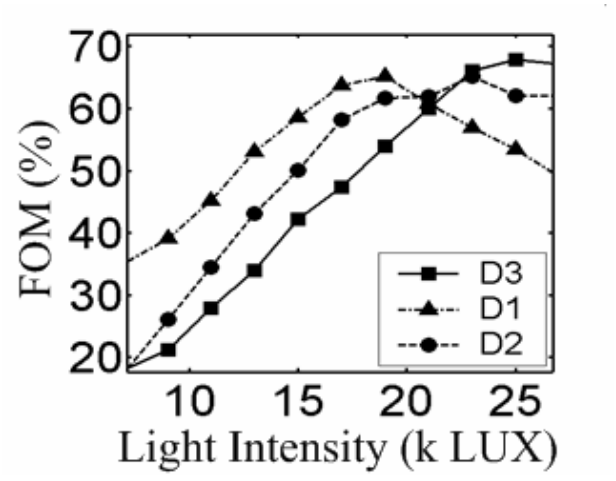

Figure 7: Measured figure of merit (FOM) plotted vs. input light intensity.

4. CONCLUSION

Figure 7 plots a figure-of-merit (FOM) for each photodiode which is defined as the maximum delivered power for a given level of illumination divided by the product of the open circuit voltage (V_{OC}) and the short circuit current (I_{SC}) [5]. Design D1 has the best FOM for low to moderate light intensities, but falls off significantly at high intensity. Design D3 has the largest FOM with high light conditions. For comparisons in terms of scaling each diode was laid out in three different sizes: 36 μm^2, 108 μm^2 and 338 μm^2. Larger photodiodes showed slightly better metrics which are largely attributed to lateral photocurrents [9,10]. In more advanced technologies the capacitance per unit area will increase as the minimum distance between plates shrinks. However, for the case where vertical parallel plate storage capacitors are constructed above the photodiodes this decrease in distance will negatively impact the OE due to a smaller aperture size. Figure 8 shows a die photograph of two D3 diodes connected in parallel. Table 2 summarizes the results with an incident light intensity of 20k LUX, similar to being outside on a sunny day. Based on these results, design D3 with area 150 μm x 150 μm can deliver 5 μW to power the system described above. D1 needs 184 μm x 184 μm and D2 needs 164 μm x 164 μm to deliver 5 μW. Without illumination, the system energy must be supplied by the integrated storage capacitors. For a 25 mm^2 total diode area consisting of 3 diodes in series with the metal storage capacitances for each diode connected in parallel, D1, D2, and D3 can supply enough energy for the DSP in [2] to produce 687, 745, and 903 output samples respectively. Future work will involve testing the photodiodes' response with incident light from a green laser (532 nm wavelength) to determine OE and QE as well as fabricating the diodes in polysilicon on top of the die to exploit more area for energy scavenging.

Table 2: Measured Performance (25°C, Area=338μm^2).

Parameters	D1	D2	D3
Power (nW)	50	63	76
Energy Stored (fJ)	26	35	31
FOM (%)	65	66	62
Capacitance, C_m (pF)	0.245	0.254	0.216
V_{OC} (mV)	465	525	533
I_{SC} (nA)	165	182	230

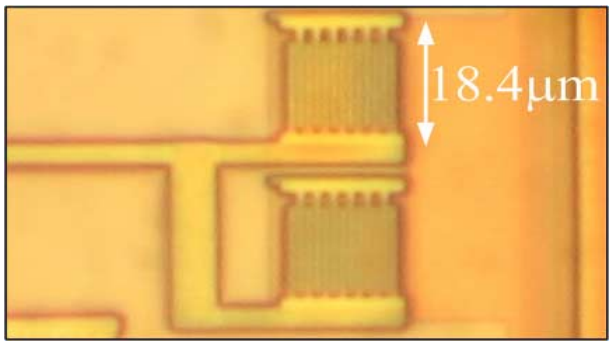

Figure 8: Die photograph of two D3 diodes connected in parallel.

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