Circuits for Energy Harvesting Sensor Signal Processing

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ABSTRACT

The recent explosion in capability of embedded and portable electronics has not been matched by battery technology. The slow growth of battery energy density has limited device lifetime and added weight and volume. Passive energy harvesting from solar radiation, thermal sources, or mechanical vibration has potentially wide application in wearable and embedded sensors to complement batteries. The amount of energy from harvesting is typically small and highly variable, requiring circuits and architectures which are low power and can scale their power consumption with user requirements and available energy. We describe several circuit techniques for achieving these goals in signal processing applications for wireless sensor network nodes such as using Distributed Arithmetic to implement energy scalable signal processing algorithms. In addition, we propose increasing vibration energy harvesting efficiency by eliminating AC/DC conversion electronics, and have investigated self-timed circuits, power-on-reset circuitry, and memory for energy harvesting AC power supplies. These techniques can also be applied to energy harvesting from other sources. A chip will be fabricated to test the proposed circuits.

Categories and Subject Descriptors: B.7 Hardware: Integrated Circuits

General Terms: Design

Keywords: energy harvesting, self-timed circuits, AC power supplies, dynamic memory, power-on-reset

1. INTRODUCTION

Over the past decade, the number and variety of embedded digital electronics has exploded, driven by applications such as cellular phones, portable multimedia devices, and sensor networks. Yet this dramatic increase in functionality and computing power has been accompanied by slowly improving battery technology. Energy harvesting from environmental sources is a promising alternative which can reduce system weight and volume, increase operating lifetime, decrease maintenance costs, and open new frontiers for integrating digital computation with sensing and actuation.

Because wireless communication typically consumes much more power than computation, many applications want to maximize the amount of computation done at a particular sensor network node [1]. Much current work is focused on maximizing power generation by developing and optimizing transducers for energy harvesting. However, the desire for smaller devices (< 1 cm^3) and higher levels of integration fundamentally limit output power. The work presented here addresses these issues from the power consumption standpoint by describing circuit techniques which are suitable for energy harvesting sensors. We focus on signal processing applications to drive microarchitecture and circuit design. Section 2 describes some energy harvesting alternatives and the system design issues they present. Section 3 describes modeling a vibration-based energy harvester for circuit simulation. An energy scalable signal processing microarchitecture and circuit alternatives for implementing it are presented in Section 4. Since off-chip power electronics increase system cost and volume and limit energy harvesting operation due to losses in the conversion from AC to DC voltage, Sections 5 and 6 describe datapath and memory circuits, respectively, which can tolerate rapid variation in supply voltage and can be used to eliminate AC/DC conversion [2]. Finally, Section 7 presents conclusions and opportunities for future work.

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2. ENERGY HARVESTERS

One of the major issues for circuit design in an energy harvesting system is dealing with the variability of the available energy, which can occur whether the energy source is solar, thermal, or mechanical vibration.

2.1 Solar and Thermal

Solar energy, converted to electricity by photovoltaic cells, has been used to power electronic systems for decades. Light intensity varies dramatically due to the 24 hour solar cycle and cloud cover for an outdoor sensor network. Recent work has shown that a distributed framework for the network to learn the available energy and adapt local routing algorithms using this knowledge can significantly extend system lifetime [3]. A similar framework can be applied to reconfigure analog and digital circuits once a model of energy availability is developed. Temperature differences converted to electricity by thermocouples have also been proposed to

power wearable electronics [4]. The power available from this source would vary as a person walked from an indoor, heated environment to a cold winter day outdoors.

2.2 Mechanical Vibration

Mechanical vibration is a complementary energy source to solar and thermal sources. Vibrations are present in active machinery such as ship turbines and building infrastructure such as heating ducts. Since they do not require light, sensors powered from mechanical vibration can be buried or used indoors where the light intensity is orders of magnitude lower than outdoors [5]. The available output energy can vary dramatically with vibration amplitude or even at the vibration frequency, depending on the power electronics used to convert the harvester output voltage. For these reasons, we focused on the vibration energy harvester context to explore our circuit concepts.

There are three main types of vibration-based energy harvesters. Electromagnetic converters generate a voltage by moving a coil relative to a fixed magnetic field [6]. Electrostatic converters place charge onto a variable capacitor and allow the vibrations to move the capacitor plates apart, reducing the capacitance. Capacitance and charge are related as $Q = CV$, so if Q is fixed and C decreases, V must increase [7] [8]. Piezoelectric generators use a piezo beam mounted as a cantilever with a mass on the unsupported end. Electrodes are plated on surfaces of the beam and sometimes between layers of the piezo material. As the beam flexes, a potential difference is created between the electrodes [9].

Several recent papers describe the theoretical and measured power output from various vibration-based energy scavenging devices, summarized in Figure 1 [7] [8] [6] [10]. Measured values from average amplitude vibrations indicate power on the order of 100 μW can be expected. The vibrations are expected to have frequencies between 60 Hz and 1 kHz and amplitudes between 2.5 μm and 5 μm.

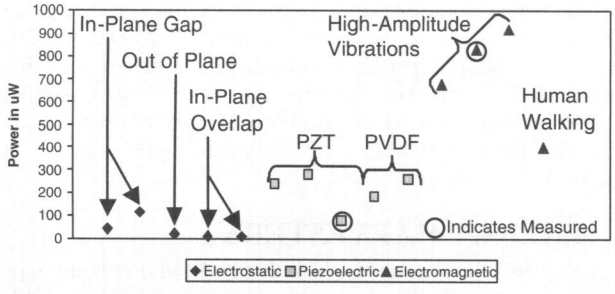
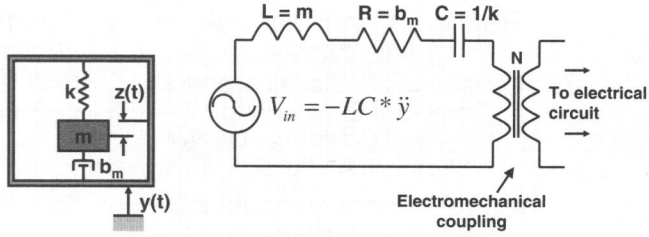


Figure 1: Harvester output powers.

3. ENERGY HARVESTER MODELING

Current EDA tools do not support direct integration of the electromechanical dynamics of vibration-based energy harvesters into circuit simulations. Whether we will use the harvester output directly or buffer it through an AC/DC converter, we want to accurately represent all significant aspects of energy harvesting in our circuit designs. We are developing a parameterizable equivalent circuit model for vibration-based energy harvesting that can be easily incorporated into standard circuit simulators such as Spice. We hope to use this model to drive circuit design and energy harvester development in a co-design cycle, so that specific circuit, mechanical, and electrical parameters can be evaluated for particular vibration sources to maximize power delivery.



(a) (b)

Figure 2: (a) General energy harvester mechanical model. (b) Equivalent circuit model with electromechanical coupling.

Vibration-based energy harvesters consist of a mechanical element that moves in response to external vibrations and a coupling mechanism that converts mechanical movement into electrical energy. Though the coupling elements vary by converter type, the mechanical response can be modeled as a damped driven oscillator (Figure 2(a)) with behavior described as $m\ddot{z}+b_m\dot{z}+kz = -m\ddot{y}$, where z and y represent position of the harvester mass and base, respectively, b_m is the mechanical damping coefficient, k is the spring constant, and m is the mass. The electrical load circuit is generally modeled as a damping term in parallel with the mechanical damping [8].

To model the mechanical elements, a series RLC circuit is used and is shown in Figure 2(b). The system equation for the damped driven oscillator matches the system equation for the RLC circuit if L is equal to the mass m, R is equal to the mechanical damping coefficient B_m, C is equal to the inverse of the spring constant k, and the magnitude of the acceleration is multiplied by LC and used as voltage source V_{in} [11]. The mechanical to electrical coupling differs among harvester types, though in general, the electrical system can be thought of as additional, variable damping to the mechanical system. One method of coupling for simulation is to connect the electrical system into the electrical model for the mechanical system through a transformer as shown in Figure 2(b).

Several types of transducers have been studied to look for potential power sources. The three main types of transducers are piezoelectric, electrostatic, and electromagnetic Several characteristics can be used to evaluate the potential usefulness of the different types of transducers. The range of output voltages is one concern. Electromagnetic transducers may produce too small of an output voltage (< 0.2 volts) when constrained to small volumes. Piezoelectric generators may produce too large of an output voltage depending on their construction and thus may require overvoltage protection circuits. Electrostatic transducers may also produce large output voltages. Depending on their operation, electrostatic transducers need one or two additional voltage sources. They also need a control system to switch the transducer in and out of the electrical circuit. Both the piezo-

electric and the electromagnetic generators do not require additional sources or control electronics. The final concern is the ease of fabricating the transducer and integrating it into the electronic system. Electrostatic transducers can be fabricated in a MEMS process and can potentially be integrated on chip. Electromagnetic transducers can be built on a macro scale but on a micro scale the magnetic materials needed are difficult to integrate. Piezoelectric transducers can also be built on a macro scale but are challenging to fabricate on the micro scale because of the difficulty of integrating piezoelectric material. As yet, there is no definitive answer on which type of transducer is superior to the other types. However, the equivalent circuit model abstracts these details and can be used to aid design of power electronics and digital logic for energy harvesting applications.

4. LOW POWER DSP USING DISTRIBUTED ARITHMETIC

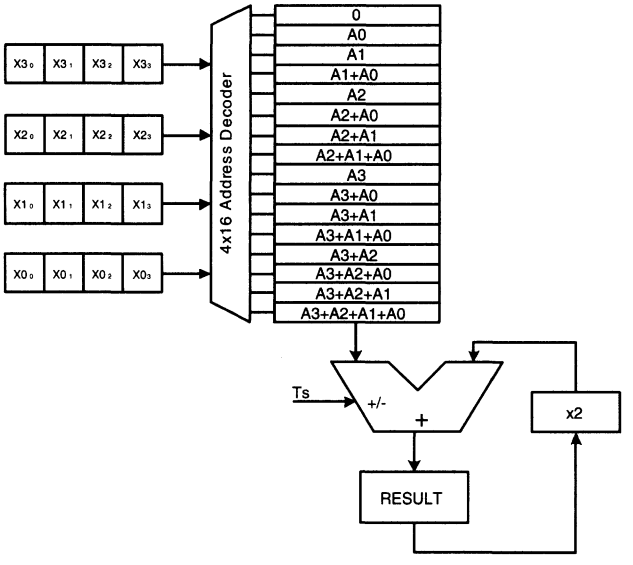


Figure 3: DA unit with register based shift memory.

Since the output power of energy harvesting is highly variable, it is important to incorporate *energy scalability* into a sensor signal processing architecture so that the power consumed by the system can be adapted to the available energy or user demands. One elegant approach to implementing energy scalability is to use serial computation. Since the throughput requirements for sensor signal processing are typically very low, the increased latency and/or dynamic power of serial circuits is compensated by their reduced area and leakage power. Energy can be directly traded off for output quality by varying the number of input bits shifted during the computation [6]. Distributed Arithmetic (DA) is a bit-serial and word-parallel technique for computing vector dot products by replacing multipliers with lookup tables (LUTs). Figure 3 shows an implementation of a DA four-tap FIR filter operating on 4-bit input data. All linear combinations of the filter coefficients A0 through A3 are stored in the LUT. As the bits of the input words are shifted to the right, successive bit slices $X0_i$-$X3_i$ through the vector of input samples address the LUT, and the LUT contents are read out and accumulated. Once all the bits have been shifted, the final FIR filter result is stored in the accumulator. Decreasing the number of bits shifted decreases the accuracy of the final result and reduces power consumption linearly with the number of bits. Thus, energy scalability is implemented with very little circuit overhead.

4.1 Subthreshold Circuit Design

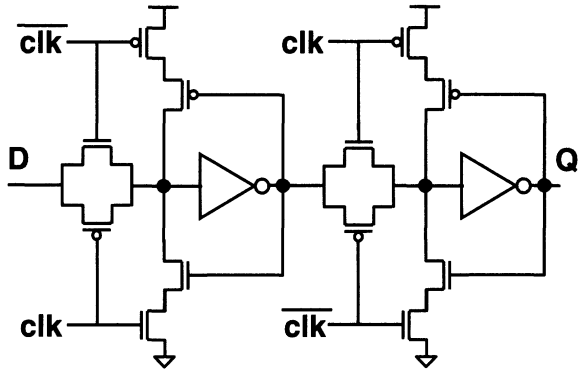


Figure 4: Static positive edge-triggered flip-flop.

Aggressive voltage scaling can be used to implement a serial computation structure such as DA to further reduce circuit power consumption. Operating transistors in the subthreshold regime is possible for energy harvesting sensors since sensor throughput requirements are low and applications can typically tolerate long circuit latencies [12]. Previous work has shown that existing static CMOS standard cell libraries can function well in subthreshold [13]. However, in deep submicron technologies care must be taken to ensure a sufficient ratio of on current to off current (I_{on}/I_{off}) to maintain adequate voltage levels on logic outputs or internal state nodes [12]. For example, Figure 4 shows a flip-flop which could be used to implement the input shift memory for the DA implementation in Figure 3. The feedback C^2MOS latch in the master stage must be sized wide enough to compensate for any current supplied by parallel leakage paths due to circuits driving input D. Otherwise, the master stage storage node could settle at an intermediate voltage and cause a logic failure.

4.2 SRAM Shift Memory

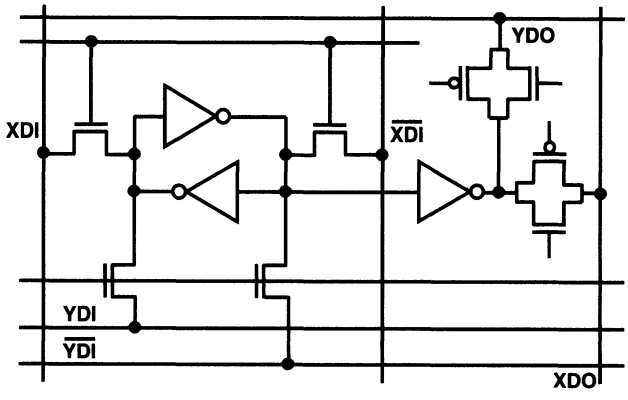


Figure 5: SRAM-based multiported register file circuit for DA shift memory.

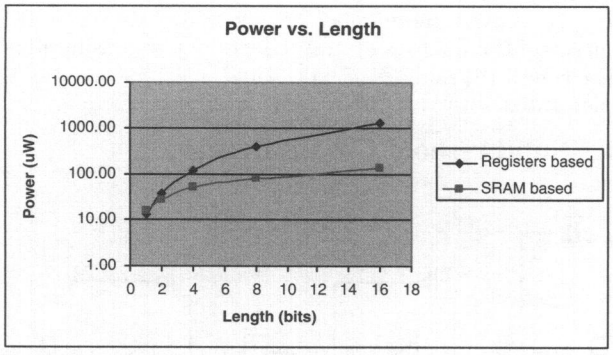


Figure 6: SRAM based and register based shift memory power versus data bit width.

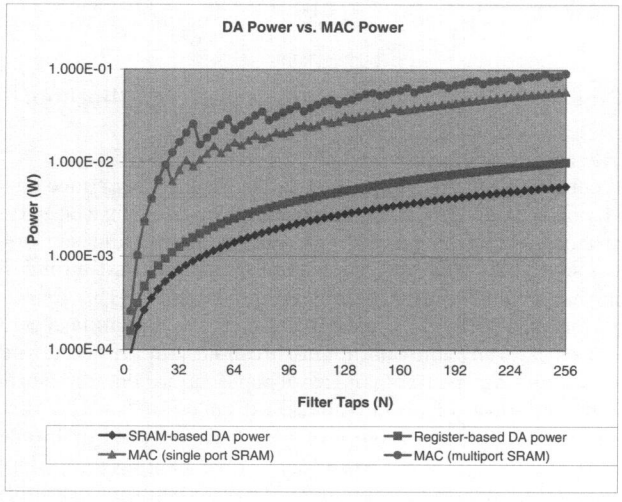


Figure 7: Distributed Arithmetic power vs. MAC power scaling with filter length for fixed area, supply voltage, and throughput.

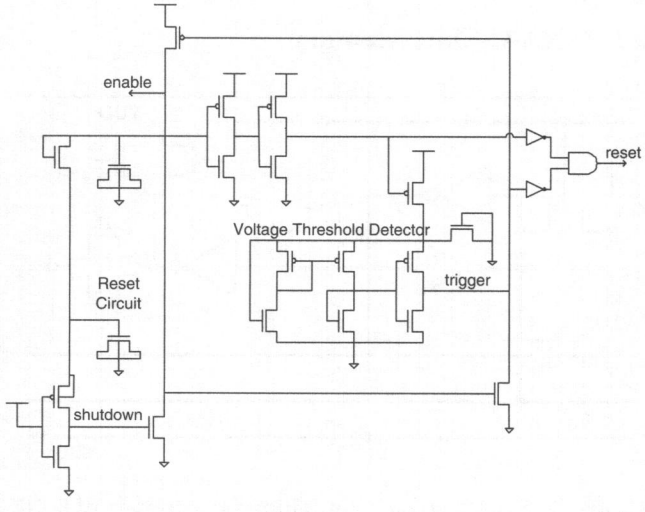


Figure 8: Power-on-reset circuit.

	Avg.	Max.	Min.
Turn-on voltage	0.45 V	0.61 V	0.30 V
Average power	4.1 nW	40.9 nW	0.1 nW
Peak power	500 nW	4.32 μW	7.5 nW

Table 1: Power-on-reset simulated performance.

An alternative implementation of the DA input shift memory uses a multiported SRAM. A single memory element is shown in Figure 5, where a 6T SRAM cell can be written through two differential ports, XDI and YDI, and read through two single-ended ports XDO and YDO. The bitlines for the X and Y ports route orthogonally, to allow parallel loading along the X direction and shifting of multiple parallel bit streams in the Y direction. The YDO port addresses the LUT. The area of a 4x16 array of flip-flops and multiported memories is about the same, however the flip-flop array lacks the ability to perform parallel loads. Figure 6 shows the SRAM-based solution is 3-10 times lower power than the flip-flop implementation for all interesting bit widths. Figure 7 shows power scaling with filter length for an array of DA units compared to multiply-accumulate (MAC) units implemented in the same area and with the same throughput constraint. Both DA implementations have lower power than MAC units using single or multiport data RAMs. Moreover, the DA approach has the ability to achieve energy scalability that the MAC implementation does not possess without additional hardware.

5. AC SUPPLY DATAPATH CIRCUITS

In addition to aggressive voltage scaling and subthreshold circuit operation, by interfacing digital circuits directly to the AC output of a vibration-based energy harvester, the power dissipation and cost of complex power electronics can be avoided. Significant digital computation can still be completed with the AC power supply because the supply frequency is several orders of magnitude lower than the integrated circuit operation frequency. For each power supply cycle, the chip must turn on, perform computation, and turn off. To guarantee correct operation, an accurate power-on-reset circuit is needed to properly initialize the chip at the beginning of every power supply cycle. The power-on-reset circuit should also set an enable signal that controls when circuit operation starts. After a reset pulse occurs, the circuits must operate correctly over large variation in the supply voltage. Self-timed circuits are used since they are robust to variations in supply voltage [14].

5.1 Power-On-Reset Circuit

A power-on-reset circuit for AC supplies ideally has a turn-on voltage in the deep subthreshold region. This maximizes the fraction of the power supply cycle during which the circuit is operating while minimizing power dissipation. In order to function correctly with a low turn-on voltage over the target range of frequencies, the power-on-reset circuit must generate a reset pulse independent of power supply frequency. Conventional power-on-reset circuits typically use an RC charging delay to at least partially control the turn-on voltage [15]. To design a power-on-reset circuit suitable for AC power supplies, a different approach was taken [2].

At a high level, the circuit functions as an analog finite state machine (FSM). State variables are analog signals (ca-

pacitor voltages) and state transitions are triggered by analog sense circuits. V_{DD} and a power-on-reset (POR) enable signal identify three different states. The circuit shown in Figure 8 implements a sequence of these three states. State 1 (V_{DD} off, POR on) corresponds to the beginning of a power supply cycle. The FSM waits in this state until the voltage threshold detector indicates that V_{DD} has risen above some threshold by lowering the trigger signal. When in state 2 (V_{DD} on, POR on), the power supply is considered on, therefore reset is asserted. Next, enable is asserted, the POR circuit turns off, and the FSM transitions into state 3 (V_{DD} on, POR off). This state represents the normal operating condition for the chip. A reset circuit asserts the shutdown signal when V_{DD} turns off, causing the enable signal to go low and reinitializing the POR circuit for the next power supply cycle. The power-on-reset circuit was simulated using a post-layout extracted netlist in Spectre. Table 1 summarizes the power-on-reset performance.

5.2 Ring Oscillator Self-Timed Circuit

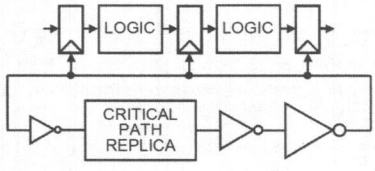


Figure 9: Self-timed datapath.

Figure 9 shows a self-timed pipelined datapath in which the clock is provided by a ring oscillator containing a replica of the critical path [14]. This design style is similar to traditional synchronous design in that the worst case performance of the longest pipe stage delay dictates frequency of operation. The ring oscillator frequency, however, varies with supply, temperature, and process automatically to ensure correct operation. Robustness to voltage and temperature was demonstrated in simulation using a self-timed clock for a distributed arithmetic unit with 16-bit ripple carry adders [6]. A replica of the adder critical path forms the ring oscillator. Performance of the self-timed datapath degrades as supply voltage is reduced, but the datapath still operates correctly. By using a circuit style which is compatible with subthreshold operation, a very wide range of supply voltages can be supported, although power dissipation may not be minimized at all voltages [13].

The self-timed datapath and power-on-reset circuit can also operate correctly under a DC supply voltage. In this case, the power-on-reset circuit will produce a reset pulse during the supply voltage rise time. The self-timed ring oscillator matches the clock frequency to the constant supply voltage and the chip operates as a traditional DC supply system. This provides for a dual-supply system where energy can be harvested from multiple energy sources.

6. AC SUPPLY MEMORIES

The combination of an AC power supply and a small power budget places strict limits on the types of memory that can be used for this system. Memory cells must be able to hold their values while the power supply is too low

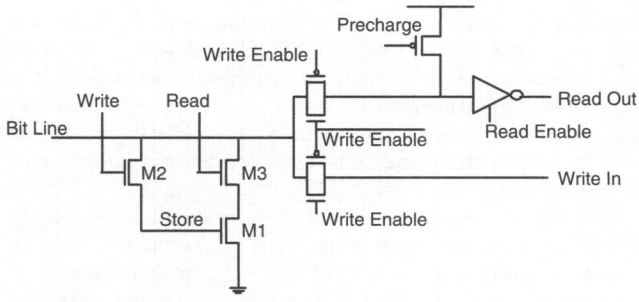


Figure 10: DRAM cell and sense circuit.

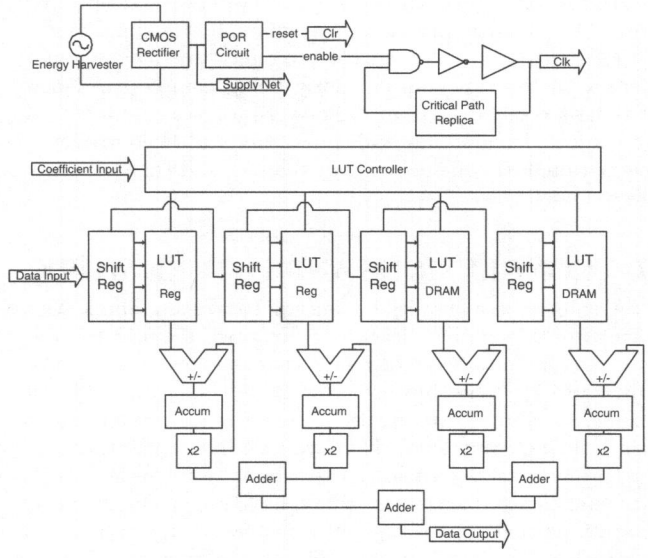


Figure 11: Test chip block diagram.

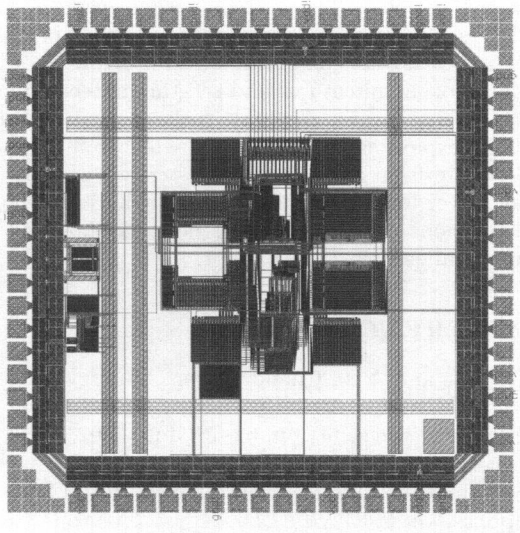


Figure 12: Test chip layout.

to operate without requiring frequent refreshing. Circuits requiring DC bias current must be eliminated. Due to these concerns, a three-transistor DRAM cell with non-destructive read was selected [16]. The sensing circuit for this cell is built from two transmission gates, a precharge transistor, and a tri-state buffer. The memory cell and its sensing circuit are shown in Figure 10 where transistors M1, M2, and M3 make up the memory cell [2].

The gate of transistor M1 and the source diffusion of transistor M2 comprise the storage node capacitance. Transistor M1 is sized to have a length of 9.9 μm and a width of 4.59 μm. Write transistor M2 is minimum sized. Simulations indicate that this configuration has the best ability to both minimize leakage and maximize the peak voltage written to the storage node. The storage node has approximately 300 fF of capacitance and is able to hold its state correctly for at least 1.2 ms, the time where the supply voltage is too low to operate for a rectified 60 Hz supply.

These memory cells were used to build two 16×16 memory arrays on the test chip currently being completed. On receiving a reset pulse from the power-on-reset circuit or a refresh pulse from an internal timer, the DRAM controller cycles through the memory array, reading and then re-writing each 16-cell row.

7. CONCLUSIONS AND FUTURE WORK

A chip to test circuits for energy harvesting applications using an AC supply voltage was designed in a 0.18 μm logic process. A simplified block diagram of the test chip is shown in Figure 11. The chip uses a scalable resolution FIR filter using Distributed Arithmetic as a test structure and is currently being completed. The layout is shown in Figure 12.

The circuits described above can be used with solar or thermal energy harvesters, which have much slower voltage variations than vibration-based devices. They can also be generalized to interface with inductively powered devices, a growing area with applications such as biomedical implants, embedded sensors, and RFID tags [17]. The proposed power-on-reset circuit was designed for low frequency power supplies but could be adapted for these higher frequency applications. The current design achieves correct operation in simulation up to a supply frequency of 250 kHz over all process corners and temperatures below 50 °C. The energy scalable architectures and self-timing techniques described above are fully compatible with subthreshold circuit design. By exploiting digital circuits which can operate on an AC supply from an energy harvester, we hope to open the door wider for future full mixed-signal, system-on-chip implementations of wireless sensor networks powered from environmental energy.

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