Invited Paper

Circuit Interfaces and Optimization for Resistive Nanosensors

Rajeevan Amirtharajah[a], Albert Chen[a], Darshan Thaker[b], and Frederic T. Chong[c]

[a]Dept. of Electrical and Computer Engineering, Univ. of California, Davis, One Shields Ave., Davis, CA, USA;
[b]Dept. of Computer Science, Univ. of California, Davis, One Shields Ave., Davis, CA, USA;
[c]Dept. of Computer Science, Engineering I, Univ. of California, Santa Barbara, Santa Barbara, CA, USA;

ABSTRACT

Carbon nanotube and semiconductor nanowires could potentially usher in a new era in chemical detection for environmental, biomedical, and security applications by providing highly sensitive detection at very low cost. For wireless sensor networks and implantable biomedical sensing devices, system power consumption is a critical factor in determining volume, operating lifetime, and circuit performance. We describe several key circuit challenges related to interfacing variable resistance nanosensors to digital integrated circuits through analog-to-digital data conversion. These challenges include drift in nanosensor baseline resistance due to fabrication variances and incomplete chemical desorption, various sensor and circuit noise sources, and integrated sensor and circuit area and power tradeoffs. We describe and evaluate the potential of several circuit techniques to address these issues, including self-test, self-calibration, and noise cancellation. Simulations indicate that ±40% variations in fabricated baseline resistance can be reduced to ±2% with a 25% increase in sensing area using a configurable sensor design. Based on these results, we explore potential A/D converter architectures for their use as low power nanosensor interfaces. Finally, we discuss resolution limits to miniaturization of nanosensor interface circuits.

Keywords: Circuits, nanosensor, bridge sensors, analog-to-digital conversion

1. INTRODUCTION

Detection of specific molecules is a critical operation in environmental monitoring, missions in space, control of chemical processes, and many medical and agricultural applications. We propose a sensor architecture that leverages nanoscale sensing elements and deep submicron CMOS transistors to produce inexpensive, long lifetime gas-sampling devices. At the core of our architecture is the principle of self-calibration. We design a system that adjusts for both fabrication variations and partially saturated sensors.

The high surface area-to-volume ratio of nanomaterials allows them to detect very low gas concentrations, enabling sensors with high sensitivity, but offering other advantages as well. Traditional gas sensors are either time or power intensive. As gases bond to a sensing medium, the sensor becomes saturated and loses its capability to detect small concentrations. These bonds are broken over an exponential amount of time or through the application of energy. Heat is used to aid the recovery time of traditional silicon sensors and heating the sensor element requires significant power. For example, one commercial sensor[1] consumes 850 mW, which severely limits the lifetime of an autonomous battery-operated wireless gas sensor node. Low power illumination with ultraviolet light has been shown to accelerate recovery for carbon nanotube sensors,[2] and could enable longer-lasting sensor operation from batteries. In this study, we focus on carbon nanotubes and silicon nanowires as sensing elements, introducing circuit and system techniques to overcome process variations in order to maintain sensor resolution and decrease system cost.

Figure 1 shows the self-calibrating design which forms the basic building block of our system. A four-element sensor configured as a bridge detects target gases. Its output signal is digitized by an analog-to-digital converter. The digital signal is sent to a microcontroller and a finite state machine, which implements the

Further author information: (Send correspondence to R.A.) R.A.: E-mail: ramirtha@ece.ucdavis.edu, Telephone: 1 530 754 6562

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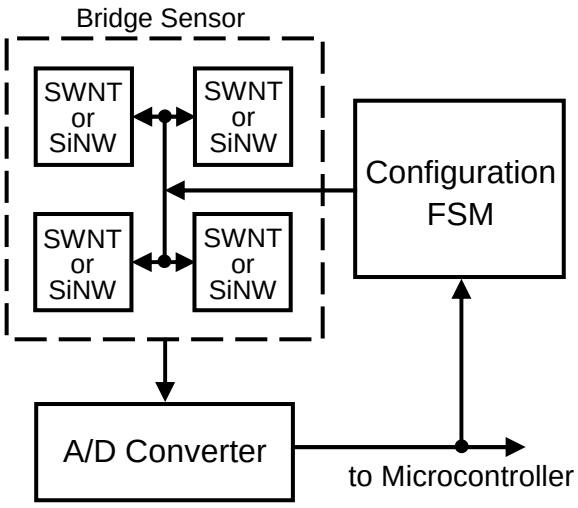


Figure 1. Self-calibrating sensor block diagram.

sensor configuration and calibration. This calibration capability allows us to maintain gas sensing accuracy in parts-per-billion (versus the 10 parts-per-million available from conventional sensors) in the face of large nanoscale fabrication variations. This same calibration capability allows us to dynamically redefine the baseline for minimum measurable gas concentrations as the sensor saturates. We use this moving baseline to iteratively adapt to environmental gas levels, detecting saturated readings, and enabling the potential application of energy to move the sensor array out of saturation. Furthermore, we exploit the low bandwidth requirements of gas sensing applications to develop interface circuits with very low power consumption. These circuits occupy modest area in deep submicron CMOS while still maintaining sensor resolution and thus help reduce system cost as well as power.

In the next section, we further describe the characteristics of both carbon nanotubes and silicon nanowires for gas sensing. This is followed, in Section 3, by a discussion of the critical issues in gas sensor element design and presents the self-calibrating building block for our architecture. Section 4 discusses the design of low power A/D converters targeting gas sensors and explores the circuit limits to gas detection for a minimal power interface circuit. We conclude with a discussion of open issues and future work and the impact of self-calibrating nanoscale arrays on broad areas of sensing.

2. SENSOR MATERIALS AND OPERATION

2.1. Carbon Nanotubes

Single dimensional, thin, hollow cylinders of carbon were first discovered in 1993 by groups at NEC and IBM. Single Walled Carbon Nanotubes (SWNTs), as they are called, have captured the imagination of researchers in physics, chemistry and the material sciences. SWNTs have many remarkable properties, of which the electrical properties are of interest to us. *Armchair* SWNTs display metallic properties while *zigzag* SWNTs tend to behave as semiconductors.

Electrical resistance of SWNTs has been demonstrated to change in the presence of small gas molecules like NO_2 and NH_3.[3] SWNTs are able to detect a small concentration of gas (< 10 ppm) at room temperature due to the large surface area to volume ratio inherent to nanoscale devices. More important for our work, researchers have built a simple gas sensor that consists of a network of SWNTs on an interdigitated electrode (IDE).[2] Such a configuration of SWNTs and IDE ensures that there is effective contact between the IDE fingers and the SWNTs while at the same time providing a large surface area over which gas molecules could be adsorbed. The advantages of such a manufacturing process are its simplicity, reproducibility and low cost. Figure 2 shows such an IDE (on the left) and a close-up of how the SWNTs fill the gaps between the fingers.

There are two limitations of the just-mentioned sensor that have to be addressed before such a device can be used in the field. The first limitation is that not all the SWNTs that are deposited on the IDE are semiconducting, some of them are metallic. This is because it is very difficult to obtain a sample that contains SWNTs of only one type. To overcome such discrepancies in the nature of the SWNTs, we think of them as manufacturing defects and then design an architecture that accounts for these defects. We propose a calibration technique that involves using redundancy to improve sensor accuracy. In short, we use more than one IDE sensor. The calibration of our sensor is described in detail in Section 3.3.

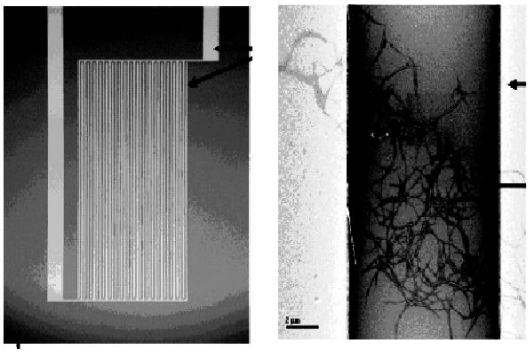


Figure 2. An IDE-SWNT sensor. The image on the left is one IDE. On the right is a magnified view of one IDE finger showing SWNTs in the gap between fingers. From Li.[2]

2.2. Silicon Nanowires

Semiconductor nanowires have also shown similar promise as molecular sensing devices. Lieber et al.[4] have shown chemical and biological sensing using individual CVD-grown Si nanowires, detecting simple metal ions and proteins. A Si nanowire ChemFET was also reported to be highly sensitive to prostate-specific antigens.[5] Techniques to create nanowire arrays that are coated with biomolecular probes for detection of proteins have also been proposed.[6] Outside of Si nanowires, there are also other nanostructures made of semiconducting metal-oxide materials capable of gas sensing[7],[8] most notably ZnO and In_2O_3. More recently, new techniques in fabricating semiconductor nanowires have shown improved process control. Utilizing a CVD process, Si nanowires can be grown between two vertical Si sidewalls,[9] creating mechanically robust nano-bridges (Figure 3). Another technique grows the Si nanowires vertically, producing nano-colonnades and making epitaxial connection to electrodes (Figure 4(a)).[10]

Both techniques have allowed greater process control in the fabrication of nanodevices, reducing the variability between devices and enabling design for mass production. Preliminary studies done at the Integrated NanoDevices and Systems Research Group in UC Davis have shown linear resistance from such fabricated devices, exhibiting less than 5% standard deviation in device length. However, standard variation of resistivity from device to device is still larger than 59%, indicating the need for calibration and statistical methods for improved control.

2.3. Sensor Modeling

A gas sensor depends on a chemical reaction which binds gas molecules to reaction sites in a solid sensing material, for example a mat of carbon nanotubes or individual silicon nanowires. A typical reaction with first order chemical kinetics is:[11]

$$S_c + NH_3(g) \overleftrightarrow{} NH_3(b) \tag{1}$$

where S_c denotes binding sites in the sensing material, NH_3(g) is ammonia gas, and NH_3(b) is ammonia bound to the sensing material. Suppose the forward reaction (adsorption of NH_3) has rate constant k_f and the backward reaction (desorption) has rate constant k_b. Then a differential equation for the concentration of bound ammonia is:

$$\frac{d[NH_3(b)]}{dt} = k_f[S_c][NH_3(g)] - k_b[NH_3(b)] \tag{2}$$

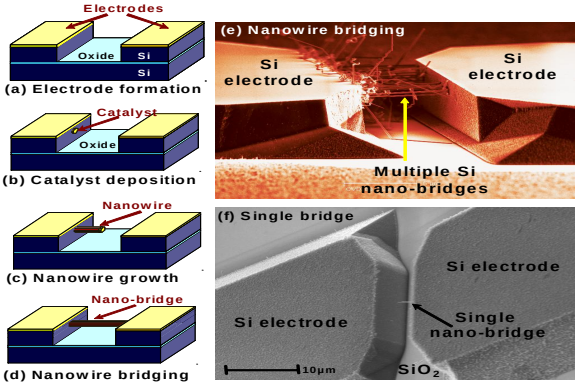


Figure 3. (a-d) Schematics of lateral nano-bridging technique and (e) SEM image of multiple and (f) single nano-bridging. Nanodevices are epitaxially grown between two vertical semiconductor electrodes. Courtesy M.S. Islam.[9]

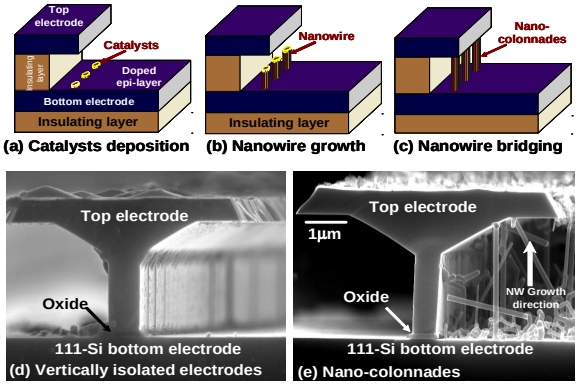


Figure 4. (a-c) Vertical synthesis mechanism of metal catalyzed nanowires between electrodes. (d-e) Demonstration of nano-colonnades between two vertical electrodes. Courtesy M.S. Islam.[10]

where the square brackets [ ] denote concentration. Similar equations can be derived for the concentrations of gaseous ammonia and binding sites. The conductance $G(c)$ as a function of gas concentration c observed in the gas sensor is given by the following equation:[12]

$$G(c) = G_0(1 + A_g c^{\beta}) \tag{3}$$

where A_g is the sensitivity of the sensor material and β is the response power, typically 1/2 for metal-oxide semiconductor gas sensors, and shown to be 1 for carbon nanotube mats.[2]

3. SENSOR CONFIGURATION AND CALIBRATION

Given the wide range of variations in material characteristics described above, an appropriate sensor element design and calibration strategy must be developed to enable accurate gas sensing.

3.1. Sensor Element Design

A limiting factor in utilizing SWNTs or silicon nanowires are the wide process variations. For accurate and repeatable gas detection, it is imperative that the response characteristics of the sensing element be deterministic. Unfortunately, the response characteristics are determined by the electrical, chemical and physical properties of the sensing element. Of key interest is the resistance variation. Resistance variations in bulk SWNTs have been reported as high as 40% of the mean resistance.[2] More recently, measurements on silicon nanowires have found resistivity ρ to have standard deviations of up to 59.7% of the mean ρ. For many applications, these large variations are unacceptable and severely limit the accuracy of the sensor. To statistically reduce the variation, two techniques are used. The first technique involves adjusting well-controlled dimensions in small increments in order to compensate for process variations. The second technique utilizes the law of large numbers, where the variation of the sensing element can be reduced by incorporating many nanodevices in parallel. The following sections will explore the design of sensing elements based on SWNTs and silicon nanowires.

3.1.1. Sense elements based on carbon nanotubes

Methods of producing SWNTs currently have little process control, with wide variations in the physical dimensions of the nanotube as well as the purity of the species present (i.e.. semi-conducting, metallic, carbon impurities). This causes $R_{element}$ to have widely varying values across processes and on-chip. The design begins with the interdigitated electrode (IDE) described previously as the sensing element.

By depositing a large number of SWNTs onto the IDE, the effective resistance of the IDE is primarily controlled by the gap spacing between the electrodes and the density of the SWNTs over the IDE area. Thus, the IDE utilizes the law of large numbers in its design, and the resistance variation of the sense element is now determined by a sample of SWNTs, instead of a single device. Further reduction of the variation can be achieved by incorporating adjustable finger lengths into the design of the IDE (Figure 5).

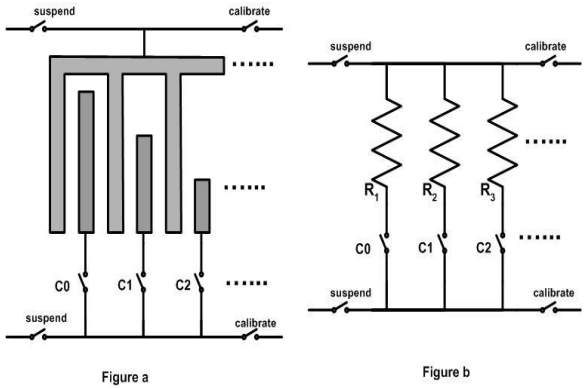


Figure 5. Figure (a) shows the design of the adjustable finger lengths. Figure (b) is the circuit representation.

Each finger length adds a certain area to the total interdigitated area, essentially adding a parallel resistor to the base resistor. The additional area added determines how much the overall resistance of the IDE decreases. A large area added corresponds to a large change in resistance. Similarly, a small area added corresponds to a small change in resistance. To optimize for low-power, minimization of the total area of the IDE as well as reducing the number of fingers is necessary to reduce capacitance and parasitics. However, to maintain the resistance of the sensing element within a specified range requires fine granularity. This constrains a lower bound in the reduction of area and number of fingers. To maintain a tighter range, each finger must have finer resolution, implying smaller increases in finger length and a greater number of finger lengths to choose from. The relationship is:

$$\frac{\rho}{L_d} = R(1 \pm \delta)$$

Where ρ is the resistivity and can vary with process, R is the desired resistance, δ is the desired tolerance of R, and L_d is the total finger length dimension. A feasible solution set of L_d values is thus constrained for any ρ allowed by the process, there is at least one value of L_d in the solution set such that $R = R_{desired} \pm \delta$. Typically, the solution set is found by defining the maximum and minimum required values of L_d that correspond to the extreme process corners and dividing the difference between $L_{d,max}$ and $L_{d,min}$ in a binary fashion until the constraint is met. However, this technique is suboptimal, and may produce more than one possible L_d solution for a given ρ.

An optimal solution can be obtained by recognizing that the maximum area (total finger length) required is determined by the highest resistivity and at the largest resistance tolerated. As resistivity ρ decreases due to process, the resistance will drop until $R(1 - \delta)$, at which point the area will need to be reduced. This is done iteratively until the minimum ρ is reached. A plot of optimized solutions versus acceptable tolerance is shown in Figure 6 and compared to the standard binary weighted solution. A target resistance of $R = 5.4$ kΩ was chosen, based on SNR analysis (Section 3.2). The optimized solution reduces the number of fingers by 53%.

3.1.2. Sense elements based on silicon nanowires

Similar to SWNTs, silicon nanowires exhibit resistance variations based on the physical dimensions of the device, as well as the doping concentration. However, one distinguishing feature from the carbon nanotube sensor described above is the ability to control the placement and growth of the nanowires. Our study will begin by assuming the sensing element consists of a single nanowire bridging two contacts. Later, it will be shown that having multiple nanowires in parallel can statistically reduce resistance variation even further.

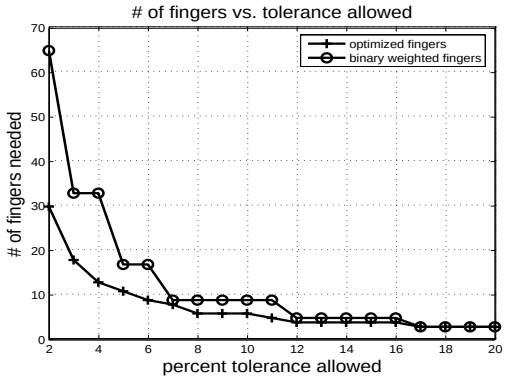


Figure 6. Plot of optimized and binary finger lengths as a function of δ

The relationship between the resistance and the physical parameters of the nanowire is:

$$\rho_{nw}\frac{L_{nw}}{\pi r_{nw}^2} = R_{nanowire}(1 \pm \delta)$$

Where ρ_{nw} is the resistivity, L_{nw} is the length of the nanowire, and r_{nw} is the radius. From measurements done by the Integrated NanoDevices and Systems Research Group at UC Davis, it has been shown that the standard deviation in the length is less than 5% of the mean, stemming from growth at a deflection from normal. Comparatively, the standard deviations of the radius and resistance are much higher, by a factor of 2 or more. This suggests that the variations in ρ_{nw} and r_{nw} dominate and determine the resistance variation. Thus the variation in length can be neglected. For the rest of this study, the length is assumed to be non-varying and well-controlled. Thus, the technique of adjusting the length to compensate for resistance variation can be applied with some modification. Since the length of nanowire is essentially fixed by the contact spacing, we propose fabricating replica sensing elements, each with a nanowire of different length. Selecting the appropriate element with the correct length thus becomes the method to compensate for process variation.

Finding the optimal set of L_{nw} is similar to the process described for carbon nanotubes. One difference is that there are now two factors, ρ_{nw} and r_{nw}, that must be considered. Each factor is considered separately to determine the sensitivity to the optimized solution set and to reduce complexity. By fixing the value of $r_{nw} = r_{nw,average}$, the variation of ρ_{nw} can be independently considered. The optimal solution set considering only the variation in ρ_{nw} is compared to the binary weighted solution in Figure 7(a). Similarly, fixing $\rho_{nw} = \rho_{nw,average}$, and the effects of r_{nw} variation on the solution set is shown in Figure 7(b). The target resistance was arbitrarily chosen to be $R_{nanowire} = 100k\Omega$.

In both cases, the optimized solution has reduced the number of required replica sensing elements by more than 60%, and is able to achieve a resistance tolerance of 3%. We can further reduce the number of required elements by taking advantage of the law of large numbers. Instead of a single nanowire as the sensing element, an element consisting of multiple parallel nanowires will have a variation less than the variation of a single nanowire.

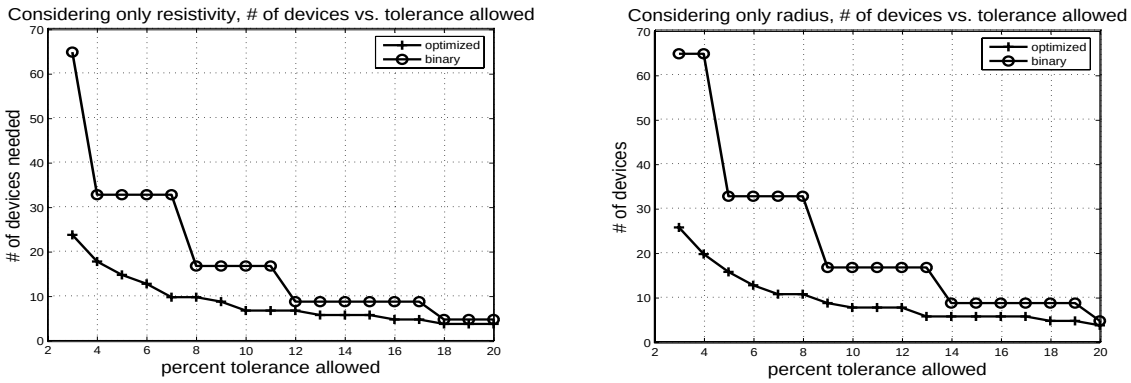
Taking the parallel resistor formula:

$$\frac{1}{R_{eq}} = \sum_{i=1}^{N}\frac{1}{R_i}$$

Differentiating both sides and assuming δR's are Gaussian with zero mean:

$$\frac{\delta R_{eq}}{R_{eq}^2} = \sum_{i=1}^{N}\frac{\delta R_i}{R_i^2} \Longrightarrow \delta R_{eq} = R_{eq}^2\sum_{i=1}^{N}\frac{\delta R_i}{R_i^2} \Longrightarrow \sigma_{eq}^2 = R_{eq}^4\sum_{i=1}^{N}\frac{\sigma_i^2}{R_i^4}$$

where R_i is the average value, R_{eq} is the equivalent resistance using the average R_i, and σ_i, σ_{eq} are the standard deviations, respectively. Since $R_i > R_{eq}$, the variation in the equivalent resistance becomes smaller as more resistors are added in parallel.



(a) (b)

Figure 7. Plot of optimized and binary device lengths as a function of δ, considering only (a) ρ_{nw} and (b)r_{nw}

3.2. Bridge Sensor Configuration

Circuit architectures focusing on gas sensing have traditionally emphasized obtaining the maximum accuracy allowed by the sensing material. Consideration of the power/area/accuracy trade-off has been minimal at best. In this section, a configurable, adaptable circuit architecture optimizing for both accuracy and low power is presented.

The basic design for the sensor is shown in Figure 8(a). Four $R_{element}$ resistors are configured into a Wheatstone bridge topology. This configuration is extremely sensitive to small changes in conductance and provides high accuracy for sensor applications. Each leg of the Wheatstone bridge is essentially a voltage divider created by two element resistors. As $R_{element,sense}$ is exposed to gas, its resistance will change, altering the voltage difference seen across the two legs. The other SWNT resistors are unexposed and unaffected. Assuming $\Delta R \ll R$, the voltage difference is related to the resistance change by the following:

$$\frac{\Delta R}{R} \approx 2\frac{V_{sense}}{V_{dd}}$$

Since the gas concentration is related to $\frac{\Delta R}{R}$, a simple voltage measurement across the two legs of the Wheatstone bridge is sufficient. An advantage of this design is that it requires no bias voltages or currents to provide a reference. Instead, the reference leg provides a relative comparison. This is desirable, as the circuit elements can be better matched, reducing offset errors and providing common-mode rejection.

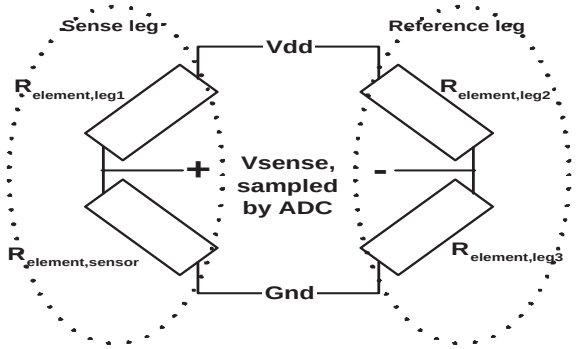


Figure 8. Wheatstone bridge topology used for sensing.

Choosing the value of the element resistors is a key design parameter. The value of the resistance is constrained by the noise characteristics of the device and the sensitivity required for small concentrations of gas. A large

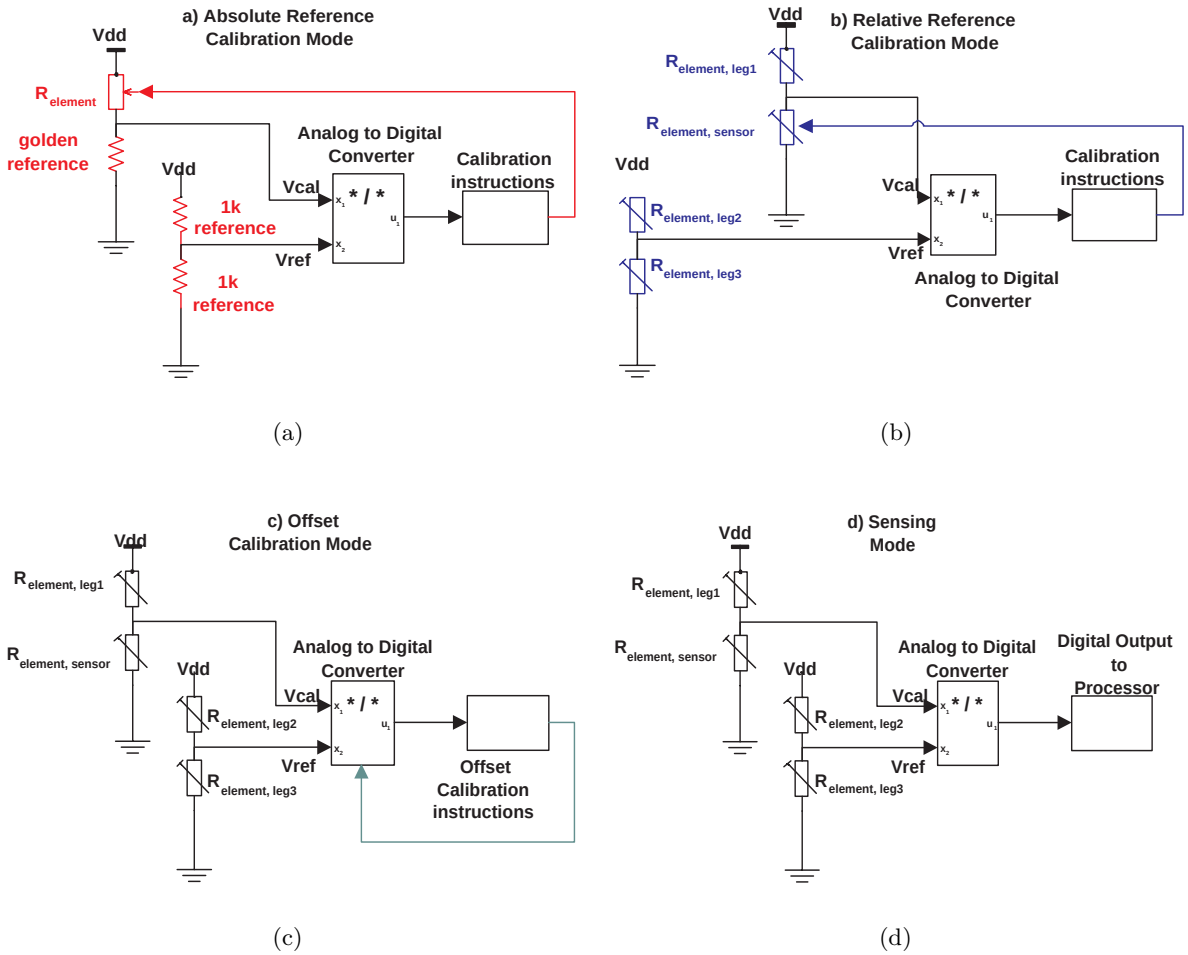


Figure 9. (a) Sensor configuration for Absolute Calibration. (b) Sensor configuration for Relative Calibration. (c) Sensor configuration for Offset Calibration. (d) Default sensor configuration

resistance value provides better sensitivity (i.e. larger change in resistance) to gas, but also increases the noise seen by the ADC. The noise of SWNT's is dominated by $\frac{1}{f}$ noise.[13] The sensitivity of the sensor is given by Equation 3. For accurate measurement, a Signal-to-Noise (SNR) ratio of 3dB is needed. Calculations performed using MATLAB translate this SNR requirement to a desired $R_{SWNT} \approx 5.4$ kΩ.[2]

3.3. Self-Calibration

Selection of the correct finger lengths is the role of calibration. However, the capabilities of calibration can also be extended to improve efficiency and accuracy. The functionality of the calibrator can be separated into three operating modes: absolute calibration, relative calibration, and offset calibration.

An absolute resistance with a deterministic gas response is needed for reproducibility and to reduce statistical sampling variation. For this purpose, a laser-trimmed "'golden"' resistance of the desired value is used to compare the resistance of the element resistor. Figure 9(a) shows the block diagram. This comparison is done by placing the element resistor and the golden resistor in a voltage divider configuration. The voltage is then compared to a reference voltage and the difference sampled by an analog-to-digital converter (ADC). The reference voltage is produced by on-chip poly resistors that are matched to each other and do not necessarily need to be at a specific resistance value; they simply produce a reference voltage equal to half the supply voltage. Once the difference is sampled by the ADC, a decision circuit adjusts the size of the element resistor such that the voltage difference is minimized. All four element resistors must be calibrated in this way.

Once the sensor is in operation, the element resistors may experience changes in resistance due to process drift or electrical stress. In this case, the calibrator is utilized to improve the common-mode rejection between the two legs of the Wheatstone bridge. In Figure 9(b), the ADC is sampling the voltage difference between the two legs of the Wheatstone bridge. This difference is then used to adjust $R_{element,sensor}$ to reflect the new baseline resistance. Only $R_{element,sensor}$ needs to be adjusted, as $R_{element,leg}$ has not been exposed to gas and provides a good indicator to process drift.

The calibration technique can also be used to improve accuracy dynamically. The absolute and relative calibration assumes that the sensor is idle and has sufficiently recovered to return to its static base state. However, during sensing operation, the sensor can gain further improvement by dynamically normalizing the base resistance and measuring the difference between future values and the new "'recalibrated"' base resistance. This is shown in Figure 9(c). In this topology, the ADC samples the difference between the sensing leg and the reference leg. This offset is stored and used to adjust the ADC so that all subsequent samples are compared to this common offset. In a sense, the ADC renormalizes itself and gains dynamic range. Another usage of offset calibration is to achieve finer resolution than what absolute or relative calibration allows. For example, after absolute or relative calibration, there may still be some small difference in the absolute and relative values of the element resistors. This difference directly limits the sensitivity of the ADC. Since this difference is DC common, the system can adjust and remove this DC offset, should further accuracy be desired. This is similar to filtering out the common-mode noise.

Determination of what type of calibration is needed can be shown in Figure 10. If the system is presently accurate enough, then no calibration is needed. If the system is not accurate enough by a user-defined setting, then the system examines how far off the current accuracy is compared to the desired accuracy. If the accuracy is off by more than 2 $\text{LSB}_{desired}$, then the system will initiate an absolute calibration. If the accuracy is off by less than 2 $\text{LSB}_{desired}$, then the system will initiate a relative calibration. After each stage of calibration, the system determines whether additional calibration is needed or not. The 2 $\text{LSB}_{desired}$ is determined by assuming the $R_{element,sensor}$ is off by more than 1%. This roughly translates to a mismatch offset voltage of 5 mV for a 1 V supply. This is roughly 1 LSB_{min} of an 8-bit ADC. To have the desired accuracy and reliablity, the ADC must be able to distinguish at least $\frac{1}{2}$ $\text{LSB}_{desired}$. The system validates its accuracy by measuring the difference between the sensing leg and the reference leg. If the difference is larger than $\frac{1}{2}$ $\text{LSB}_{desired}$, then additional calibration is required. If after going through absolute calibration, relative calibration and offset calibration the system still cannot resolve the accuracy setting, then the only option is to reset the accuracy setting or wait until conditions allow the desired accuracy.

4. CIRCUIT INTERFACE

The integration of nanotube and nanowire sensors with CMOS transistors offers further opportunities in intelligent sensor design beyond self-calibration and compensation for process variations described in preceding sections. We are exploring alternative topologies for analog-to-digital conversion that exploit the low bandwidth nature of gas sensor signals to decrease system power consumption and relax transistor matching requirements. Both issues are significant challenges as CMOS scales into the deep submicron region.

4.1. Voltage Mode A/D Converter

A highly accurate A/D converter (ADC) design is required to detect gas concentrations as low as 1 ppb. For example, spanning a dynamic range for concentration from 1 ppb to 10 ppm requires a 16 bit converter. Current design techniques have allowed ADCs to achieve precision as great as 24 bits of resolution. However, most of these techniques do not lend themselves easily to low power, low energy adaptations. Recently, an ADC design proposed by Scott, et. al.[14] has set the standard in terms of energy efficiency per bit. However, its maximum precision of 8 bits limits the lowest detectable gas concentration and provides insufficient resolution for postprocessing techniques such as digital filtering. We are exploring techniques to increase ADC resolution to 16 bits while minimizing energy consumption.

To minimize energy during system operation, the ADC must scale energy with accuracy, allowing the user to exploit the energy/accuracy tradeoff. This implies a variable precision design, while minimizing power at all precisions. Two approaches widely considered for low energy applications are successive approximation ADCs

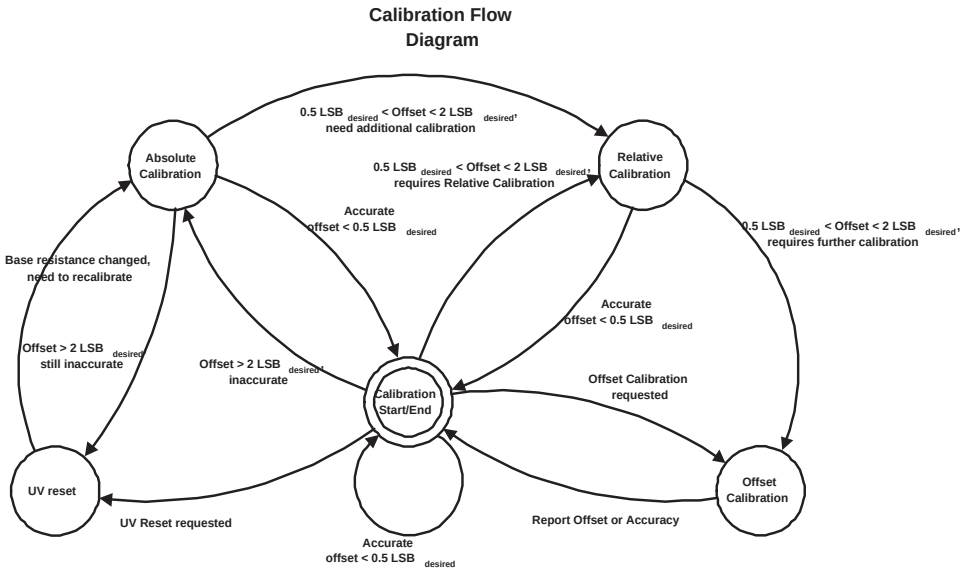


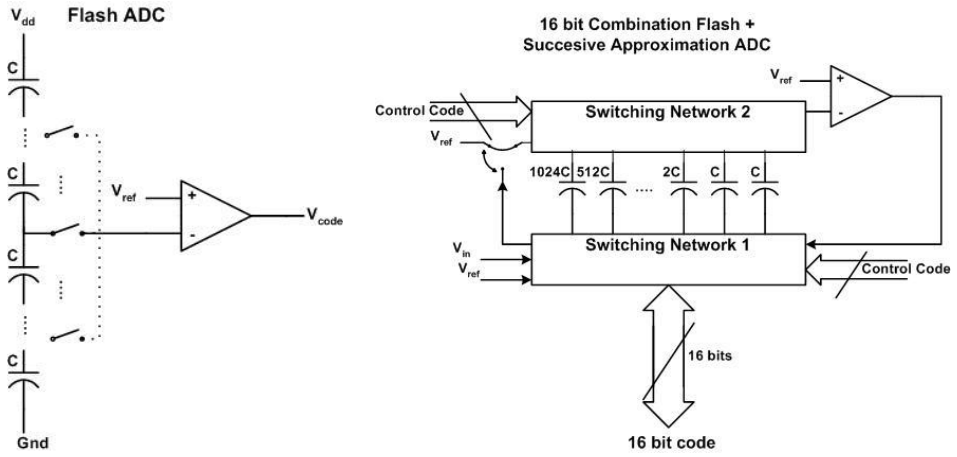
Figure 10. Calibration State Flow

and algorithmic ADCs. Both approaches scale precision with energy, however the successive approximation ADC allows initialization of the internal state. This allows the ADC to begin its search at an estimated value, thus reducing convergence time and energy consumption and makes successive approximation attractive for sensor applications.

Charge Redistribution ADC One implementation of successive approximation is to sample the input onto a capacitor array. The capacitors are disconnected from the input and a subset are connected to a reference voltage V_{ref}. There is no low impedance path for the capacitors to discharge, so the charge redistributes itself on the new equivalent capacitance. The resulting output voltage V_{out} is: $V_{in} - V_{ref} * \frac{C_{switch}}{C_{total}}$ where V_{in} is the input voltage, C_{switch} are the capacitors that are sourced to V_{ref} and C_{total} is the entire capacitor array. By sizing the capacitor array to be binary weighted and selecting C_{switch} so that $V_{output} = 0$, we can compute the input voltage as a binary code normalized to V_{ref}. The main drawback in successive approximation ADCs is the area required in the capacitor array. To make successive approximation ADCs high precision, large unit capacitors are needed to minimize noise (proportional to $\frac{kT}{C}$) and the effects of process variation. Each bit increase in precision requires a 2X increase in capacitor area, corresponding to an exponential increase in energy consumed. The energy consumed in charging the capacitor array in a 16-bit ADC is 256 times greater than for an 8-bit ADC.

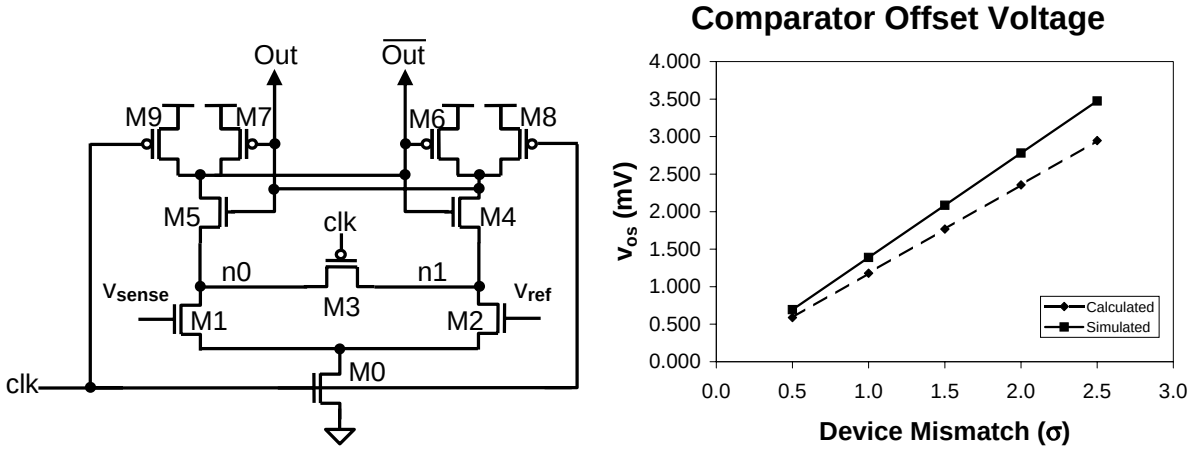
Flash + Charge Redistribution ADC To reduce energy, we are developing a flash ADC to compute the most significant bits (MSBs) of the ADC output. Typically, flash ADCs use resistor strings and are utilized for their speed, not low power. By replacing the resistor string with a capacitor string, we eliminate static power, and are only concerned with the dynamic charging of the capacitors and the power consumed by the comparator. By reusing the capacitor array from the successive approximation ADC, we can also minimize area. Calculations show that the optimal design for a 16 bit ADC which combines successive approximation and flash architectures uses the flash portion to compute the first 5 MSB bits and the remaining 11 bits are computed by successive approximation. Figure 11(a)-(b) shows the block diagram of the proposed design. The flash converter is implemented by a second switching network.

Logarithmic ADC Sensing a wide dynamic range of gas concentrations demands a large number of ADC output bits. An alternative is to use a logarithmic mapping ADC which converts a wide linear dynamic range



(a) (b)

Figure 11. (a) Flash ADC architecture. (b) Flash + capacitor array successive approximation ADC architecture.



(a) (b)

Figure 12. (a) Dynamic comparator circuit schematic. (b) Comparator voltage offset.

to a compressed logarithmic one. This approach has been used in log-sensitive signal processing applications such as artificial cochlea for the hearing-impaired.[15] For gas sensing, a logarithmic ADC reduces the resolution requirement to 10 bits, and may be suitable for some applications.

4.1.1. Dynamic Comparator

Power dissipation in comparator circuits can be a significant source of power consumption in A/D converters. This section examines a comparator design that dissipates only dynamic power and its potential application to low speed and medium resolution A/D converters for gas sensing.

The overall goal of the comparator design is to obtain medium voltage resolution at the lowest possible power. Since the target application is a low data rate (on the order of 1 kHz or less) A/D converter, the speed of the comparator is not an issue. Typical comparators for ADCs consist of a differential amplifier front end followed by a dynamic latch.[16,17] A fully dynamic design is desirable since the static power dissipation of an amplifier can dominate the power of the rest of the A/D system. However, the high gain of the analog front end provides very good resolution and speed, and it becomes a challenge to create a fully dynamic circuit with adequate performance.

Figure 12(a) shows a dynamic comparator. The circuit consists of a cross-coupled CMOS inverter pair (M4-M7), a matched differential input pair (M1 and M2), a set of precharge devices (M3 and M8-M9), and an evaluation device (M0). When the clock signal is low, PMOS transistors M8 and M9 are turned on and NMOS transistor M0 is cut off, thus pulling differential output nodes Out and $\overline{Out}$ high. This turns on devices M5 and M4 and precharges circuit nodes $n0$ and $n1$. Transistor M3 equalizes the voltages between the two nodes. During the evaluate phase, clock goes high and devices M8 and M9 are cut off while M0 turns on. The voltages at $n0$ and $n1$ start to decrease, and the rate at which they are discharged depends on the gate voltages V_{sense} and V_{ref}. Whichever node pulls down first engages the positive feedback in the cross-coupled inverters and pulls the outputs to a final value (for example, $Out = V_{dd}$ and $\overline{Out} = 0$ if $V_{sense} < V_{ref}$).

Mismatch between devices M1 and M2 limits the smallest voltage difference $V_{sense} - V_{ref}$ which can be reliably determined by the comparator.[18] Experimental data for a number of CMOS processes has shown that threshold voltage differences ΔV_T and current factor differences $\Delta\beta$, where $\beta = \mu C_{ox} W/L$ are the dominant sources of mismatch.[19] These random differences are generally considered to be independent normally distributed random variables with variances inversely dependent on the device area WL, such that $\sigma^2(\Delta V_T) = \frac{A_{VT}^2}{WL}$ and $\sigma^2(\Delta\beta/\beta) = \frac{A_\beta^2}{WL}$. Mismatch effects are typically expressed as an offset voltage v_{os}, corresponding to the input differential voltage $V_{sense} - V_{ref}$ which forces the outputs Out and $\overline{Out}$ to be equal. An equation for the offset can be derived assuming transistors M1 and M2 are operating in saturation:

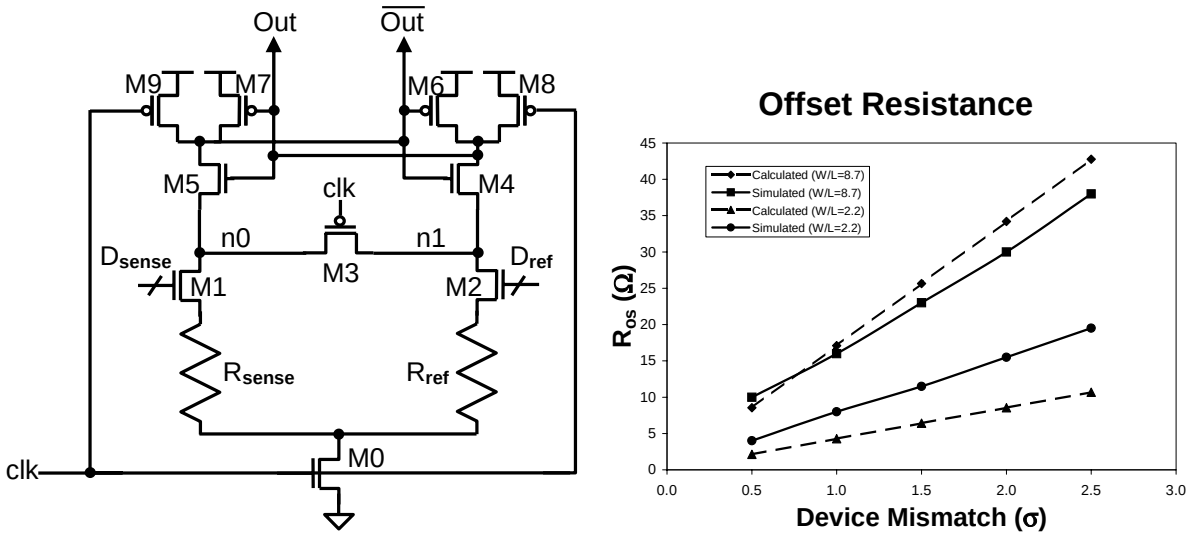
$$v_{os} = \Delta V_T + \frac{1}{(g_m/I_0)} \left(\frac{\Delta\beta}{\beta} \right) \tag{4}$$

where the terms are as defined above. Since the dynamic comparator does not operate under a steady-state bias, this equation is not strictly applicable. However, the critical part of circuit operation occurs in the initial discharge of nodes $n0$ and $n1$. For the Wheatstone bridge sensor, the common-mode voltage input to the comparator is near $V_{dd}/2$, and so the transistors will be in saturation during the critical early part of the evaluation transient.

Using the sensitivity for the carbon nanotube mat sensor[2] and the relation $V_{sense} \cong V_{dd}(\Delta R/2R)$,we find that to detect a minimum gas concentration of 200 ppb with a power supply $V_{dd} = 1$ V results in $V_{sense} = 3.4$ mV. This minimum V_{sense} corresponds to a single LSB for the A/D converter and so we must choose W and L for devices M1 and M2 such that $v_{os} \leq 1.7$, or $\frac{1}{2}$ LSB. Using data summarized in[19,20] to extrapolate values for A_{VT} and A_β for a 90nm CMOS technology and assuming that threshold voltage mismatch is the dominant effect, the required area is $WL = 34.6\mu\text{m}^2$. This area is large in terms of the minimum device area in this technology but is modest compared to the sensor area. We simulated the comparator pulldown paths with $W = 17.3\mu$m and $L = 2.0\mu$m for transistors M1 and M2 to determine the offset voltage for a range of device mismatch. The results are plotted in Figure 12(b), which shows that the calculated offsets are about 18% below the simulated offsets. This is reasonably accurate given that numerous effects due to nonzero source-bulk bias and the dynamic nature of the circuit were ignored in the simple calculation. The figure plots the offset as both ΔV_T and $\Delta\beta/\beta$ are varied together from 0.5σ to 2.5σ and shows that the comparator resolution specification will be met over $> 99\%$ of mismatch.

4.2. Variable Conductance A/D Converter

An alternative to using charge redistribution is to exploit the variable conductance available through the reconfigurable sensor resistance. Rather than digitizing the voltage at the output of the Wheatstone bridge, the circuit compares the conductance of the two legs directly by incorporating them into a comparator circuit as shown in Figure 13(a). The calibration setting D_{sense} configures the sense leg for optimum gas sensitivity. During conversion, a set of digital codes is applied to D_{ref}, the comparator is evaluated using the clock signal for each code, and the output checked by digital logic to determine which code most closely corresponds to the sense leg resistance. Previous implementations of this converter relied on accurate digital-to-analog conversion to convert conductance to voltage,[21] but the gas sensing application does not require this since it relies on conductance directly. We are currently evaluating this converter architecture and comparing its performance in simulation to the charge redistribution approach.



(a) (b)

Figure 13. (a) Conductance-based successive approximation ADC architecture. (b) Comparator resistance offset.

The circuit in Figure 13(a) is very similar to the circuit in Figure 12(a), except that the resistances R_{sense} and R_{ref} ideally determine which node $n0$ and $n1$ discharges first. Consequently, any threshold voltage or current factor mismatch in the devices M1 and M2 will affect the total resistance of each pulldown path and limit the smallest resistance difference which can be resolved by the comparator. Since the calibration settings D_{sense} and D_{ref} are digital codes, the gates of M1 and M2 will be driven to V_{dd} if they are turned on, so consequently we expect M1 and M2 to largely be in the linear (triode) region. Similar to voltage offset v_{os}, we can derive a "resistance offset" ΔR which corresponds to the resistance difference that guarantees any threshold or current factor mismatch is overcome during comparator evaluation:

$$\Delta R \approx -\Delta R_M \left(\frac{R}{R_M}\right) = \left(\frac{\Delta\beta}{\beta} - \frac{\Delta V_T}{V_{gs} - V_T - V_{ds}/2}\right) R \tag{5}$$

where V_{gs}, V_T, and V_{ds} are the gate-source, threshold, and drain-source voltages and R_M is the large signal drain-source resistance of transistors M1 or M2, respectively, and R is the common-mode resistance between R_{sense} and R_{ref}. Note that the offset can be adjusted by varying the ratio between the transistor on resistances and the sensor common-mode resistance, which yields a different tradeoff than the current biasing available to minimize the voltage offset.

Figure 13(b) plots the calculated and simulated resistance offsets versus device mismatch for pulldown switches M1 and M2 having two alternative W/L ratios and the same area as the devices for the circuit in Figure 12(a). The simulated offset is typically better than the calculated offset for $W/L = 8.7$ and while the offset decreases as W/L is decreased (R_M is increased), it does not scale as quickly as Equation 5 indicates. This is likely due to a number of competing effects including a nonzero source-bulk voltage, the implicit negative feedback of the source resistance on the current through M1 and M2, and the dynamic nature of the circuit.

To detect a minimum concentration of 200 ppb results in a sensor resistance change of 36.7 Ω, and so the resistance offset due to comparator mismatch should be less than 18.3 Ω ($\frac{1}{2}$ LSB). For the same device area, Figure 13 shows that the resistance offset can be decreased significantly below this threshold for a wide range of mismatch with an appropriate device sizing. The tradeoff is that by increasing R_M, the evaluation time of the comparator is also increased, but this is unlikely to limit performance in most gas sensing applications.

5. FUTURE WORK

The ultimate goal of this project is to design and fabricate a manufacturable power-aware gas sensor, utilizing nanostructures for improved sensitivity and power efficiency. The previous sections describe some of the components and architectures needed to accomplish this goal. However, further investigation into three key areas are needed: 1) device characterization for improved modeling, 2) circuit investigations into power and accuracy trade-offs and 3) system-level policies to govern sensor operation and adapt the sensor to meet end-user requirements.

Further research into process improvements and characterization of nanodevices is crucial for their widespread adoption. In particular, better understanding of the causes in process variation will lead to improved optimization models. Current work in this area includes developing statistical methods of designing process-tolerant elements. Design of the sensor elements will also require improved gas response characterization of these devices, as the resistance and physical/chemical properties change with molecular absorption. In the extreme case, sensitivity is ultimately limited by the intrinsic noise of the devices. Noise characterization will affect both circuit implementation and architectural choice.

As MOSFET technology shrinks further into deep submicron, the increasing effects of device mismatch and reductions in supply voltage make it increasingly difficult to operate analog circuits. Indeed, the small-signal approximations used in conventional analog circuit design (assuming constant current biases and operation in the saturation region), are becoming less and less applicable. New design styles involving nonlinear and time-varying analog circuits such as the dynamic comparator discussed above are currently being investigated for power reduction and increased input range. Subthreshold-based circuits are also another potential area where the power/accuracy trade-off could be better exploited. The vast numbers of transistors available provides opportunities for digital compensation of analog circuits and digital postprocessing of sensor data to improve system performance.

As the fundamental limitations of devices are approached, new system architectures must be developed that compensate for wider statistical variation. Two techniques currently being explored are sensing element redundancy and self-aware system design that can adapt to changing requirements through self-configuration. One example of the latter is the application of ultraviolet (UV) light to saturated sensing elements. It has been shown that UV illumination can reduce the recovery time of SWNT sensors from 10 hours to 10 minutes, enabling increased sampling rate.[2] It is also possible to use the application of UV light as a "quench" to quickly reset the sensor back to baseline conditions for optimum sensitivity. Through a clever UV illumination policy, it is possible for a sensor to maintain a large dynamic range without compromising sensitivity.[22] Hence, a system could overcome its current limitations through adaptation.

6. CONCLUSIONS

We have presented an integrated sensor and interface circuit design that focuses on the principle of self-calibration to deliver dramatically improved gas sensing system performance from nanoscale sensor technology. Our design exploits the high sensitivity, high molecular selectivity, and low power of carbon nanotube and silicon nanowire sensing elements while addressing the challenges of manufacturing variation and mismatch in both the sensing elements and deep submicron CMOS transistors.

At the core of our design is the use of multiple sensor arrays to perform dynamic calibration. By optimizing these sensor arrays, significant reductions in sensor variation can be obtained with minimal increase in sensor area. We have demonstrated these reductions through analytical techniques applied to both carbon nanotube and silicon nanowire variations. Furthermore, we have analyzed the potential of using dynamic comparator circuits as the sensor interface. These circuits offer drastically reduced power consumption by exploiting the low data rate requirements for typical gas sensing applications to allow for long comparator evaluation times. In 90 nm CMOS, input device area on the order of 35 μm^2 enables gas sensing resolution of 200 ppb for both conventional and variable conductance A/D converters. Further improvements in resolution are available for lower conversion speed. The dramatic improvements in power efficiency and cost reductions achievable by the combination of nanoscale sensing elements and CMOS circuits will create exciting new opportunities for sensors in critical areas such as environmental science, chemistry, and public safety.

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