

EEC 216 W09 Problem Set #1 Solutions

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Problem 1

1.1 Figure 1 shows the layout for a minimum-sized NMOS device for computing the width, source/drain area, and source/drain perimeter, based on the MOSIS DEEP submicron rules for $\lambda = 0.024\mu\text{m}$. The formulas and their values are entered into Table 1. It is also acceptable to use the alternative contact rules (Rule 6.2.b), in which case the ACTIVE overlap of CONTACT is 1λ for a minimum NMOS width of 4λ and the minimum extension of ACTIVE beyond the polysilicon gate is 5λ (**5 points**).

Two possible ways of determining the sizing are to perform a DC sweep of the inverter input voltage and size the PMOS so that the transition from high to low occurs when the input is at $\frac{V_{DD}}{2}$. This approach is shown in Figure 2 which displays the V_{in} versus V_{out} curve for three possible sizings. An alternative is to tie the output of the inverter back to the input and adjust the PMOS sizing until it settles to $\frac{V_{DD}}{2}$. This approach is shown for three PMOS sizes in Figure 2, which displays the inverter output voltage in feedback. A P/N ratio of 1, 2, or 3 is reasonably close, but a ratio of 2 is probably the most appropriate choice since it roughly balances the mobility ratios without using too much area for the PMOS device. This ratio is used to compute the PMOS parameters in Table 1 (**5 points**) Similar approaches can be used to size the inverters for thresholds of $0.4V_{DD}$ (which requires a nonminimum channel length PMOS) and $0.6V_{DD}$ (which requires a very large width PMOS device) (**10 points**).

V_{SW}	Device	Length	Width	PD/PS	AD/AS
$\frac{V_{DD}}{2}$	NMOS	$0.048\mu\text{m}$	$5\lambda = 0.12\mu\text{m}$	$1 \cdot 5\lambda + 2 \cdot 5.5\lambda = 0.384\mu\text{m}$	$5 \cdot 5.5\lambda^2 = 0.01584\mu\text{m}^2$
	PMOS	$0.048\mu\text{m}$	$7\lambda = 0.168\mu\text{m}$	$1 \cdot 7\lambda + 2 \cdot 5.5\lambda = 0.432\mu\text{m}$	$7 \cdot 5.5\lambda^2 = 0.0222\mu\text{m}^2$
$0.4V_{DD}$	NMOS	$0.048\mu\text{m}$	$5\lambda = 0.12\mu\text{m}$	$0.384\mu\text{m}$	$0.01584\mu\text{m}^2$
	PMOS	$45\lambda = 1.08\mu\text{m}$	$5\lambda = 0.12\mu\text{m}$	$0.384\mu\text{m}$	$0.01584\mu\text{m}^2$
$0.6V$	NMOS	$0.048\mu\text{m}$	$5\lambda = 0.12\mu\text{m}$	$0.384\mu\text{m}$	$0.01584\mu\text{m}^2$
	PMOS	$0.048\mu\text{m}$	$400\lambda = 9.6\mu\text{m}$	$9.864\mu\text{m}$	$1.267\mu\text{m}^2$

Table 1: CMOS Inverter Sizing.

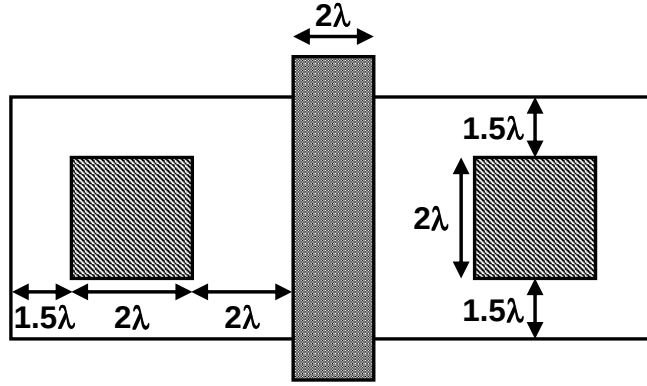


Figure 1: Layout of minimum-sized NMOS device.

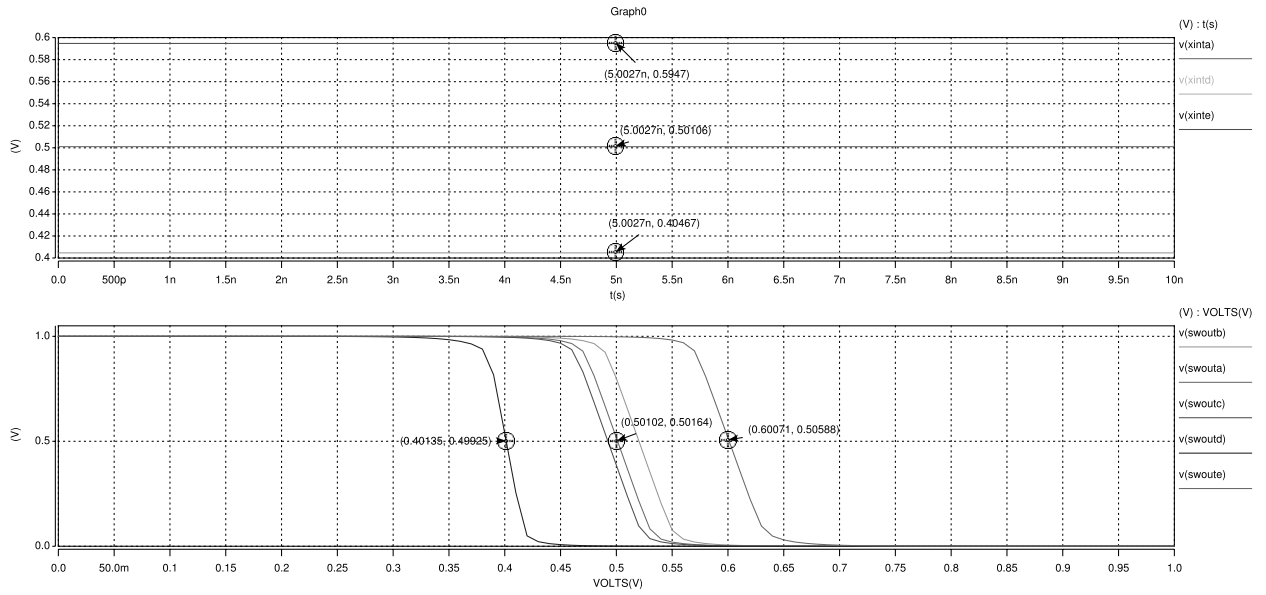


Figure 2: Inverter sizing based on inverter output feedback and on DC input voltage sweep.

The following Hspice file contains the inverter designs for this problem.

```
* EEC 216 W09 Problem Set 1 Inverter Sizing

* Inverter: Vdd/2
* -----
.macro invA in out
Xp0 vdd in out pfet Wi='7*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom

.macro invTA in out
Xp0 vcc in out pfetT Wi='7*lambda'
Xn0 gnd in out nfetT Wi='5*lambda'
.eom

* Inverter: Traditional Sizing
* -----
.macro invB in out
Xp0 vdd in out pfet Wi='3*5*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom

* Inverter: All Minimum
* -----
.macro invC in out
Xp0 vdd in out pfet Wi='1*5*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom

* Inverter: 0.4*Vdd
* -----
.macro invD in out
Xp0 vdd in out pfet Wi='1*5*lambda' Le='45*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom

.macro invTD in out
Xp0 vcc in out pfetT Wi='1*5*lambda' Le='45*lambda'
Xn0 gnd in out nfetT Wi='5*lambda'
.eom

* Inverter: 0.6*Vdd
* -----
.macro invE in out
```

```
Xp0 vdd in out pfet Wi='400*lambda' Le='2*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom
```

```
.macro invTE in out
Xp0 vcc in out pfetT Wi='400*lambda' Le='2*lambda'
Xn0 gnd in out nfetT Wi='5*lambda'
.eom
```

The following Hspice deck was used to generate the figures for this solution (note that in some SPICE implementations, the .alter commands result in incorrect simulation, in that case one must cut-and-paste the different macros into separate SPICE files and simulate them individually):

```
* EEC 216 W09 Problem Set 1 Number 1.1
* File: ps1n1d1.sp
* Author: Raj Amirtharajah (ramirtha@ece.ucdavis.edu)
* Date: 01/08/09
```

```
**
```

```
**
```

```
** Problem Set 1
```

```
**
```

```
** Problem 1.1: Static CMOS Sizing
```

```
** Last edited: Jan 8 14:35 2009 (ramirtha)
```

```
**-----
```

```
.include 'PTM45nm_LP.sp'
```

```
.param lambda=24nm vdd=1.0V vsweep=0V
```

```
.options accurate post
```

```
.temp 27
```

```
.tran 2ps 10.0ns
```

```
.dc vsweep start=0V stop=1.0V step=10mV
```

```
.global vdd gnd
```

```
.probe
```

```
.op
```

```
.nodeset swout=vdd
```

```
* Power Supplies
```

```
Vvdd vdd gnd dc=vdd
```

```
Vsweep swin gnd dc=vsweep
```

```
* NOTE: DEEP submicron scalable rules for contacts set the minimum width
```

```

* as  $1.5+2+1.5=5$  lambda, and minimum S/D area as  $5 \text{ lambda} \times 2+2+1.5=5.5$ 
*  $\text{lambda} = 27.5 \text{ lambda}^2$ . S/D perimeter is  $5+2 \times 5.5 \text{ lambda} = 16 \text{ lambda}$ .

```

```

* Parameters

```

```

* -----

```

```

.param Wmin='5*lambda'

```

```

* Three terminal FET macros

```

```

* -----

```

```

.macro nfet s g d Le='2*lambda' Wi=Wmin

```

```

MNO s g d gnd nmos L=Le W=Wi AS='5.5*lambda*Wi' PS='2*5.5*lambda+Wi'

```

```

+ AD='5.5*lambda*Wi' PD='2*5.5*lambda+Wi'

```

```

.eom

```

```

.macro pfet s g d Le='2*lambda' Wi=Wmin

```

```

MP0 s g d vdd pmos L=Le W=Wi AS='5.5*lambda*Wi' PS='2*5.5*lambda+Wi'

```

```

+ AD='5.5*lambda*Wi' PD='2*5.5*lambda+Wi'

```

```

.eom

```

```

* Inverter Designs

```

```

* -----

```

```

.include 'ps1inverters.sp'

```

```

* Sizing Test: Feedback

```

```

* -----

```

```

XdutA0 xintA xintA invA

```

```

XdutB0 xintB xintB invB

```

```

XdutC0 xintC xintC invC

```

```

XdutD0 xintD xintD invD

```

```

XdutE0 xintE xintE invE

```

```

* Sizing Test: DC Sweep

```

```

* -----

```

```

XdutA1 swin swoutA invA

```

```

XdutB1 swin swoutB invB

```

```

XdutC1 swin swoutC invC

```

```

XdutD1 swin swoutD invD

```

```

XdutE1 swin swoutE invE

```

```

.end

```

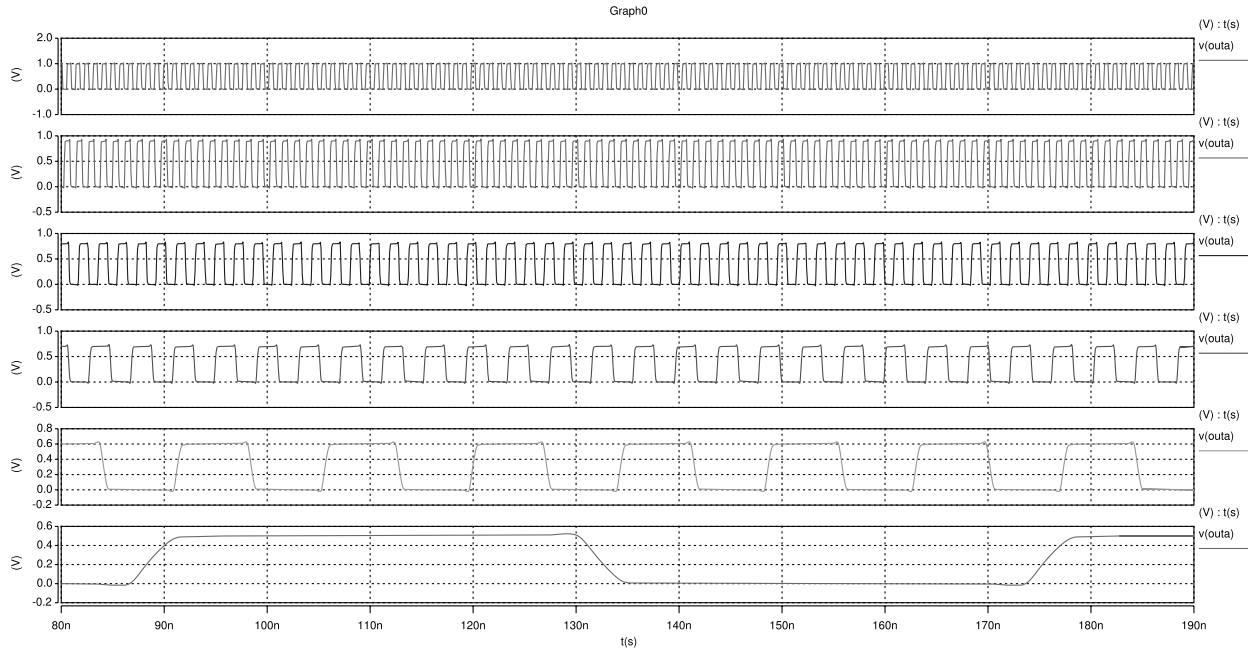


Figure 3: Ring oscillator waveforms at different supply voltages ($\frac{V_{DD}}{2}$ switching threshold).

1.2 Figure 3, 4, and 5 show the ring oscillator waveform outputs at the supply voltages tested for all three inverter thresholds. As the threshold is decreased below $V_{DD}/2$, the high-low transition occurs faster and the low-high transition is slower. The opposite effect occurs when the threshold is raised above $V_{DD}/2$. The inverter delays are listed in Tables 2, 4, and 3 (**10 points**). Note that using the 50%-50% delay specification can lead to spurious results (negative delays) for skewed inverter sizes. This occurs because the output switches through the $V_{DD}/2$ point before the input completes its transition or reaches the same point. Another approach to measuring inverter delay is to divide the ring oscillator period by twice the number of inverter stages (a transition must propagate twice through the ring to go through two inversions). These results are tabulated in the fourth column of the tables and give a more correct average delay for the circuit. Figures 6, 7, and 8 plot the inverter delay as V_{DD} is varied from 0.5 V to 1.0 V as the solid line for each of the three inverter sizings (**10 points**).

An example spice deck for measuring inverter delays using ring oscillators follows (**5 points**). Note that there may be issues in using the .alter card. Also, you may need to edit the .measure cards to reference the correct rising and falling edges when measuring delays as some simulators will have different initial transients on the circuit nodes.

```
* EEC 216 W09 Problem Set 1 Number 1.2
* File: ps1n1d2.sp
* Author: Raj Amirtharajah (ramirtha@ece.ucdavis.edu)
* Date: 01/28/09
**
**
```

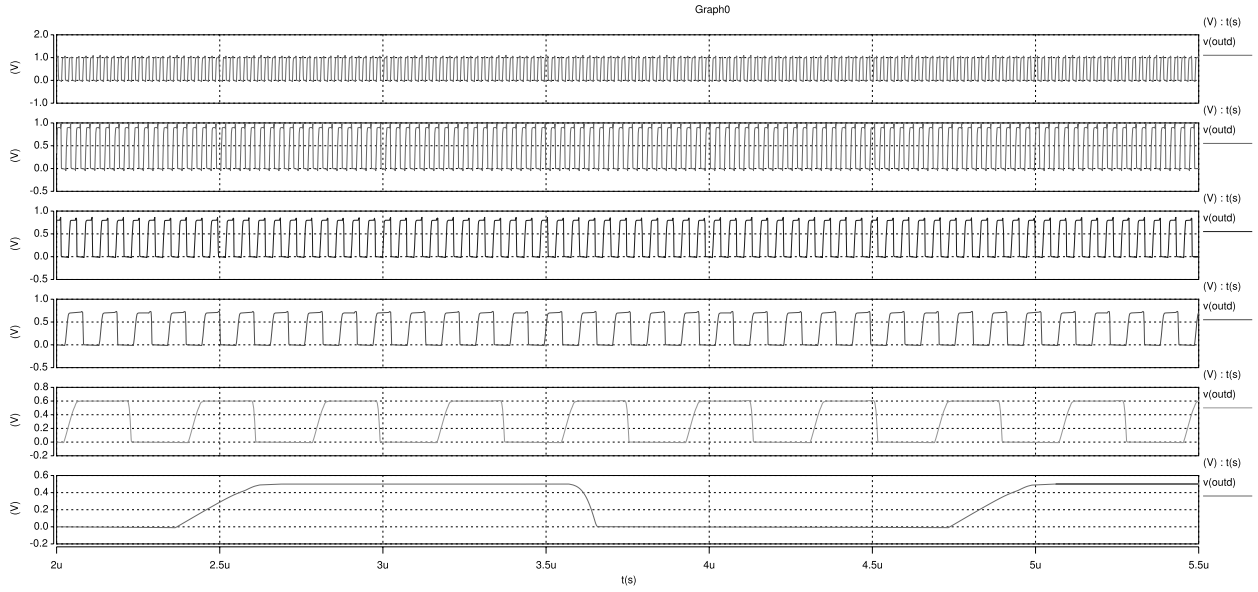


Figure 4: Ring oscillator waveforms at different supply voltages ($0.4V_{DD}$ switching threshold).

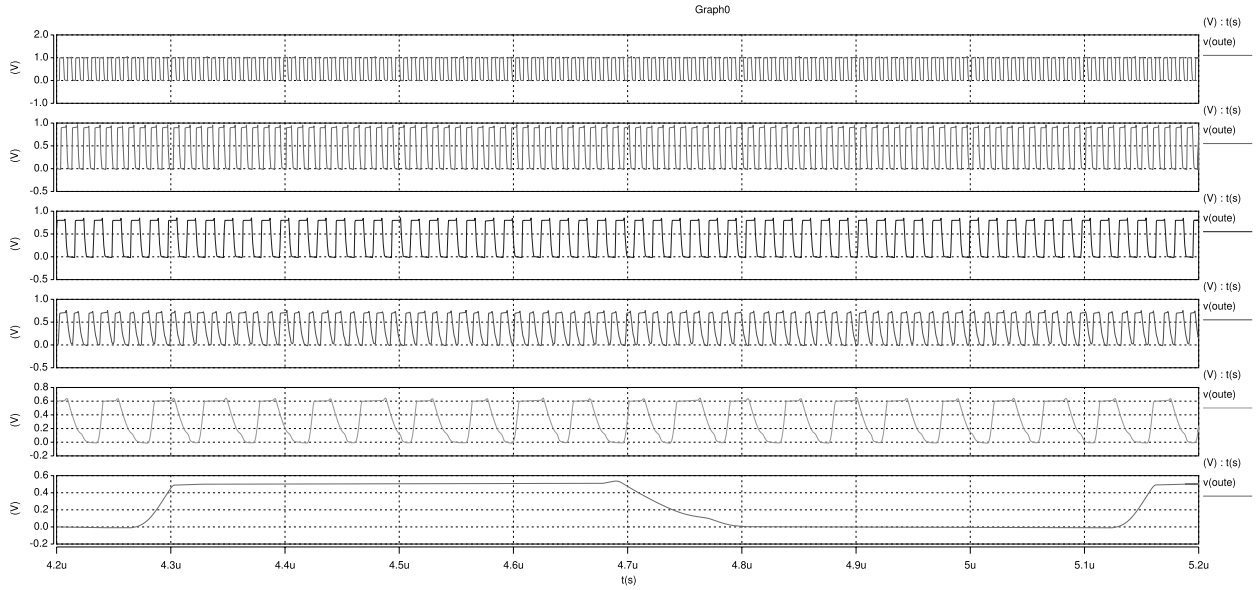


Figure 5: Ring oscillator waveforms at different supply voltages ($0.6V_{DD}$ switching threshold).

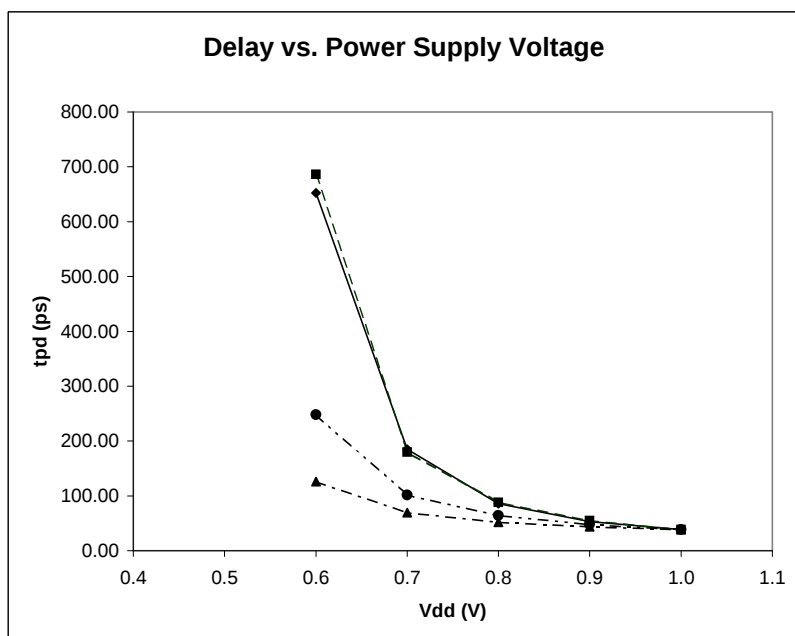


Figure 6: Inverter delay versus supply voltage ($\frac{V_{DD}}{2}$ switching threshold).

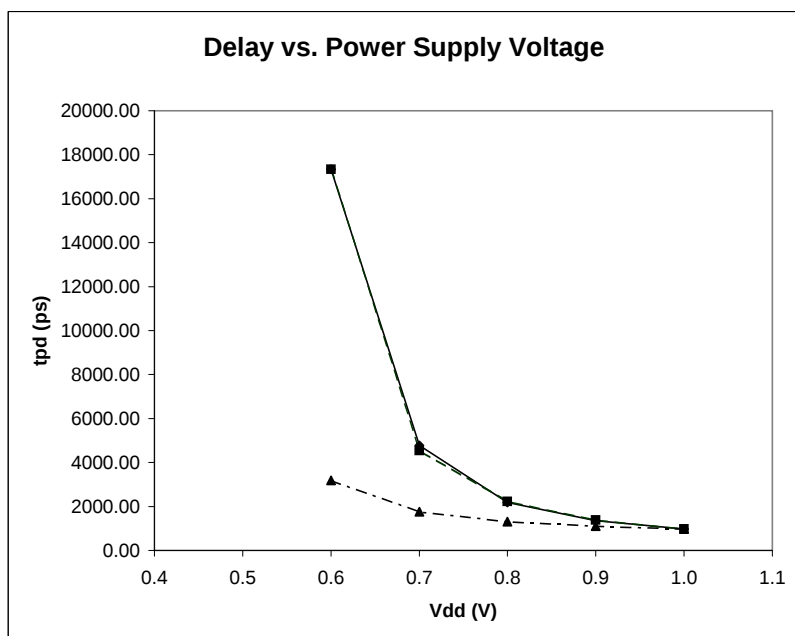


Figure 7: Inverter delay versus supply voltage ($0.4V_{DD}$ switching threshold).

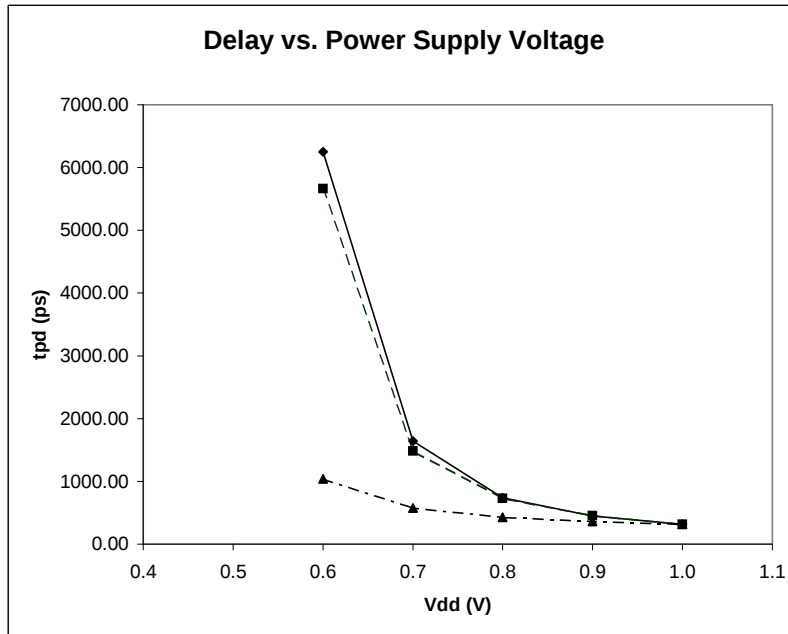


Figure 8: Inverter delay versus supply voltage ($0.6V_{DD}$ switching threshold).

** Problem Set 1

**

** Problem 1.2: Voltage-Delay Tradeoff

** Last edited: Jan 29 08:07 2009 (ramirtha)

**-----

.include 'macros.sp'

.include 'PTM45nm_LP.sp'

.param lambda=24nm vdd=0.5V

.options accurate post probe

.temp 27

.tran 20ps 10.0us

.global vdd gnd

.probe v(XringA.n0) v(XringA.n1) v(XringA.n2) v(outA)

.probe v(XringD.n0) v(XringD.n1) v(XringD.n2) v(outD)

.probe v(XringE.n0) v(XringE.n1) v(XringE.n2) v(outE)

* Power Supplies

Vvdd vdd gnd dc=vdd

* Inverters

	$V_{SW} = \frac{V_{DD}}{2}$			
V_{DD}	t_{PHL} (ps)	t_{PLH} (ps)	$T_{RO}/22$ (ps)	Delay (ps)
0.5 V	4050	3860	3955	3956
0.6 V	670	634	652	652
0.7 V	190	180	185	185
0.8 V	87.2	84.7	85.7	85.9
0.9 V	53.6	53.2	53.4	53.4
1.0 V	38.2	38.9	38.6	38.6

Table 2: CMOS Inverter Delay at Different Supply Voltages for Half V_{DD} Switching Threshold.

	$V_{SW} = 0.6V_{DD}$			
V_{DD}	t_{PHL} (ps)	t_{PLH} (ps)	$T_{RO}/22$ (ps)	Delay (ps)
0.5 V	50.6 ns	27.5 ns	39.1 ns	39.1 ns
0.6 V	7.94 ns	4.56 ns	2193	6251
0.7 V	2.15 ns	1.13 ns	577	1642
0.8 V	1020	467	742	742
0.9 V	635	261	150	448
1.0 V	483	154	318	318

Table 3: CMOS Inverter Delay at Different Supply Voltages for 0.6 V_{DD} Switching Threshold.

```
* -----
.include 'ps1inverters.sp'

.macro invT in out
Xp0 vcc in out pfetT Wi='2*5*lambda'
Xn0 gnd in out nfetT Wi='5*lambda'
.eom

* 11-Stage Ring Oscillators
* -----
.subckt ring11A out
.ic out=0V
.ic n1=0V
.ic n2=vdd
Xinv0 out n0 invA
Xinv1 n0 n1 invA
Xinv2 n1 n2 invA
Xinv3 n2 n3 invA
Xinv4 n3 n4 invA
Xinv5 n4 n5 invA
Xinv6 n5 n6 invA
```

	$V_{SW} = 0.4V_{DD}$			
V_{DD}	t_{PHL} (ps)	t_{PLH} (ps)	$T_{RO}/22$ (ps)	Delay (ps)
0.5 V	75.2 ns	140 ns	108 ns	108 ns
0.6 V	12.2 ns	22.5 ns	17.3 ns	17.3 ns
0.7 V	2970	6570	4768	4768
0.8 V	1140	3240	2188	2188
0.9 V	585	2110	1349	1349
1.0 V	361	1590	975	975

Table 4: CMOS Inverter Delay at Different Supply Voltages for 0.4 V_{DD} Switching Threshold.

```
Xinv7 n6  n7  invA
Xinv8 n7  n8  invA
Xinv9 n8  n9  invA
Xinv10 n9  out invA
.ends
```

```
.subckt ring11D out
.ic out=0V
.ic n1=0V
.ic n2=vdd
Xinv0 out  n0  invD
Xinv1 n0  n1  invD
Xinv2 n1  n2  invD
Xinv3 n2  n3  invD
Xinv4 n3  n4  invD
Xinv5 n4  n5  invD
Xinv6 n5  n6  invD
Xinv7 n6  n7  invD
Xinv8 n7  n8  invD
Xinv9 n8  n9  invD
Xinv10 n9  out invD
.ends
```

```
.subckt ring11E out
.ic out=0V
.ic n1=0V
.ic n2=vdd
Xinv0 out  n0  invE
Xinv1 n0  n1  invE
Xinv2 n1  n2  invE
Xinv3 n2  n3  invE
Xinv4 n3  n4  invE
Xinv5 n4  n5  invE
```

```

Xinv6 n5    n6    invE
Xinv7 n6    n7    invE
Xinv8 n7    n8    invE
Xinv9 n8    n9    invE
Xinv10 n9   out   invE
.ends

XringA outA ring11A
XringD outD ring11D
XringE outE ring11E

.measure tran tpdnA trig v(XringA.n1) val='vdd/2' rise=2
+                  targ v(XringA.n2) val='vdd/2' fall=2
.measure tran tpupA trig v(XringA.n1) val='vdd/2' fall=2
+                  targ v(XringA.n2) val='vdd/2' rise=2

.measure tran tpeuA trig v(outA) val='vdd/2' rise=2
+                  targ v(outA) val='vdd/2' rise=3
.measure tran tpedA trig v(outA) val='vdd/2' fall=2
+                  targ v(outA) val='vdd/2' fall=3

.measure tran tpdnD trig v(XringD.n1) val='vdd/2' rise=2
+                  targ v(XringD.n2) val='vdd/2' fall=2
.measure tran tpupD trig v(XringD.n1) val='vdd/2' fall=2
+                  targ v(XringD.n2) val='vdd/2' rise=2

.measure tran tpeuD trig v(outD) val='vdd/2' rise=2
+                  targ v(outD) val='vdd/2' rise=3
.measure tran tpedD trig v(outD) val='vdd/2' fall=2
+                  targ v(outD) val='vdd/2' fall=3

.measure tran tpdnE trig v(XringE.n1) val='vdd/2' rise=2
+                  targ v(XringE.n2) val='vdd/2' fall=2
.measure tran tpupE trig v(XringE.n1) val='vdd/2' fall=2
+                  targ v(XringE.n2) val='vdd/2' rise=2

.measure tran tpeuE trig v(outE) val='vdd/2' rise=2
+                  targ v(outE) val='vdd/2' rise=3
.measure tran tpedE trig v(outE) val='vdd/2' fall=2
+                  targ v(outE) val='vdd/2' fall=3

.alter
.param vdd=0.6V

.alter

```

```

.param vdd=0.7V

.alter
.param vdd=0.8V

.alter
.param vdd=0.9V

.alter
.param vdd=1.0V

.end

```

1.2 (cont.) Figures 6, 7, and 8 also plot two alternative models for delay scaling with V_{DD} . The dashed curve assumes a quadratic dependence for I_{DS} on $V_{GS} - V_T$, corresponding to the classical model. The dash-dot curve represents a linear dependence. As can be seen from the first graph, the measured delay scaling is approximately quadratic, indicating that the classical model is reasonably applicable. A similar curve occurs for the third graph (switching threshold $0.6V_{DD}$). (**5 points**). A curve marked with circles is also shown in Figure 6, which corresponds to a dependence to the power 1.4.

1.3 Figures 9, 10, and 11 display the single inverter switching cycle and the corresponding supply current (**6 points**). The current shape matches intuition in that the current is drawn from the supply during charging of the output to V_{DD} . The other positive current spikes correspond to capacitive coupling on the output (the small blips can be seen on the output node) pushing charge into the supply. Note that the current is not particularly triangular in shape, so there is a component corresponding to the dynamic power and a component corresponding to short circuit current, which is especially important in the $0.4V_{DD}$ case since the rise time is so long. (**3 points**). For the $V_{DD}/2$ switching threshold, the average current is given by a measure card as $1.82\mu\text{A}$ which corresponds to an average power of $1.82\mu\text{W}$ (**2 points**). For the $0.4V_{DD}$ switching threshold, the average current is given by a measure card as 124 nA which corresponds to an average power of 124 nW (**2 points**). For the $0.6V_{DD}$ switching threshold, the average current is given by a measure card as $5.27\mu\text{A}$ which corresponds to an average power of $5.27\mu\text{W}$ (**2 points**). The average current for the $0.4V_{DD}$ case is so low because its switching frequency is much lower than the $V_{DD}/2$ case. Note also the significant leakage current for this inverter sizing. Although the oscillator frequency of the $0.6V_{DD}$ design is also very low, it has so much more switched capacitance that the average power is higher.

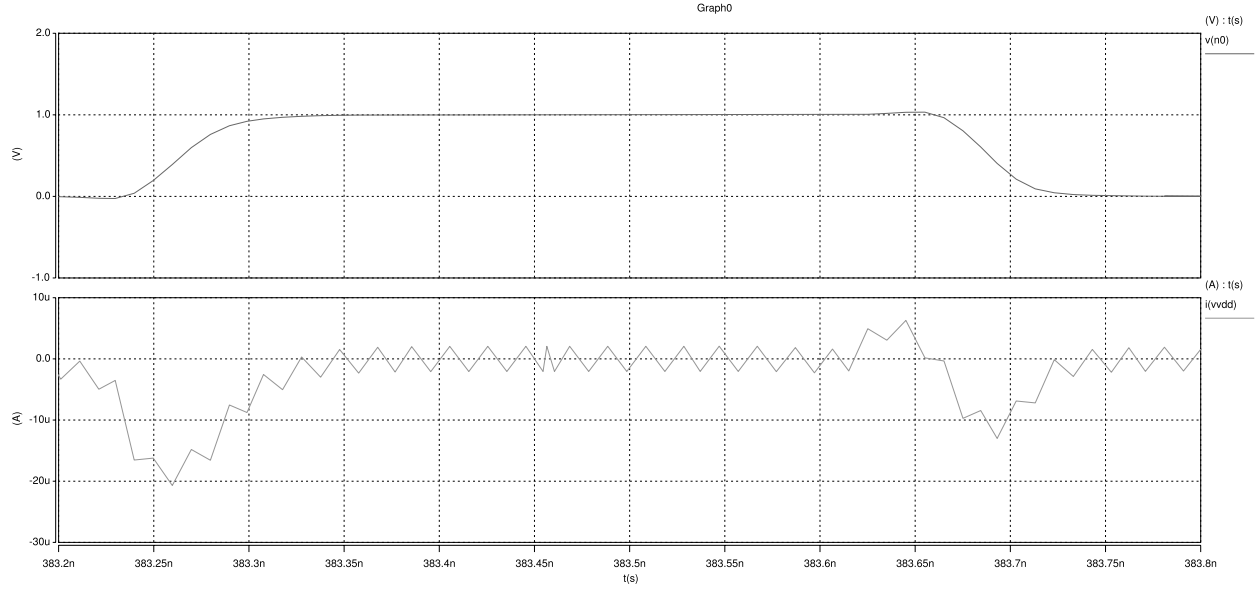


Figure 9: Single charge-discharge cycle and corresponding power supply current for a single inverter in the ring oscillator (switching threshold $V_{DD}/2$).

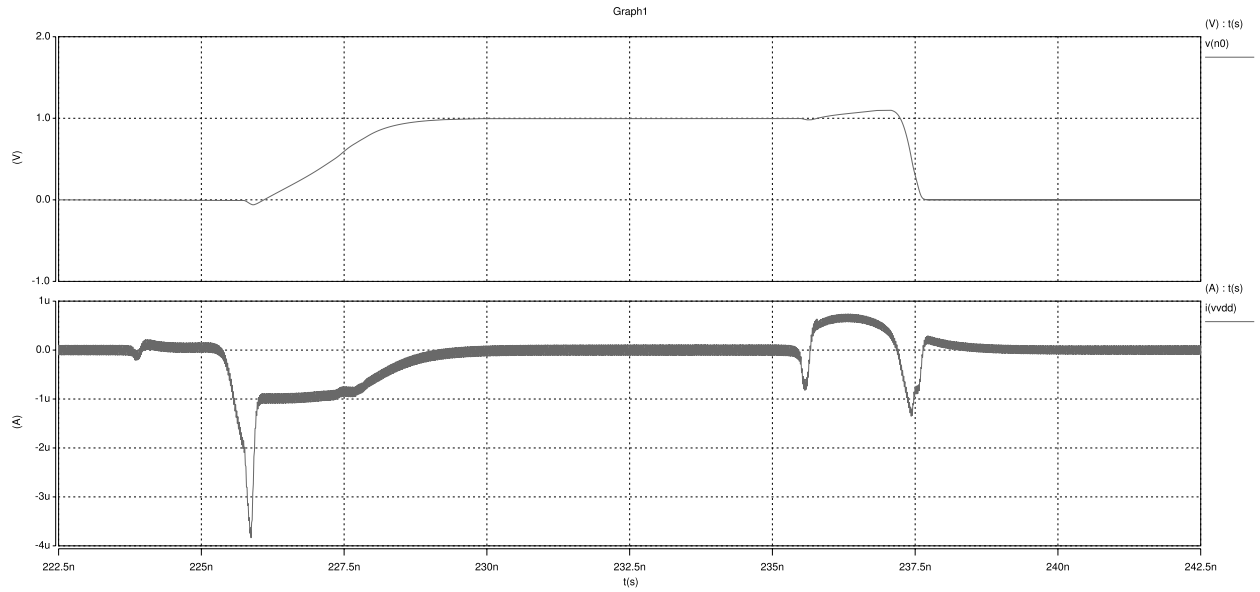


Figure 10: Single charge-discharge cycle and corresponding power supply current for a single inverter in the ring oscillator (switching threshold $0.4V_{DD}$).

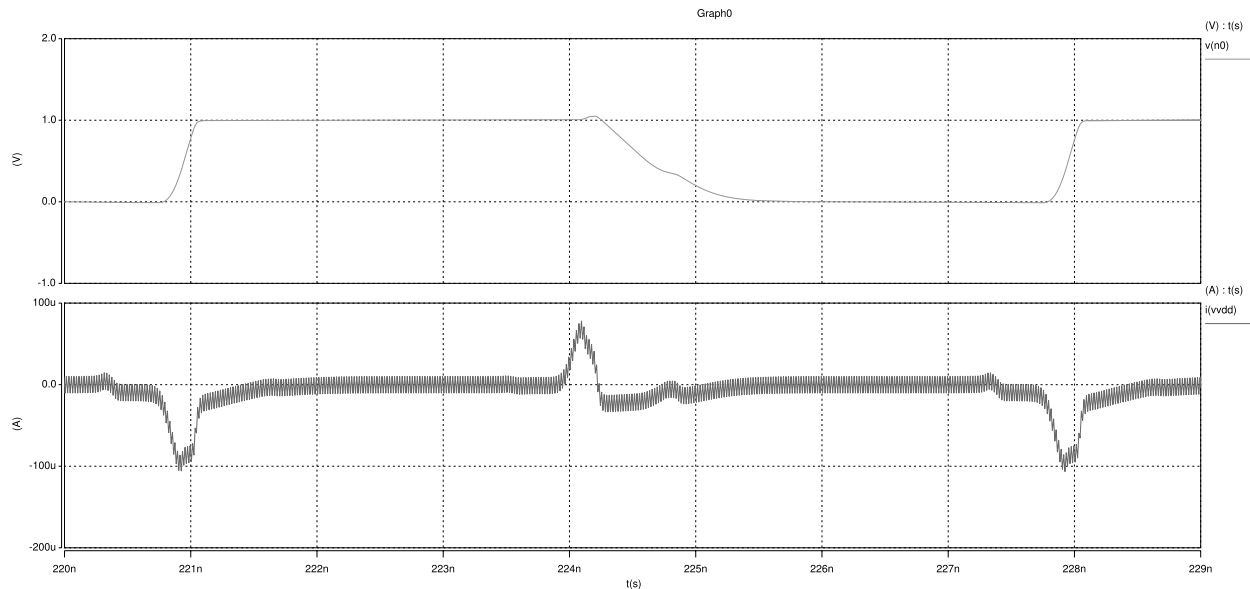


Figure 11: Single charge-discharge cycle and corresponding power supply current for a single inverter in the ring oscillator (switching threshold $0.6V_{DD}$).

The spice deck which generated the plots in Figures 9, 10, and 11 and the measured currents is (**3 points**):

```
* EEC 216 W09 Problem Set 1 Number 1.3
* File: ps1n1d3.sp
* Author: Raj Amirtharajah (ramirtha@ece.ucdavis.edu)
* Date: 01/17/05
**
**
** Problem Set 1
**
** Problem 1.3: Power Consumption
** Last edited: Jan 29 12:58 2009 (ramirtha)
**-----
```

```
.include 'macros.sp'
.include 'PTM45nm_LP.sp'
.param lambda=24nm vdd=1.0V

.options accurate post probe absmos=1e-15 relmos=0.001 abstol=1e-15
.temp 27

.tran 5ps 400.0ns

.global vdd vcc gnd
```

```
.probe v(Xring.n0) v(Xring.n1) v(Xring.n2) v(out)
```

```
* Power Supplies
```

```
Vvdd vdd    gnd dc=vdd
```

```
Vvcc vcc    gnd dc=vdd
```

```
* Inverters
```

```
* -----
```

```
.include 'ps1inverters.sp'
```

```
* 11-Stage Ring Oscillators
```

```
* -----
```

```
.subckt ring11A out
```

```
.ic out=0V
```

```
.ic n1=0V
```

```
.ic n2=vdd
```

```
Xinv0 out  n0  invA
```

```
Xinv1 n0   n1  invTA
```

```
Xinv2 n1   n2  invTA
```

```
Xinv3 n2   n3  invTA
```

```
Xinv4 n3   n4  invTA
```

```
Xinv5 n4   n5  invTA
```

```
Xinv6 n5   n6  invTA
```

```
Xinv7 n6   n7  invTA
```

```
Xinv8 n7   n8  invTA
```

```
Xinv9 n8   n9  invTA
```

```
Xinv10 n9  out invTA
```

```
.ends
```

```
.subckt ring11D out
```

```
.ic out=0V
```

```
.ic n1=0V
```

```
.ic n2=vdd
```

```
Xinv0 out  n0  invD
```

```
Xinv1 n0   n1  invTD
```

```
Xinv2 n1   n2  invTD
```

```
Xinv3 n2   n3  invTD
```

```
Xinv4 n3   n4  invTD
```

```
Xinv5 n4   n5  invTD
```

```
Xinv6 n5   n6  invTD
```

```
Xinv7 n6   n7  invTD
```

```
Xinv8 n7   n8  invTD
```

```
Xinv9 n8   n9  invTD
```

```
Xinv10 n9  out invTD
```

```
.ends
```

```

.subckt ring11E out
.ic out=0V
.ic n1=0V
.ic n2=vdd
Xinv0 out  n0  invE
Xinv1 n0    n1  invTE
Xinv2 n1    n2  invTE
Xinv3 n2    n3  invTE
Xinv4 n3    n4  invTE
Xinv5 n4    n5  invTE
Xinv6 n5    n6  invTE
Xinv7 n6    n7  invTE
Xinv8 n7    n8  invTE
Xinv9 n8    n9  invTE
Xinv10 n9   out invTE
.ends

Xring out ring11A
* Xring out ring11D
* Xring out ring11E

.measure tran tpdn trig v(Xring.n1) val='vdd/2' rise=2
+
      targ v(Xring.n2) val='vdd/2' fall=2
.measure tran tpup trig v(Xring.n1) val='vdd/2' fall=2
+
      targ v(Xring.n2) val='vdd/2' rise=2
.measure tran avgcur AVG i(Vvdd)

.end

```

Problem 2

2.1 Each of the equations in Chandrakasan's paper reflect purely dynamic power: $P = CV^2f$ [1]. We add to each of the equations a leakage term which is proportional to area, such that total power is now $P_{TOT} = CV^2f + kI_0AV$ (**2 points**). The modified equations and the relative leakage currents I_0 follow.

Reference datapath (**2 point**):

$$P_{ref} = C_{ref}V_{ref}^2f_{ref} + kI_0AV_{ref} \quad (1)$$

$$I_0(ref) = \frac{C_{ref}V_{ref}f_{ref}}{kA} \quad (2)$$

Parallel datapath (**2 point**):

$$P_{par} = (2.15C_{ref})(0.58V_{ref})^2 \left(\frac{f_{ref}}{2} \right) + kI_0(3.4A)(0.58V_{ref}) \quad (3)$$

$$\begin{aligned} I_0(par) &= \frac{(2.15C_{ref})(0.58V_{ref})f_{ref}}{kA(2)(3.4)} \\ &= (0.1834)I_0(ref) \end{aligned} \quad (4)$$

Pipelined datapath (**2 point**):

$$P_{pipe} = (1.15C_{ref})(0.58V_{ref})^2 f_{ref} + kI_0(1.3A)(0.58V_{ref}) \quad (5)$$

$$\begin{aligned} I_0(pipe) &= \frac{(1.15C_{ref})(0.58V_{ref})f_{ref}}{kA(1.3)} \\ &= (0.51)I_0(ref) \end{aligned} \quad (6)$$

Parallel-Pipelined datapath (**2 point**):

$$P_{parpipe} = (2.5C_{ref})(0.4V_{ref})^2 \left(\frac{f_{ref}}{2} \right) + kI_0(3.7A)(0.4V_{ref}) \quad (7)$$

$$\begin{aligned} I_0(parpipe) &= \frac{(2.5C_{ref})(0.4V_{ref})f_{ref}}{kA(2)(3.7)} \\ &= (0.1351)I_0(ref) \end{aligned} \quad (8)$$

By increasing the number of devices through parallelism and pipelining, the designer also increases the amount of leakage current since all of those extra devices will leak when not in use. Thus, the most area-intensive architecture (parallel-pipelined) only needs 13% of the per-device leakage of the reference datapath for leakage power to contribute equally to dynamic power for total power consumption. Partly this is due to reducing the dynamic power and partly this is due to increased sensitivity to leakage through a larger number of devices. Now the tradeoff is not just area for power, but area plus leakage power for dynamic power (**2 points**). Because there is now a power penalty associated with these architectural changes, one is less likely to be as aggressive utilizing them, which means in general the optimal supply voltage will be higher for the overall system (**2 points**). The designer is more likely to use a single datapath with less pipelining, and so will keep the power supply voltage higher, expending more dynamic power but keeping leakage to a minimum (**1 points**).

References

- [1] A. Chandrakasan, S. Sheng, and R. W. Broderson, "Low-power CMOS digital design," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 4, pp. 473–84, April 1992.