

# EEC 216 Winter 2009 Problem Set #1

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**Reading:** Chandrakasan, et al. “Low-Power CMOS Digital Design”, 1992. The classic recent work on low power design [1]. Available on the course web page.

## 1 Sizing, Delay, and Total Power at the 45 nm Process Node

**Simulation:** This problem requires extensive use of HSPICE. For information on running HSPICE on the UCD ECE department network, follow this URL:

<http://www.ece.ucdavis.edu/cad/hspice/index.html>.

If you want to use another version of Spice (e.g. PSpice, Berkeley Spice, Spectre), you must get permission from the instructor first.

**Device Models:** This problem relies on freeware models from the Predictive Technology Model Group [2, 3]. Download the 45nm low power CMOS model file `PTM45nm_LP.sp` from the course web site and include it in your Spice deck.

**Problem 1.1** (20 points) **Static CMOS sizing.** Determine the appropriate P/N width ratio for this process by simulating an inverter with a minimum width and gate length NMOS. In this class, we will assume a generic process based on the MOSIS Scalable CMOS design rules for deep submicron. The design rules are available online at:

[http://www.mosis.org/Technical/Layermaps/lm-scmos\\_scn6m.html](http://www.mosis.org/Technical/Layermaps/lm-scmos_scn6m.html)

Use the DEEP column for the assumed layout rules to compute such things as minimum transistor width, source/drain perimeter and source/drain area. A minimum width device is no smaller than a minimum contact width, i.e. no “dogbone” devices are allowed.  $\lambda$  for this process is 24 nm. Assume  $V_{DD}$  is 1.0 V.

Hint: The only layers you should be concerned with for this problem are ACTIVE, POLY, and CONTACT.

We will design three different inverters with different switching thresholds by adjusting the P device sizing. Size the P such that the inverter output high-to-low switching threshold  $V_{SW}$  is  $\frac{V_{DD}}{2}$ ,  $0.4V_{DD}$ , and  $0.6V_{DD}$ . You may need a nonminimum length P device for one of the inverters. Assume that  $V_{DD}$  for this process is 1.0 Volts unless told otherwise. Fill in Table 1 with the appropriate numbers from your simulation. You must turn in the Spice deck and the simulation results (for example, a waveform plot) confirming that the sizing is correct.

$V_{SW}$	Device	Length	Width	PD/PS	AD/AS
$\frac{V_{DD}}{2}$	NMOS	0.048 $\mu\text{m}$			
	PMOS				
$0.4V_{DD}$	NMOS	0.048 $\mu\text{m}$			
	PMOS				
$0.6V_{DD}$	NMOS	0.048 $\mu\text{m}$			
	PMOS				

Table 1: CMOS Inverter Sizing.

**Problem 1.2** (30 points) **Voltage-Delay Tradeoff.** Simulate an 11 stage ring oscillator based on the inverter device sizes determined in the first part. Measure, tabulate, and plot a single inverter delay vs.  $V_{DD}$  for  $0.5V \leq V_{DD} \leq 1.0V$  in 100 mV increments. Use the 50-50 point between inverter input and output for both low-high ( $t_{PLH}$ ) and high-low ( $t_{PHL}$ ) transitions and compute the average for the inverter delay. Turn in your Spice deck along with the plot and fill in Table 2.

	$V_{SW} = \frac{V_{DD}}{2}$			$V_{SW} = 0.4V_{DD}$			$V_{SW} = 0.6V_{DD}$		
$V_{DD}$	$t_{PLH}$	$t_{PHL}$	Delay	$t_{PLH}$	$t_{PHL}$	Delay	$t_{PLH}$	$t_{PHL}$	Delay
0.5 V									
0.6 V									
0.7 V									
0.8 V									
0.9 V									
1.0 V									

Table 2: CMOS Inverter Delay at Different Supply Voltages.

(5 points) Based on the “classical” MOSFET models described in class, do the delay vs. supply voltage curves follow your intuition for how delay changes as voltage is scaled? If not, what are some possible reasons for the deviation from what’s expected? How does changing the inverter threshold affect the ring oscillator frequency and why?

**Problem 1.3** (15 points) **Average Total Power:** We’ve seen in lecture that short circuit current can be modeled as an additional load capacitor in parallel with the actual output load of a CMOS gate, and so the short circuit current contribution to total power can be lumped with the physical dynamic power. Simulate and measure the average current for the ring oscillators designed above for at least 10 charge and discharge cycles, at the nominal  $V_{DD}$ . Plot the inverter output voltage at a single node and the current draw for a single switching cycle on two sets of axes with the times aligned (for example, using the strip plot option in Cscope). Does the shape of the current match your intuition? Explain if it does not. What is the average total current and average total power for each oscillator? How does changing the inverter switching threshold affect the total power and why? Turn in your Spice deck along with the plot.

## 2 Architecture-Driven Voltage Scaling, Leakage Power, and Design Tradeoffs

**Problem 2.1** (15 points) Chandrakasan proposes an “architecture-driven voltage scaling” approach whereby adding parallel functional units or pipelining a functional unit can relax system clock frequency requirements or decrease critical path lengths, respectively. The speed improvement can be traded off for power by decreasing the supply voltage, so overall these techniques trade silicon area for power consumption. We would like to quantify how increased leakage power affects these tradeoffs in future CMOS technologies by estimating what the per-device leakage current must be for the leakage power component to equal the dynamic power component of the total power. Add a leakage power term to equations 7, 8, 9, and 10 from Chandrakasan’s paper. Assume that the per-device leakage current is  $I_0$  and total leakage current is directly proportional to area with proportionality constant  $k$ . Using the normalized areas in Table II, find  $I_0$  when the dynamic and leakage powers are equal for the reference, parallel, pipelined, and parallel-pipelined implementations. How does  $I_0$  vary with the choice of architecture? How should this knowledge influence which architectural approach should be taken to minimize total power?

## References

- [1] A. Chandrakasan, S. Sheng, and R. W. Broderson, “Low-power CMOS digital design,” *IEEE Journal of Solid-State Circuits*, vol. 27, no. 4, pp. 473–84, April 1992.
- [2] Nanoscale Integration and Modeling (NIMO) Group, Arizona State University. (2006, December) Predictive technology model (ptm). latest.html. [Online]. Available: <http://www.eas.asu.edu/ptm/>
- [3] W. Zhao and Y. Cao, “New generation of predictive technology model for sub-45 nm early design exploration,” *IEEE Trans. Electron Devices*, vol. 53, no. 11, pp. 2816–23, November 2006.