EEC 216 Winter 2008 Midterm

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Name:

Instructions: This test consists of 3 problems and 10 pages, including the cover sheet. Please make sure that you have all of them. You are allowed one sheet of $8\frac{1}{2}$ by 11 paper with writing on one side only and a calculator. State any assumptions you make and show complete work to receive credit. The time limit is 50 minutes. The problems are weighted as shown below:

Grading:

Problem	Maximum	Score
1	25	
2	13	
3	17	
Total	55	

1 Logic Design

For this exam, use the transistor parameters in Table 1. Assume all dimensions are in microns unless otherwise specified.

Parameter	NMOS	PMOS
V_t	0.2 V	-0.2 V
$k' = \mu C_{ox}$	200 μA/V^2	100 μA/V^2
W_{min}	2 μm	2 μm
L_{min}	1 μm	1 μm

Table 1: Problem 1 Transistor Parameters.

Problem 1.1 (**3 points**) **Logic Network Design.** Design a logic gate circuit using a minimum number of only 2-input NAND and NOR gates and inverters to implement the following logical expression. Be sure to label all inputs, outputs, and internal circuit nodes.

$$F = A + B \cdot C \tag{1}$$

Problem 1.2 (**3 points**) **Activity Factors.** Assume that A, B, and C are independent, identically distributed binary random variables, where the likelihood of any individual variable being 1 or 0 is the same. Find the activity factors $\alpha_{0\to1}$ for the output F and each internal node in your circuit above.

Problem 1.3 (**6 points**) **Static CMOS.** Draw a transistor-level schematic for a static CMOS circuit which implements the logical expression for F using a 3-input gate and a minimum-sized inverter. Implement the circuit using a minimum number of transistors.

Problem 1.4 (**4 points**) **Static CMOS Sizing.** Size the transistors in the circuit you designed for Problem 1.1 such that the worst case rise and fall times are equal to the minimum-sized inverter rise and fall times while minimizing the input capacitance to the logic gate. Label the sizes in your schematic for Problem 1.1, including the inverter.

Problem 1.5 (**6 points**) **Dynamic (Domino) Circuit Design.** Design a dynamic gate to implement Equation 1. Size the transistors such that the worst case rise and fall times on the dynamic node are equal to a minimum-sized inverter rise and fall time. Label all transistor sizes in your schematic. Make sure the circuit can be connected correctly to other dynamic logic circuits in the same style.

Problem 1.6 (3 points) Discussion. Which of the two circuits is faster? Which of the two circuits is better for low power design? Justify your answers.

Faster (circle one): 1.3 or 1.5

Lower Power (circle one): 1.3 or 1.5

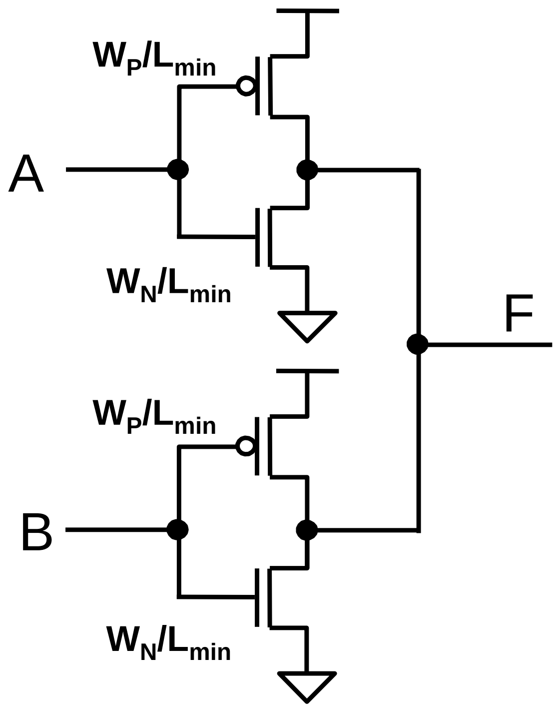

Figure 1: Logic gate. Transistor sizes are labeled in the figure.

2 Ratioed Circuit Design

Problem 2.1 (1 points) Circuit Function. Figure 1 shows a logic circuit which can implement one of two possible logic functions depending on the sizes of W_P and W_N. Circle which pair below:

OR / AND

NOR / NAND

XOR / XNOR

Problem 2.2 (**8 points**) **Circuit Sizing.** Using the transistor parameters in Table 1 and assuming $V_{DD} = 1\text{V}$, find the smallest W_P and W_N for each possible logic function implementation given that the worst case valid high output must satisfy $V_{OH} \geq 0.75V_{DD}$ and the worst case valid low output must satisfy $V_{OL} \leq 0.25V_{DD}$.

Logic Function:
$W_P =$
$W_N =$

Logic Function:
$W_P =$
$W_N =$

Problem 2.3 (**4 points**) **Static Power "Activity" Factor.** Assume inputs A and B are independent, identically distributed, binary random variables with equal probability of being a 0 or a 1. For each possible logic function, what percentage of time does the circuit in Figure 1 dissipate static power?

Logic Function:
% Static Power:

Logic Function:
% Static Power:

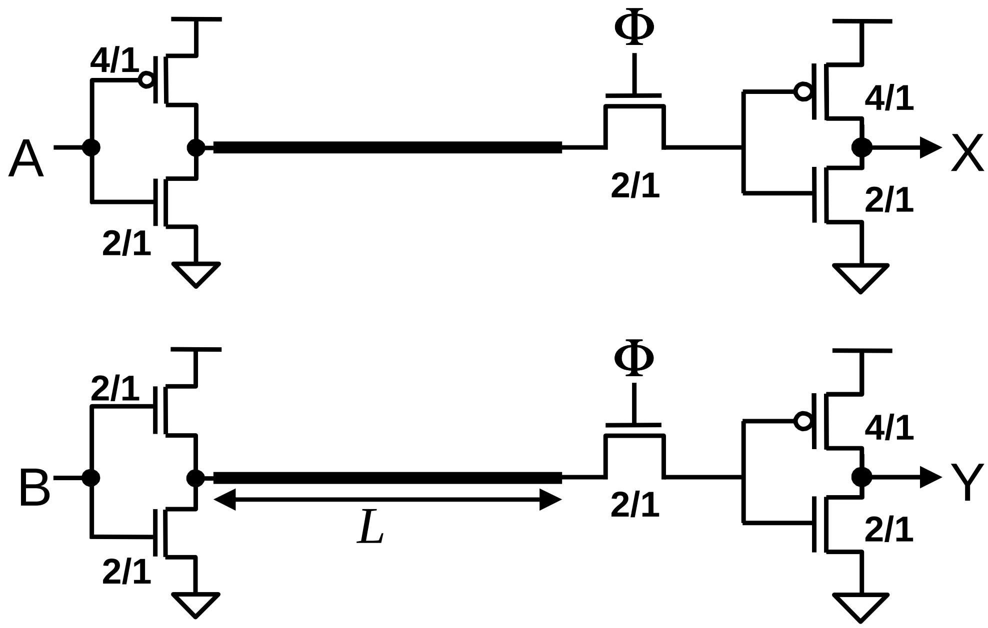

Figure 2: Two alternative circuits for driving a single long wire of length L.

Parameter	Metal 2
Sheet Resistance ($R_{sq.}$)	0.1 $\Omega/sq.$
Spacing (S)	500 nm
Thickness (T)	0.1 μm
Height (H, above substrate)	150 nm
Dielectric Constant (ϵ_r)	4.3 $\times$ 8.85e-12 F/m
Length (L, on figure)	1.5 cm
Width (W)	0.5 μm

Table 2: Problem 2 Interconnect Parameters.

3 Low Power Bus

Figure 2 shows two alternative circuits for driving a single long wire of length L. Assume the transistor parameters listed in Table 1 and the wire dimensions and parameters shown in Figure 2 and listed in Table 2. Also assume $V_{DD} = 1.0$V.

Problem 3.1 (**2 points**) **Wire Capacitance.** Calculate the total capacitance for the long wire of length L. Ignore any contribution of fringing fields or coupling capacitance.

Problem 3.2 (**5 points**) **Delay.** Estimate the worst case delay of driving the long wire for each of the two circuits above. Assume that the transistors operate ideally in the saturation region, inputs A and B are full-swing signals, neglect channel length modulation or any other short channel effects, and assume an ideal step waveform on the driver inputs.

Delay (Circuit $A - X$):

Delay (Circuit $B - Y$):

Problem 3.3 (**5 points**) **Dynamic Power.** Compute the dynamic power of driving the long wire for each of the two circuits above, assuming $\alpha_{0\to1} = 0.25$ for the wire, $f = 2\text{GHz}$, and $V_{DD} = 1.0\text{V}$. Assume A and B are full-swing signals.

Power (Circuit $A - X$):

Power (Circuit $B - Y$):

Problem 3.4 (**2 points**) **Receiver**. What type of circuit is the three-transistor sequential element clocked by signal Φ, which is used as a receiver in the circuits of Figure 2?

Problem 3.5 (**3 points**) **Static or Leakage Power**. Which circuit, $A - X$ or $B - Y$, is likely to dissipate more static or leakage power in the receiver and why?