EEC 216 Lecture #8: Energy Recovery Circuits

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Outline

• Announcements
• Wrap Up: Low Power Interconnect
• Review: Energy Dissipation
• Adiabatic Charging
• Energy Recovery Circuit Basics
• Dynamic Energy Recovery Logic
• Power and Clock Waveform Generation
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CMOS Inverter Down Converter

- Drive input from rail-to-rail
- Output goes from VDDDL to Gnd
Cross Coupled Pullup Up Converter
Stepwise Charging

\[ \Phi_{N-1} \]
\[ C_T \]
\[ V_{N-1} \]
\[ + \]
\[ - \]
\[ \Phi_1 \]
\[ C_T \]
\[ V_1 \]
\[ + \]
\[ - \]
\[ \Phi_0 \]
\[ C_T \]
\[ V_0 \]
\[ + \]
\[ - \]
\[ \Phi_{GND} \]
\[ \text{Out} \]
Data-Dependent Swing Bus Circuit

- Hiraki, JSSC 95
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Low-to-High Transition Equivalent Circuit

\[ V_{DD} \]
\[ i_{VDD} \]
\[ v_{out} \]
\[ C_L \]
Energy Drawn From Power Supply

\[ E_{VDD} = \int_{0}^{\infty} P_{VDD}(t) dt = \int_{0}^{\infty} i_{VDD}(t) V_{DD} dt \]

\[ = V_{DD} \int_{0}^{\infty} C_L \frac{dv_{out}}{dt} dt = C_L V_{DD} V_{DD} \int_{0}^{V_{DD}} dv_{out} \]

\[ = C_L V_{DD}^2 \]
Energy Stored on Load Capacitor

\[ E_C = \int_{0}^{\infty} i_{VDD}(t)v_{out} \, dt \]

\[ = \int_{0}^{\infty} C_L \frac{dv_{out}}{dt} v_{out} \, dt = C_L \int_{0}^{V_{DD}} v_{out} \, dv_{out} \]

\[ = \frac{1}{2} C_L V_{DD}^2 \]

- Compared to \( E_{VDD} \), we see that \( \frac{C_L V_{DD}^2}{2} \) dissipated
- Same amount dissipated when capacitor discharged
- Independent of MOSFET resistance
Can We Do Better on Energy?

- Seems that $C_L V_{DD}^2$ is pretty fundamental
  - Independent of resistance, circuit delay
- Static CMOS logic basically configures FETs as switches connected to voltage sources
  - Transient determined by capacitor dynamics, $RC_L$
- But, suppose we use a current source to charge the capacitor instead…
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Principle of Adiabatic Charging

\[ E_{IDD} = \int_{0}^{\infty} i_{DD}(t) v_{IDD}(t) \, dt \]

- By controlling the current, we can control the voltage developed across the resistor, and reduce power consumption by charging slowly.
Adiabatic Charging Analysis

\[ \Phi = RC \left( \frac{dV_c}{dt} \right) + V_c \]

- Solve differential equation assuming input is ramp with duration T
Input Voltage Equation

\[ \Phi(t) = \begin{cases} 
0 & t < 0 \\
\frac{V_{DD}}{T} t & 0 \leq t < T \\
V_{DD} & t \geq T
\end{cases} \]

- \( \Phi(t) \) ideal linear voltage ramp ending in VDD steady-state voltage
- Later: how to implement \( \Phi(t) \) impacts energy dissipation and limits energy recovery efficiency
Output Voltage Solution

\[ V_c(t) = \begin{cases} 
0 & t < 0 \\
\Phi - \frac{RC}{T} V_{DD} \left(1 - e^{-t/RC}\right) & 0 \leq t < T \\
\Phi - \frac{RC}{T} V_{DD} \left(1 - e^{-T/RC}\right)e^{-(t-T)/RC} & t \geq T 
\end{cases} \]

- Solve for instantaneous resistor power using \( V_c(t) \)
- Integrate to find dissipated energy as function of \( T \)
Energy Dissipated With Ramp Driver

\[ E_{\text{diss}} = \int_{0}^{\infty} i_R(t) V_R(t) \, dt = \int_{0}^{\infty} \frac{(\Phi - V_c(t))^2}{R} \, dt \]

\[ = \int_{0}^{T} \frac{(\Phi - V_c(t))^2}{R} \, dt + \int_{T}^{\infty} \frac{(\Phi - V_c(t))^2}{R} \, dt \]

\[ = \frac{RC}{T} CV_{DD}^2 \left[ 1 - \frac{RC}{T} + \frac{RC}{T} e^{-T/RC} \right] \]

- Consider the extreme cases of \( RC \) with respect to \( T \)
Limiting Cases of Slow and Fast Ramps

• For very slow ramp $T \gg RC$:

$$E_{diss} = \frac{RC}{T} CV_{DD}^2$$

• For very fast ramp $T \ll RC$ (original CMOS case):

$$E_{diss} = \frac{1}{2} CV_{DD}^2$$

• Energy dissipation can be made arbitrarily small by making transition time $T$ arbitrarily long
Example Voltage Ramp: Stepwise Charging

\[ V_{out} \]

\[ V_{N-1} \]

\[ C_T \]

\[ V_1 \]

\[ V_0 \]

\[ C_T \]

\[ \Phi_{N-1} \]

\[ \Phi_N \]

\[ \Phi_1 \]

\[ \Phi_0 \]

\[ \Phi_{GND} \]

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Stepwise Charger Operation

- Basic idea: charge large capacitance in small incremental steps
  - Voltage swing between steps small, so small power dissipation between intermediate voltage levels
  - Falls off quadratically with number of levels $N$
  - $N$ steps required, so total dissipation for entire transition goes as $1 / N$

\[
P = f C_L \sum_{k=1}^{N} \left( \frac{V_{DD}}{N} \right)^2
\]

\[
= C_L \frac{V_{DD}^2}{N} f
\]
Adiabatic Switching Intuition

• **Power dissipated when current flows across potential (voltage difference)**
  – Voltage difference between nodes kept small, so small power dissipation as node transitions
  – Slow voltage transition on capacitor implies low currents flowing, so low voltages developed on parasitic resistances

• **Inherent energy and speed tradeoff**
  – Long transitions imply slower operation but less energy dissipation
  – Independent of supply scaling unlike dynamic power for traditional CMOS circuits
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Energy Recovery Basics

• Energy stored by placing charge on capacitive circuit nodes
  – Would like to recover that energy and return it to power supply for use again
  – Adiabatic charging and discharging minimizes losses as charge moved to and from power supply

• Energy recovery vs. adiabatic charging
  – Terms sometimes confused in literature
  – Adiabatic charging refers to slow (thermodynamically reversible) movement of charge across vanishingly small voltages for minimal power dissipation
  – Energy (charge) recovery means moving charge back and forth from a power supply or charge reservoir
Energy Recovery Process

\[ \Phi(t) \]

\[ i_c \]

\[ v_{out} \]

\[ C_L \]
Energy Recovery Timing Phases

- Similar to dynamic logic or level sensitive (latch-based) clocking, except power supply is also the clock signal
- Four phases of operation
  - *Idle Phase*: \((\Phi = 0)\) Circuit state before evaluation
  - *Evaluation Phase*: \((\Phi\) transitions from 0 V to \(V_{DD}\)) Circuit nodes evaluate to final value
  - *Hold Phase*: \((\Phi = V_{DD})\) Circuit nodes maintain state after evaluation
  - *Restoration Phase*: \((\Phi\) transitions from \(V_{DD}\) to 0 V) Circuit nodes restored to initial value
Energy Recovery Process Timing

- Want output voltage to transition slowly with power/clock waveform
- How do we cascade logic stages?

\[
\Phi(t)
\]

\[
V_{out}
\]
Cascaded Logic Energy Recovery Timing

- Charge \( n \)th stage nodes and then discharge \( (n-1) \)th stage nodes
- How do we implement the energy recovery phase?
Cascaded Logic Timing Issues

• **Must isolate input from output node**
  – Otherwise inputs cannot change until output has been sampled by succeeding stage
  – Constraint ripples to end of logic pipeline, i.e. no input can change until final stage evaluates

• **Isolation requires an alternative path (?) Box) for reverse current flow for energy recovery**
  – Reverse path must be controlled by gate output
  – If \( y_0 = 1 \), then must discharge \( y_0 \) slowly using \( \Phi_0 \) (returning charge to power supply)
  – If \( y_0 = 0 \), reverse path must be open circuit to prevent leakage from \( \Phi_0 \) contaminating output \( y_0 \)
Self-Controlled Energy Recovery

\( \Phi_0 \quad \Phi_1 \)

\( x \quad \bar{P}_0 \quad P_0 \quad y_0 \quad M_0 \quad \bar{P}_1 \quad P_1 \quad y_1 \)
Self-Controlled Recovery Issues

• Use full transmission gates to isolate outputs

• Diode connect FETs between output and clock / power node provide reverse current path for energy recovery
  – Simple to implement with low area overhead
  – Control signal varying with output voltage transition
  – Requires $V_{TH}$ voltage drop to forward bias diode M0, increasing power dissipation

• Would like recovery path control signal to maintain state throughout restoration phase

• Alternative: use succeeding stage output to compute control
Next Stage Controlled Energy Recovery

\[ F_0 \xrightarrow{x} F_1 \xrightarrow{y_0} F_1^{-1} \xrightarrow{y_1} \]

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Next Stage Controlled Recovery Issues

• Control signal for energy recovery path generated from succeeding stage output
  – Requires computing inverse function of nth stage to reproduce state of (n-1)th stage output
  – Full pass gate isolation means that control signal held constant during full restoration phase transition

• Overhead for this logic style can be high
  – Computing inverse could be even more area intensive than computing desired function

• True physically and logically reversible computation
  – Pass gate reverse current path has little loss, adiabatic transition
  – Style results in minimum overall energy dissipation
Example: Split-Level Charge Recovery Logic

- Younis 1994

- Uses rails which split up and down from half $V_{DD}$ rather than single rail ramping from 0V to $V_{DD}$

- Can use many clock phases to build pipeline
Energy Recovery System Block Diagram

- Use circuits to generate power / clock waveforms
- Generators must use as little power as possible
  - Resonant RLC circuits often used in these applications
  - Minimize parasitic losses in power / clock generator
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Dynamic CMOS Two-Input NAND Gate

- PMOS precharges (Clk low), NMOS evaluates (Clk high)
Adiabatic Dynamic Logic (ADL) Inverter

- Precharge Phase: $\Phi 0$ is long voltage ramp from 0V to $V_{DD}$ charging $V_{out}$ to $V_{DD} - V_{diode}$
- Evaluate Phase: $\Phi 0$ swings slowly low, discharging if input is high otherwise leaving output high
Cascading Adiabatic Dynamic Logic Gates

- Similar to NP-CMOS design style: cascade N-blocks with P-blocks
Adiabatic Dynamic Logic Design Issues

• Clocking methodology similar to all adiabatic designs: four phases required
  – Clocks for consecutive stages must be synchronized such that when the output of first stage is latched (hold phase) the second stage starts evaluate phase
  – When first stage is evaluating, must ensure no non-adiabatic transitions in second stage

• Output voltages must be precharged high (low) enough to guarantee correct operation
  – Reduces to guaranteeing diode drop is significantly less than FET threshold voltage \( V_{\text{diode}} < V_{\text{TH}} \)
  – Alternative is to add DC offset to power / clock voltages to compensate for diode drop
Consecutive stages have opposite clock polarities
- Similar to NP-CMOS dynamic logic clocking

Four phases are actually necessary
- In this example, stage clocked by $\Phi_2$ evaluates while $\Phi_1$ holds and $\Phi_0$ restores

Feedback must occur every four stages for consistent timing (every 4\textsuperscript{th} stage in same phase)
Adiabatic Dynamic Logic NAND2

- Complex ADL gate design similar to dynamic CMOS logic design:
  - Implement arbitrary pulldown network with a diode in parallel
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Supply Clock Generation Goals

• Energy recovery logic requires efficient power / clock waveform generation
  – Should operate with high efficiency (low loss) at high frequency
  – Must create long rise and fall times for adiabatic charging of capacitive circuit nodes
  – Must be able to deliver and receive charge to recover energy

• Stepwise driver incorporates too many losses to satisfy these requirements well

• Most approaches use an RLC resonant circuit
  – Sinusoidal slope approximates linear ramp
  – Energy moved between capacitive nodes and inductor
Basic Resonant Clock Generator

- SW0 closes, $\Phi$ rings up to $V_{DD}$ or down to ground
- MP or MN turns on to hold $\Phi$ at steady state
- $RC$ models clock net, $L$ chosen to set frequency

$V_{DD}/2$ $\rightarrow$ $SW0$ $\rightarrow$ $L$ $\rightarrow$ $MP$ $\rightarrow$ $\Phi$ $\rightarrow$ $R$ $\rightarrow$ $C$ $\rightarrow$ $V_{DD}$

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Problems With Basic Generator

• Series connected switch SW0 has finite resistance
  – Loss dramatically decreases energy efficiency
• Control signals for MP and MN must be generated by extra circuitry
• Additional voltage reference $V_{DD}/2$ required
• Energy dissipated in driving gates of SW0, MP, and MN decreases efficiency
  – Devices must be large to not put too much series resistance in power supply network
• Generates single phase clock
  – Multiple clock phases require multiple generators
Half Blip Circuit Operation

- Alternative topology for a single rail resonant driver
- Eliminates series losses since reset NMOS in parallel
- Athas et al., JSSC 97

Fig. 1. A single-rail resonant clock driver.
Original Blip Circuit

- Transistors MN0 and MN1 restore energy to oscillator dissipated by lossy elements
- Generates two almost nonoverlapping clock phases
- Gates are also driven resonantly by circuit
Full Blip Circuit Operation

- Nonoverlapping clock generation measured traces
- Athas et al., JSSC 97

Fig. 3. Scope trace of the almost-nonoverlapping two-phase clock waveforms of AC-1’s blip circuit.
Blip Circuit Issues

- Nonsinusoidal “blip” waveforms produced since there are no pullup paths
  - Sinusoidal waveform has highest energy recycling efficiency for a resonant circuit
  - Energy recovery is most efficient at fundamental frequency
  - Energy in higher order harmonics almost totally lost

- Two inductors and half $V_{DD}$ reference required for the basic circuit
Blip Circuit Variation 1

- PMOS pullup MP0 used in one branch of circuit
- Generates closer to sinusoidal output for better energy efficiency
- PMOS must be sized larger for same resistance, more loss when driving MP0 gate
Blip Circuit Variation 2

- Pullup and pulldown devices used to restore energy
- Short circuit power an issue when both are on
Other Blip Circuit Variations

• Control PMOS and NMOS gates separately
  – Careful rise and fall time management of control signals improves efficiency, creates mostly sinusoidal output
  – Never on simultaneously so no short circuit power
  – Requires PLL to align control signals properly in time, whereas blip circuit control was fully self-timed
  – Control device gates not driven resonantly so additional power dissipation there

• Other supply clock schemes proposed including using MEMS switches, MEMS resonators, etc.
Mixing Energy Recovery and Standard Logic

• Can apply energy recovery selectively to design
• Most useful for high capacitance nodes like clocks, enables, memory word lines and bit lines, other global signals
• Get some power benefits without overhead of circuit reversibility, especially for simple functions like clocks
• Decreased time for circuit redesign
• Requires careful interfacing between energy recovery and traditional circuit styles to guarantee correct operation
AC-1 Microprocessor Example

- Used energy recovery latches with traditional logic
- Athas et al., JSSC 97
Energy Recovery Logic Summary

• Adiabatic charging and energy recovery can result in asymptotically zero energy dissipation
  – Requires operation to be arbitrarily slow
  – Not all applications amenable to very low frequency operation
• Diode based approaches dissipate more power
  – Finite forward biased diode drops inherently burn power
  – Full transmission gate circuits are better from power perspective
• Leakage power currently limits usefulness
  – Energy recovery techniques apply to dynamic power only, if leakage dominates then not much gain
  – Active research to address these concerns