

EEC 216 Lecture #16: Fundamental Limits of Low Power Design

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Outline

- **Announcements**
- **Limits of Low Power Design**
- **Last Words: Thermodynamics of Computation**

Meindl's Hierarchy of Limits

- **Fundamental limits**
 - Set by laws of thermodynamics, quantum mechanics, and electromagnetism
 - Applicable to any fabrication process
- **Material limits**
 - Determined by semiconductor, interconnect, and dielectric materials
- **Device Limits**
 - Set by device structure, doping profile
- **Circuit Limits**
 - Set by choice of circuit style
- **System Limits**

Theoretical and Practical Limits

- **Theoretical limits**

- Limits can be derived for each category from first principles
- Can lead to unrealistic lower bounds

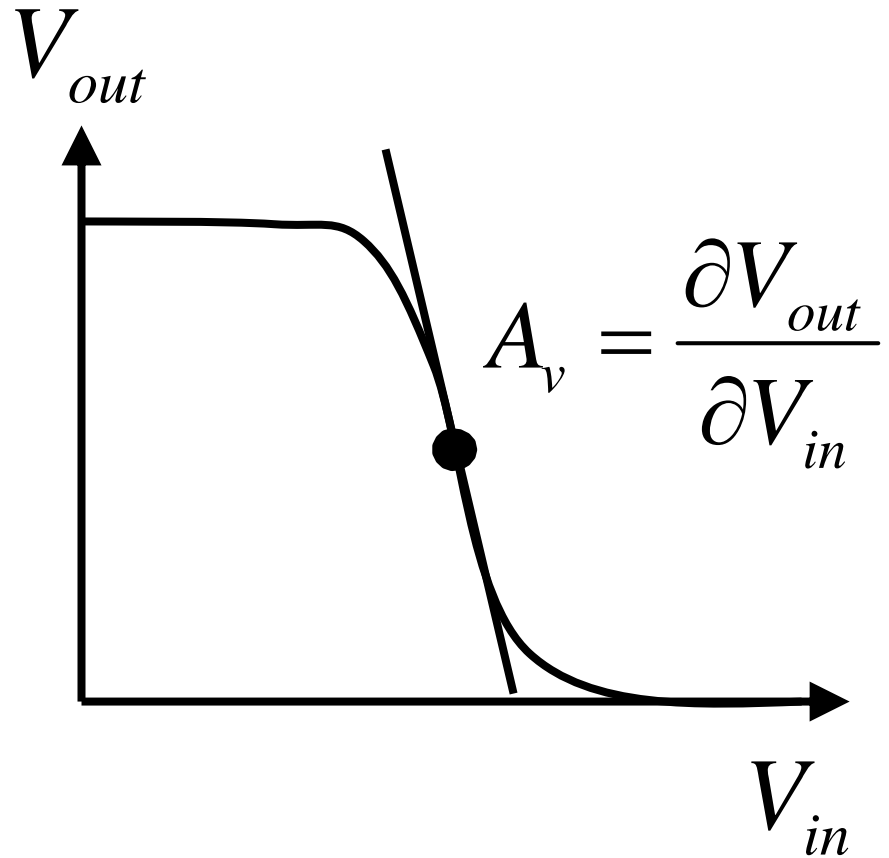
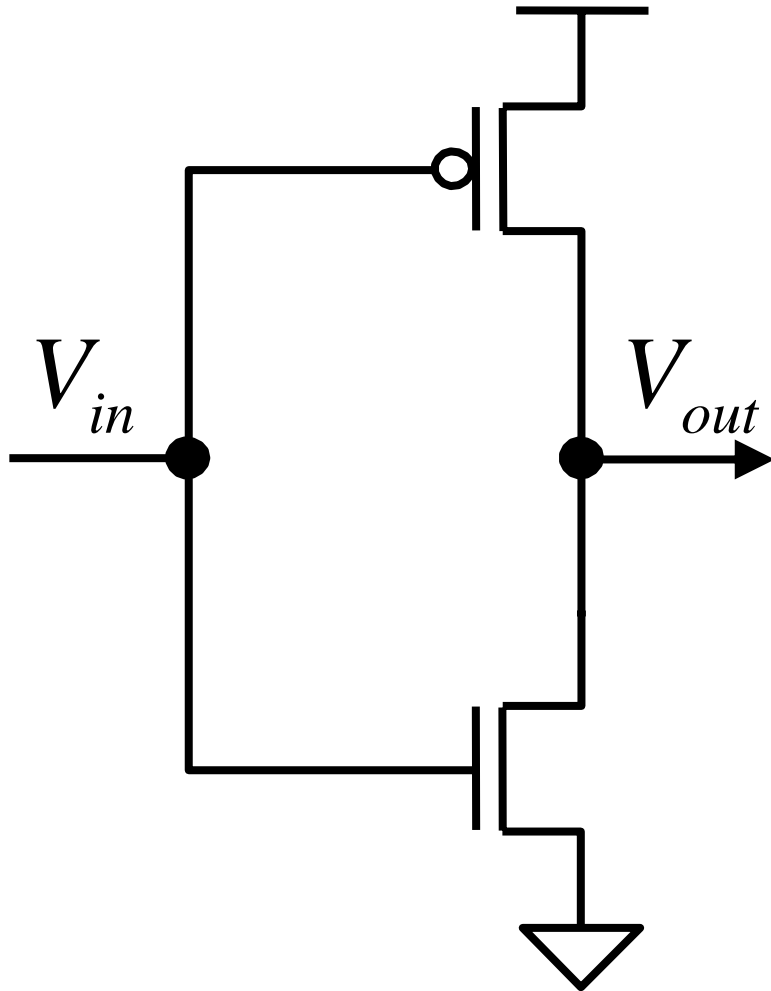
- **Practical limits**

- Cost is determining factor for practicality
- Requiring exotic materials may preclude reaching theoretical limit
- Incorporating design margins to enhance yield and reliability will pressure designs away from hard limits

- **No one really knows above fundamental limits**

- Single electron device, atomic size, in vacuum

CMOS Inverter Gain Example



• Want: $A_v \gg 1$

CMOS Inverter Gain in Weak Inversion

- **Gain at transfer curve midpoint:**

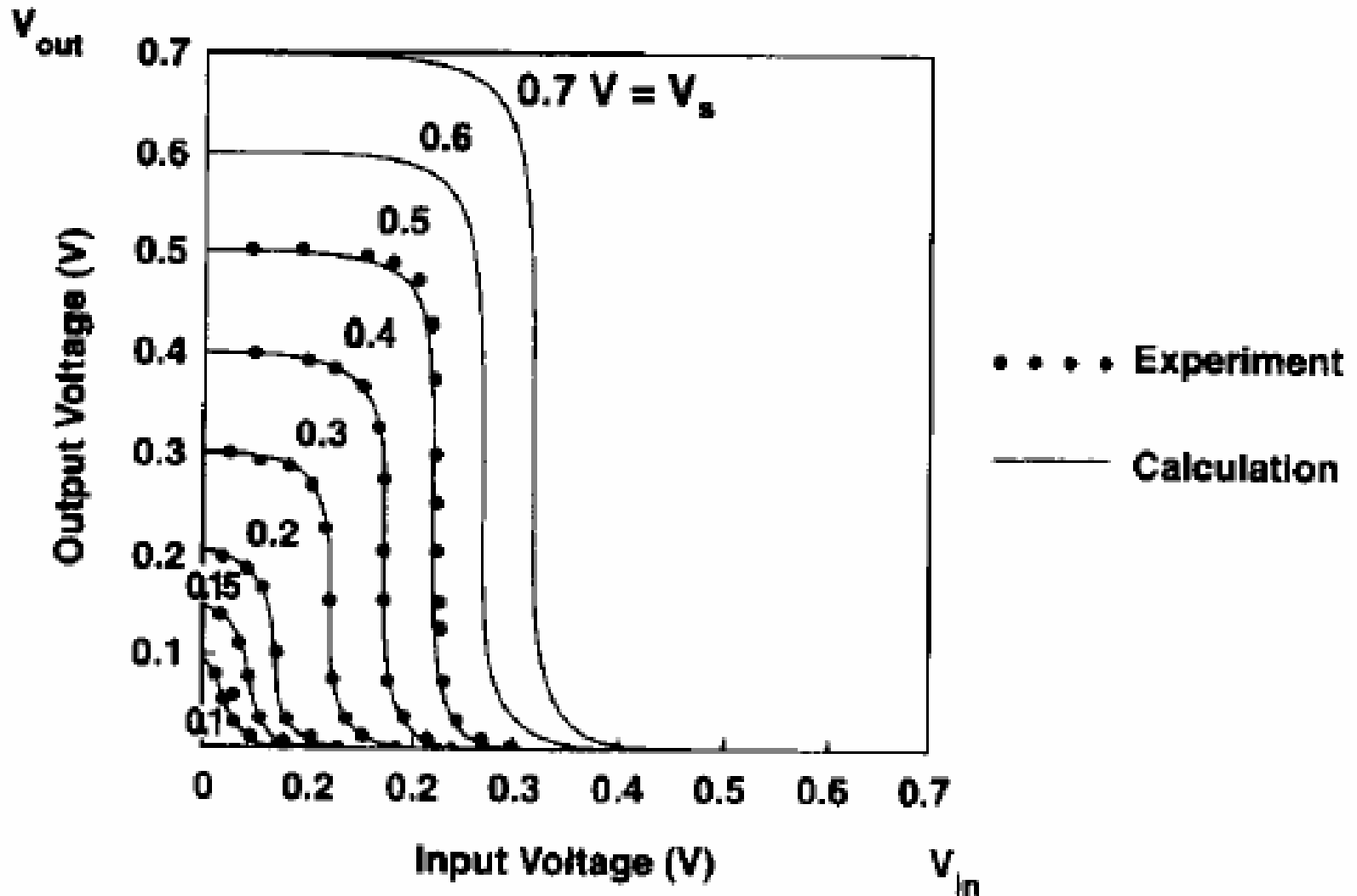
$$A_v = \exp\left(\left[\frac{qV_{DD}}{2kT}\right] - 1\right)$$

- **To satisfy gain much greater than 1:**

$$V_{DD} \geq \frac{4kT}{q}$$

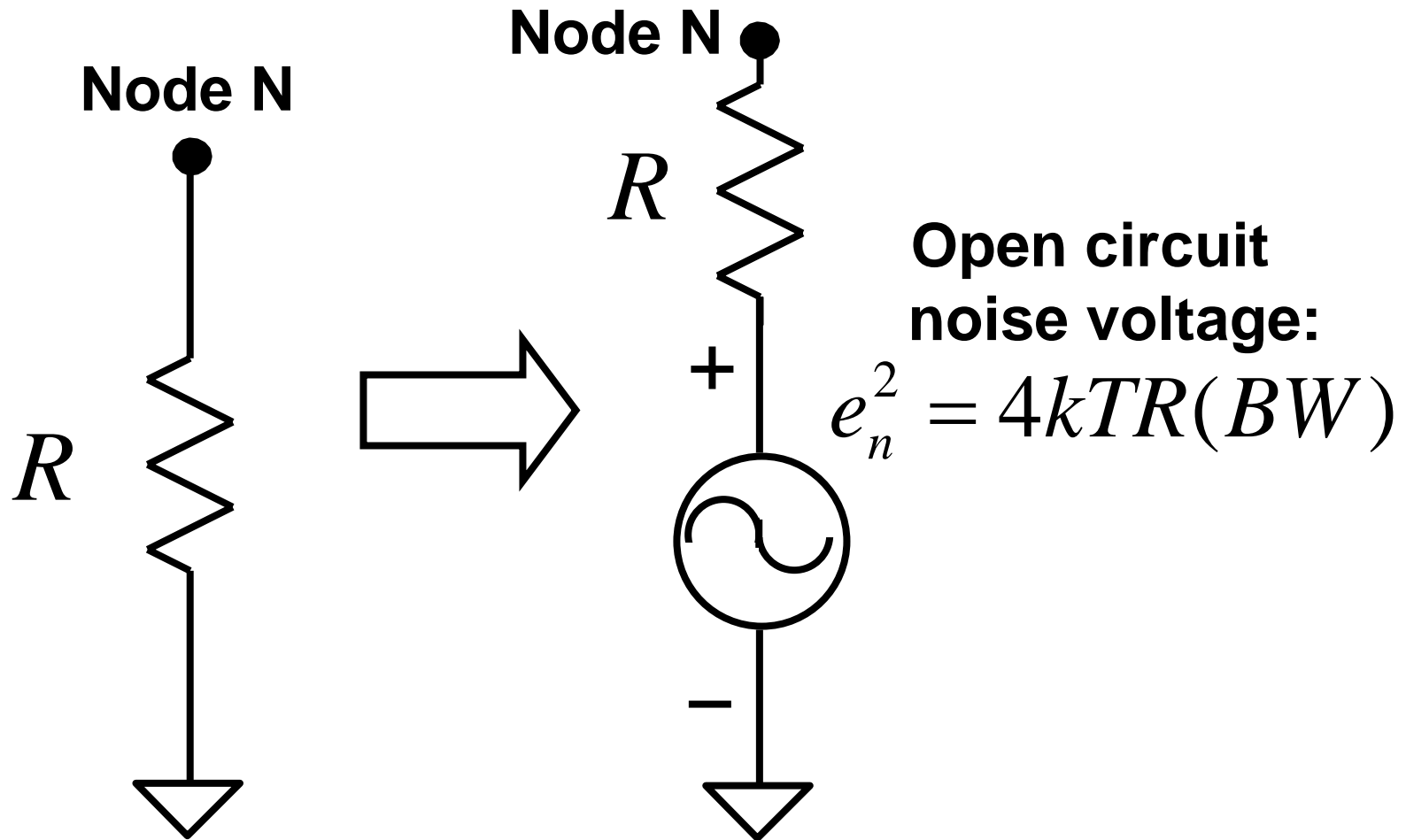
- **At room temperature, minimum supply near 0.1 V**
 - At lower temperatures, can use lower supply voltages

CMOS Inverter Transfer Curves



• V_T 's = 160 mV, Swanson and Meindl 1972

Resistor Thermal Noise



- **k** is Boltzmann's constant, **BW** is node bandwidth

Thermal Noise Limit

- **Noise power available at node N:**

$$P_{noise} = \frac{e_n^2}{R} = kT(BW)$$

- **Signal power must be larger for reliable bit storage at node N:**

$$P_{signal} \geq \gamma P_{noise} = 4P_{noise}$$

- **Switching energy transfer in node N transition:**

$$E_s \geq \gamma kT = 4kT$$

- **Greater energy implies lower BER:**

$$\Pr(error) = \Pr(E_n > E_s) = \exp(-E_s/kT)$$

Thermal Noise Limit Example

- **Assume $\gamma = 4$, $T = 300$ K:**

$$E_s \geq 1.66 \times 10^{-20} \text{ Joules}$$
$$\geq 0.104 \text{ eV}$$

- **Energy required to move a single electron through a potential difference of 100 mV**
 - Applicable in single electron transistor limit, minimum supply voltage likely to be 0.1 V
 - Current energies about 10^6 - 10^7 times as large
 - Translates into very good BER on circuit nodes (at least with respect to thermal noise)

Low Voltage CMOS Inverter Operation

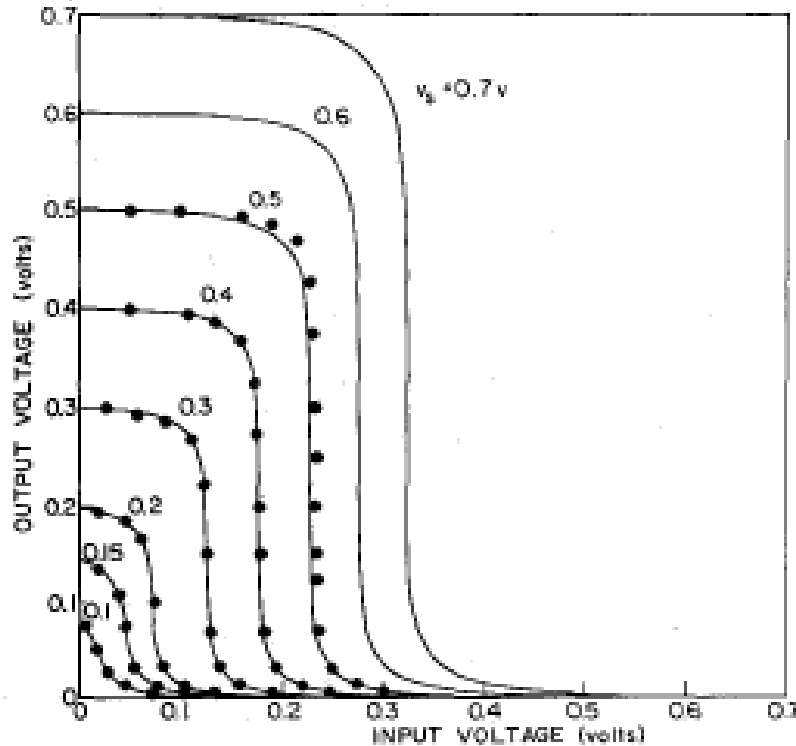


Fig. 9. CMOS inverter transfer characteristics. —experiment; theory (12a).

Swanson and Meindl, JSSC 1972

- Thermal noise limit:

$$\frac{4kT}{q} \approx 100 \text{ mV}$$

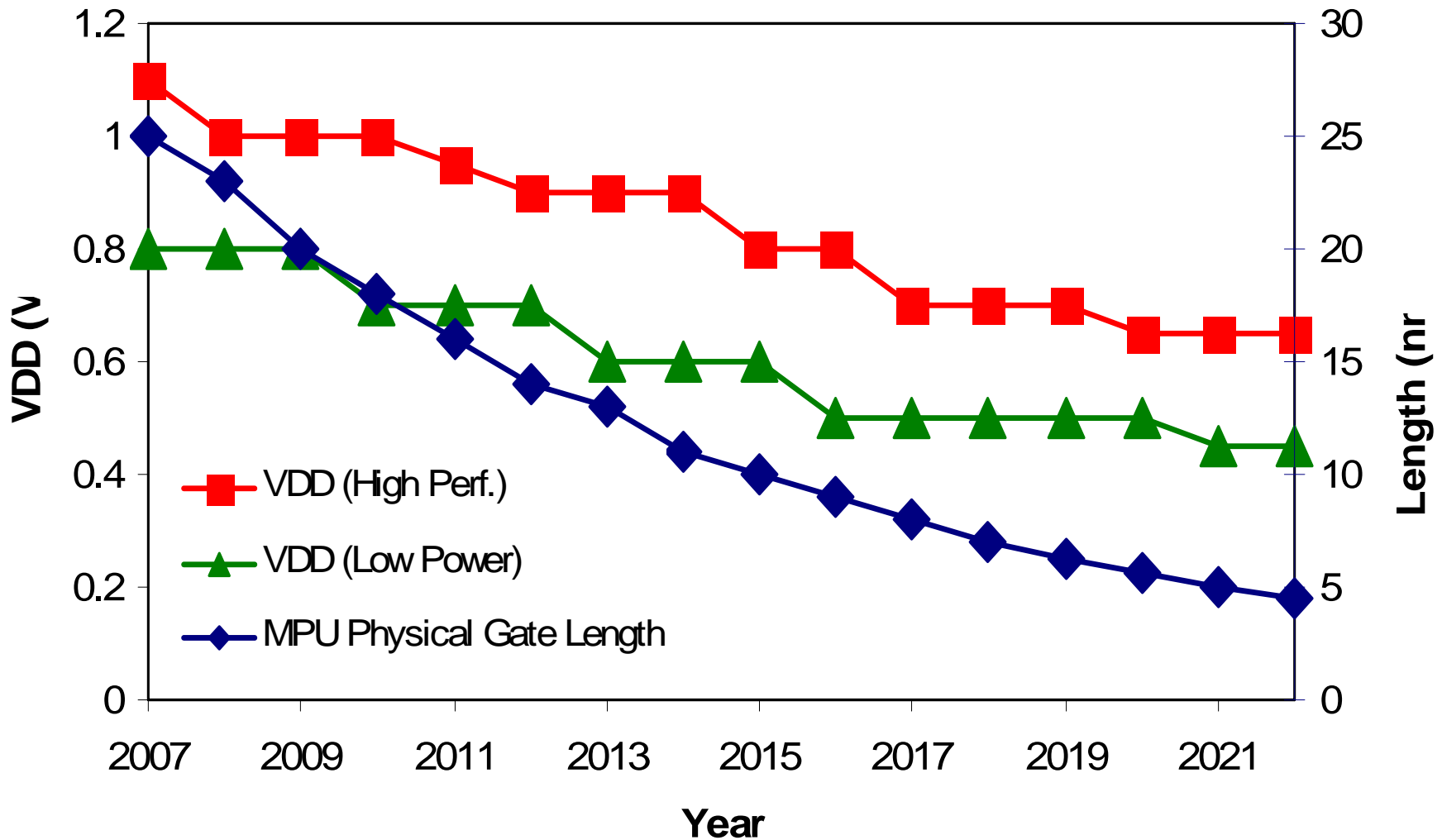
- Inverter gain limit:

$$\frac{8kT}{q} \approx 200 \text{ mV}$$

- Equalized NMOS-PMOS off currents:

$$\frac{2nkT}{q} \approx 57 \text{ mV}$$

Supply Voltage Scaling With Technology Node



- **From 2007 ITRS Roadmap**

Heisenberg Uncertainty Principle Limit

- **Physical measurement associated with a switching transition over time Δt obeys Heisenberg uncertainty principle:**

$$\Delta E \geq h / \Delta t$$

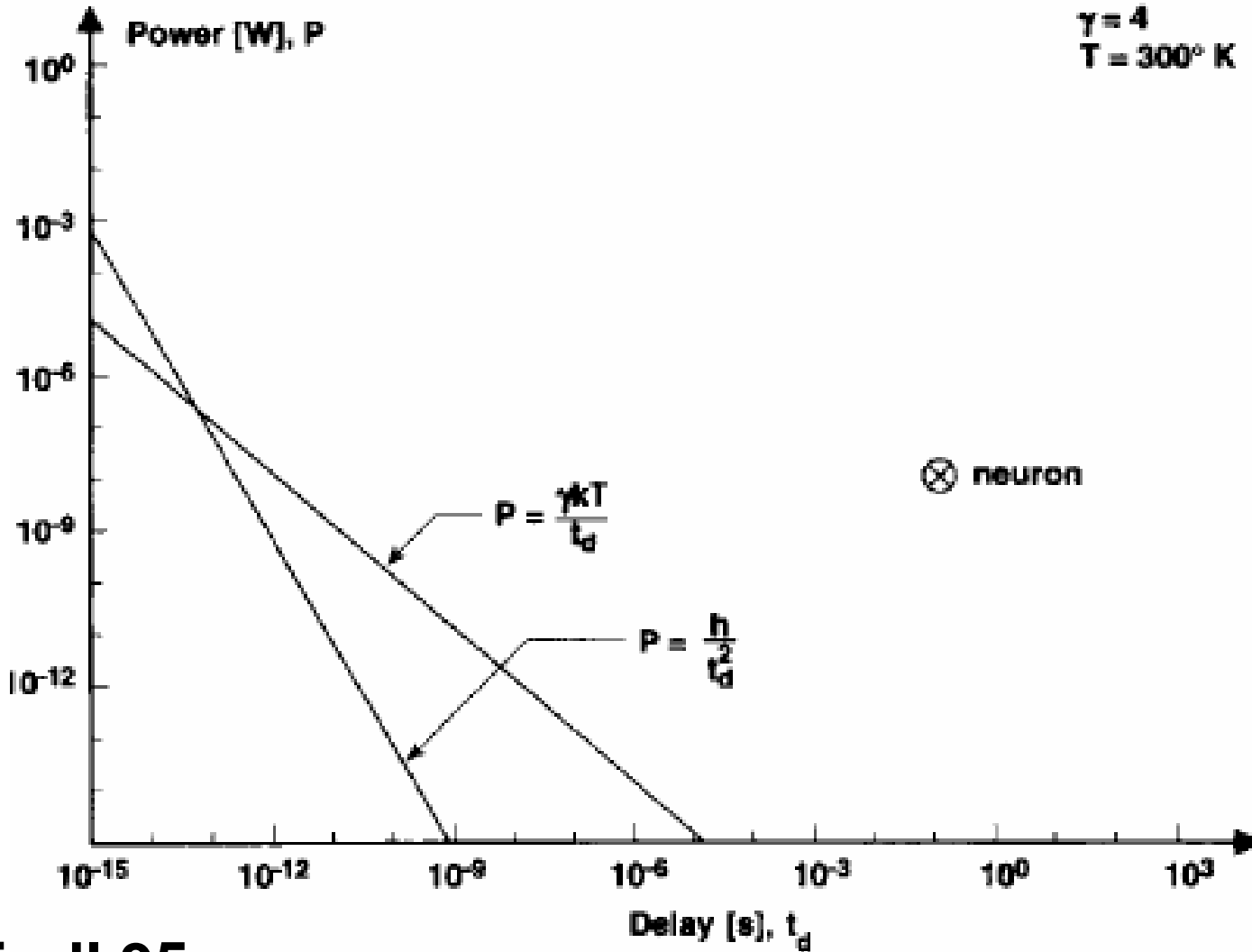
– h is Planck's constant

- **Equivalent power transfer during a switching transition of a single electron wave packet:**

$$P \geq h / (\Delta t)^2$$

- **Both limits refer to rate of energy transfer, not necessarily of energy dissipation**
 - Adiabatic techniques can reduce dissipation

Power Transfer vs. Transition Interval

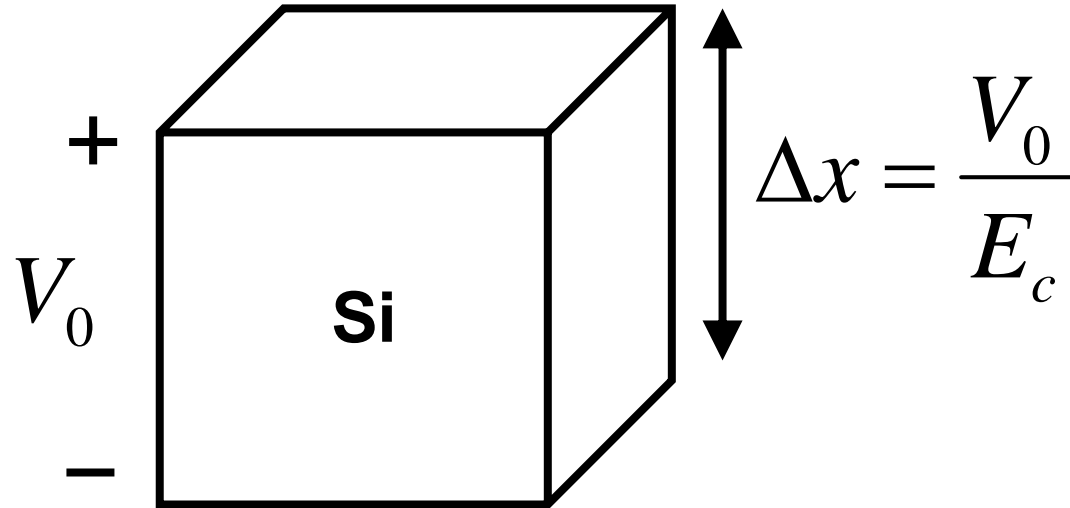


• Meindl 95

Material Limits

- **Semiconductor properties determine key material limits**
 - Carrier mobility μ
 - Carrier saturation velocity v_s
 - Self-ionizing (breakdown) electric field E_c
 - Thermal conductivity K
- **Compare different bulk materials (Si, GaAs, SiGe, carbon nanotubes, etc.)**

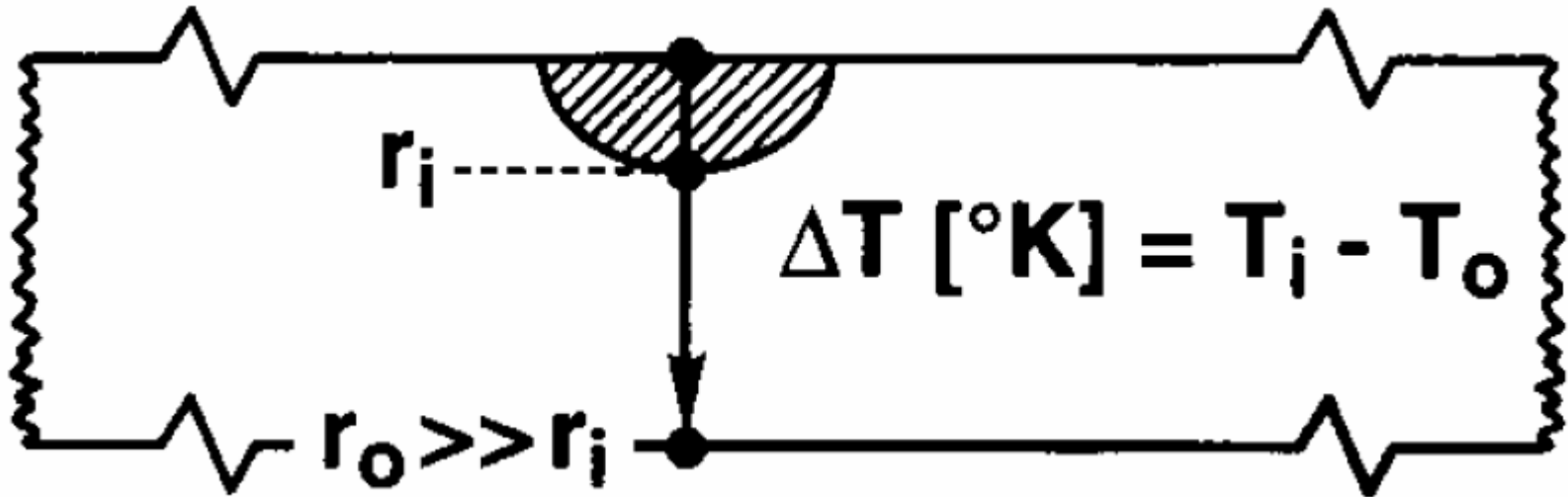
Material Electrostatic Limit



- **Consider cube of undoped silicon in bulk**
 - Limit on maximum energy stored in electric field across material set by self-ionization voltage

$$E = P t_d = \frac{e_{Si} V_0^2}{2 E_c} \quad t_d \geq \frac{V_0}{v_s E_c}$$

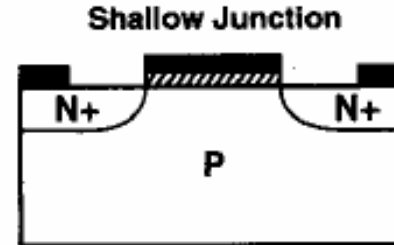
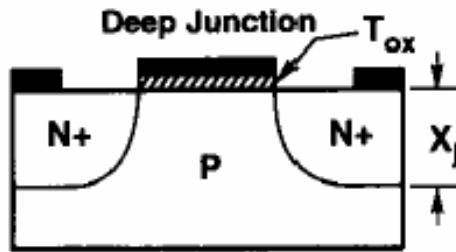
Material Thermal Limit



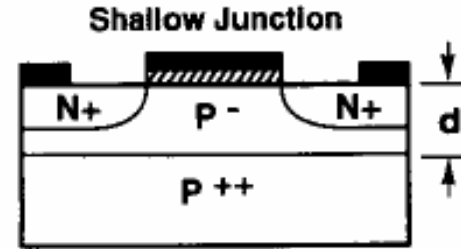
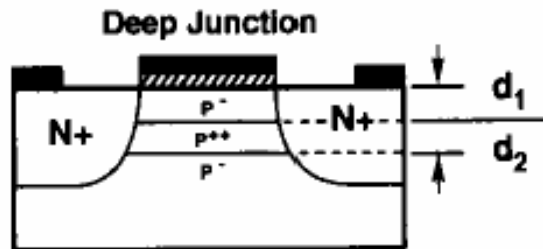
- Meindl 95
- Consider isolated hemispherical device with radius $r_i = v_s t_d / 2$ attached to ideal heat sink at $T = T_o$
- From Fourier's law of heat conduction:

$$P = \pi K v_s \Delta T t_d$$

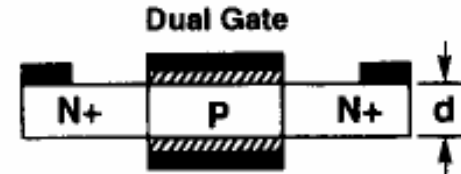
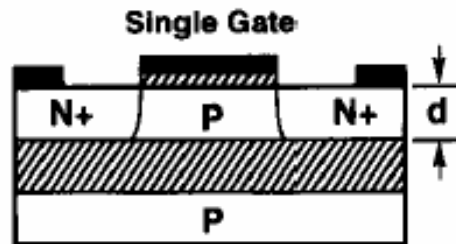
Various MOSFET Structures



Low Impurity Channel Bulk MOSFET



SOI MOSFET



• Meindl 95

Device Energy Limit

- **Minimum energy limit suggested by minimum channel length L_m for MOSFET**

$$E = P t_d = \frac{C_0 L_m^2 V_0^2}{2}$$

- **C_0 is unit area gate capacitance, V_0 is minimum power supply voltage**
- **FETs using spacer gate fabrication techniques have been demonstrated below 10 nm**
 - Other novel structures under development
- **Delay determined by channel length and velocity saturated carrier mobility**

Conclusions

- **Hierarchy of limits set by a variety of considerations**
 - Fundamental limits form loose lower bound on any type of physical implementation
- **Thermodynamics of computation**
 - Can analyze computation in a thermodynamic (energy, entropy) context
 - Bit erasure requires work and energy dissipation
 - Reversible thermodynamic process provides ultimate energy efficient computation
 - Implications for quantum computing

EEC 216 Course Objectives

- **To develop an understanding of power dissipation in modern digital integrated circuits, including the power implications of state-of-the-art architectural and circuit techniques**
- **To learn architectural and circuit design techniques to decrease power consumption at a fixed performance or trade power for performance**
- **To develop an understanding of issues related to power delivery and heat removal in electronic systems, including basic power electronics design and thermal system analysis**