

# EEC 216 Winter 2009 Midterm

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Name: *Solutions*

**Instructions:** This test consists of 4 problems and 15 pages, including the cover sheet. Please make sure that you have all of them. You are allowed one sheet of  $8\frac{1}{2}$  by 11 paper with writing on both sides and a calculator. State any assumptions you make and show complete work to receive credit. The time limit is 80 minutes. The problems are weighted as shown below:

**Grading:**

Problem	Maximum	Score
1	36	
2	19	
3	10	
4	15	
Total	80	

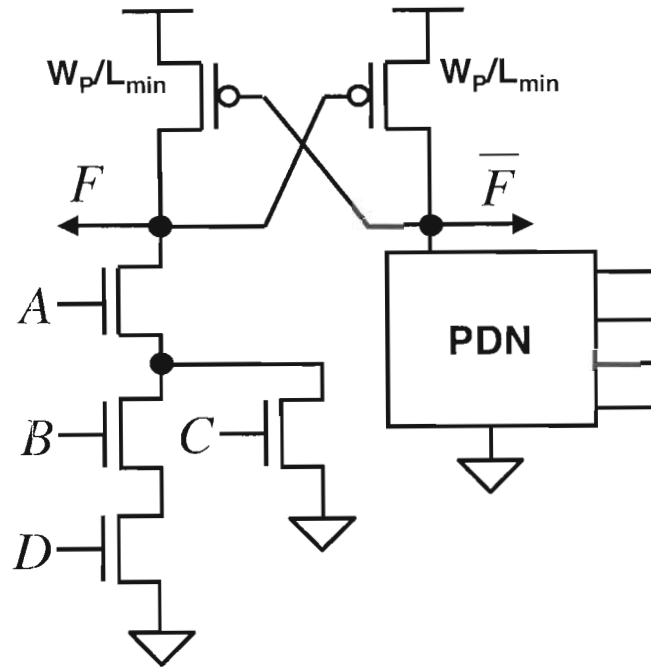


Figure 1: DCVSL gate. Transistor sizes are labeled in the figure.

## 1 Logic Design

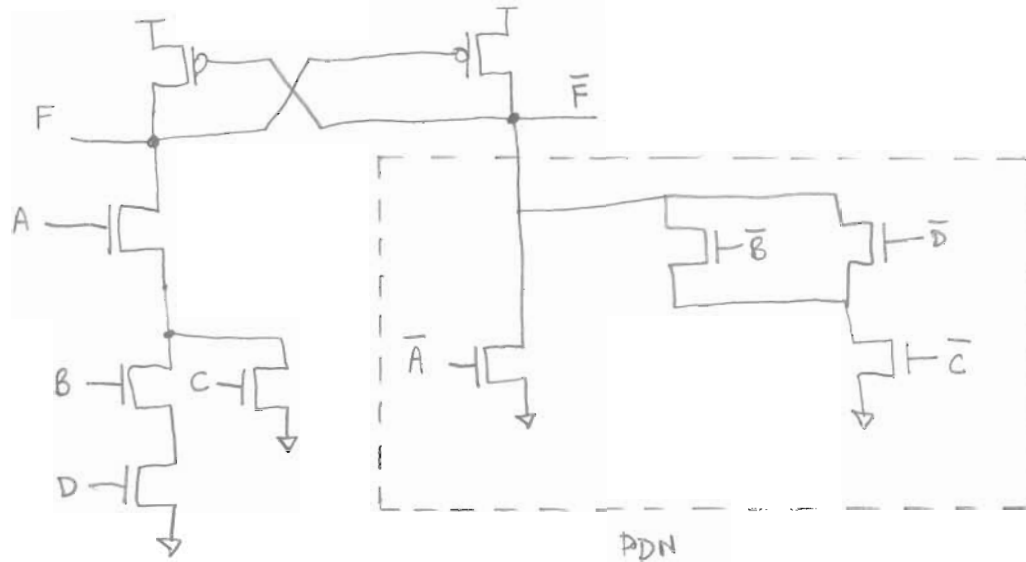
For this exam, use the transistor parameters in Table 1. Assume all dimensions are in microns unless otherwise specified.

Parameter	NMOS	PMOS
$V_t$	0.3 V	-0.3 V
$k' = \mu C_{ox}$	$300 \mu\text{A}/\text{V}^2$	$100 \mu\text{A}/\text{V}^2$
$W_{min}$	$2 \mu\text{m}$	$2 \mu\text{m}$
$L_{min}$	$1 \mu\text{m}$	$1 \mu\text{m}$

Table 1: Problem 1 Transistor Parameters.

**Problem 1.1 (4 points) Pulldown Network Design.** Design the pulldown network for the complementary side of the DCVSL gate shown in Figure 1. Assume that the complements of the four inputs ( $\bar{A}$ ,  $\bar{B}$ ,  $\bar{C}$ , and  $\bar{D}$ ) are available in addition to the true version of the inputs. Be sure to label all inputs clearly.

Problem 1.1 (cont.)



(other solutions possible ...)

**Problem 1.2 (10 points) Activity Factors.** Assume that  $A$ ,  $B$ ,  $C$ , and  $D$  are independent, identically distributed binary random variables, where the likelihood of any individual variable being 1 or 0 is the same. Find the activity factors  $\alpha_{0 \rightarrow 1}$  for the outputs  $F$  and  $\bar{F}$  in your circuit above.

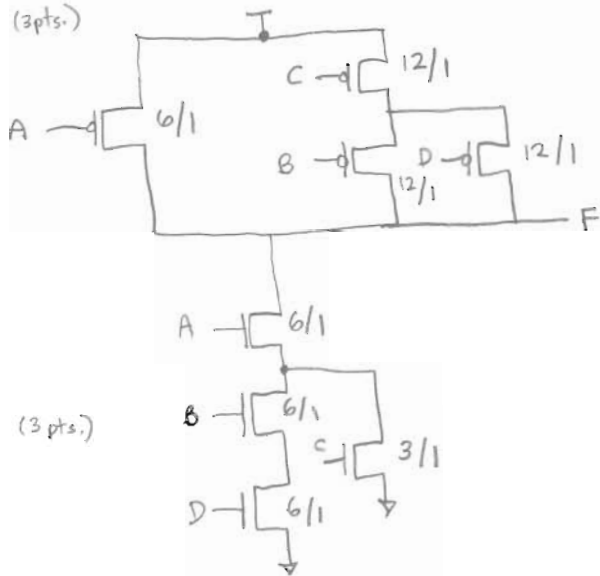
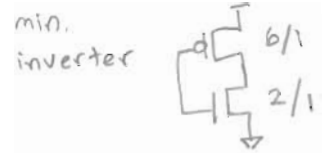
A	B	C	D	F	$\bar{F}$
0	x	x	x	1	0
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	0	1

(6 pts.)

$$F: \alpha_{0 \rightarrow 1} = P_0 \cdot P_1 = \left(\frac{5}{16}\right) \left(\frac{11}{16}\right) = \frac{55}{256} = \boxed{0.215} \quad (2 \text{ pts.})$$

$$\bar{F}: \alpha_{0 \rightarrow 1} = P_0 \cdot P_1 = \left(\frac{11}{16}\right) \left(\frac{5}{16}\right) = \boxed{0.215} \quad \underline{\text{same}} \quad (2 \text{ pts.})$$

**Problem 1.3 (6 points) Static CMOS.** Draw a transistor-level schematic for a static CMOS circuit which implements the logical expression for  $F$  using a single 4-input gate. Implement the circuit using a minimum number of transistors.

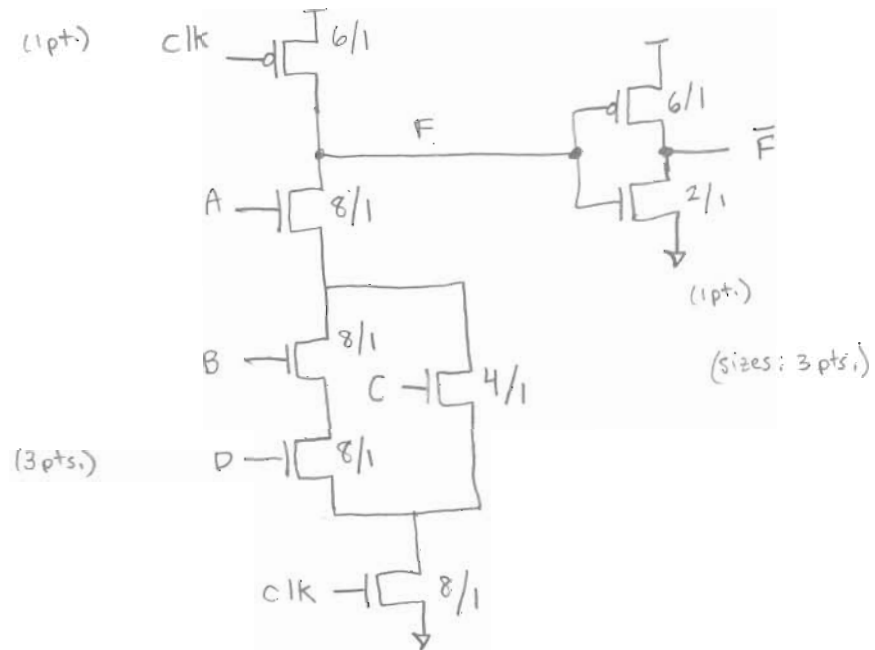


(other solutions possible...)

Sizes in  $\mu\text{m}$ .

**Problem 1.4 (4 points) Static CMOS Sizing.** Size the transistors in the circuit you designed for Problem 1.3 such that the worst case rise and fall times are equal to a minimum-sized inverter (with equal rise and fall times) while minimizing the input capacitance to the logic gate. Label the sizes in your schematic for Problem 1.3. (0.5 pt. each)

**Problem 1.5 (8 points) Dynamic (Domino) Circuit Design.** Design a dynamic gate to implement  $\overline{F}$ . Size the transistors such that the worst case rise and fall times on the dynamic node are equal to a minimum-sized inverter rise and fall time (assume the minimum-sized inverter also has equal rise and fall times). Label all transistor sizes in your schematic. Make sure the circuit can be connected correctly to other dynamic logic circuits in the same style.



**Problem 1.6 (4 points) Discussion.** Which of the three circuit styles is most robust (least sensitive) to external noise sources? Which of the three circuits is least robust (most sensitive)? Justify your answers.

Most Robust (circle one):

- DCVSL
  - Differential output (1/2 credit)
- Static CMOS
  - Full swing
  - low-Z output
  - Ratio insensitive

Dynamic (Domino)

Least Robust (circle one):

- DCVSL
  - Ratioed design
- Static CMOS
- Dynamic (Domino)
  - high-Z node noise sensitive
  - Race conditions

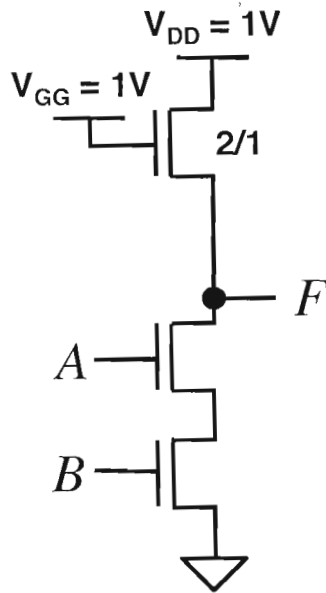


Figure 2: Logic gate. Some transistor  $W/L$  ratios are labeled in the figure.

## 2 Ratioed Circuit Design

**Problem 2.1 (1 point) Circuit Function.** Figure 2 shows a logic circuit which implements one of the two-input logic functions listed below. Circle which one:

AND

NAND

NOR

**Problem 2.2 (4 points) Logic Levels.** Using the transistor parameters in Table 1, assume the pulldown network transistors both have  $W/L = 16/1$ , the voltages on inputs A and B are between  $V_{GG}$  and  $0V$ , and assuming  $V_{GG} = V_{DD} = 1V$ , estimate the output voltage high level ( $V_{OH}$ ) and the output voltage low level ( $V_{OL}$ ).

$$V_{OH} = V_{DD} - V_{T,n} = 1V - 0.3V = \boxed{0.7V} \quad (\text{NMOS pullup}) \quad (2 \text{ pts.})$$

$$V_{OL} = \frac{\frac{1}{\frac{\mu_n (W/L)_{PDN}}{2}} \cdot V_{DD}}{\frac{1}{\frac{\mu_n (W/L)_{PDN}}{2}} + \frac{1}{\mu_n (W/L)_{PU1N}}} = \frac{1/8}{1/8 + 1/2} \cdot V_{DD} = \boxed{0.2V} \quad (2 \text{ pts.})$$

Resistive divider approximation

**Problem 2.3 (4 points) Logic Levels.** Now suppose  $V_{GG} = 1.5V$  and all other conditions are the same as in Problem 2.2. Estimate the output voltage high level ( $V_{OH}$ ) and the output voltage low level ( $V_{OL}$ ).

$$V_{OH} = V_{DD} = \boxed{1V} \quad (V_{GG} - V_{DD}) > V_{T,n} \quad (2 \text{ pts.})$$

$$= 1.5 - 0.3V = \boxed{1.2V} \quad (V_{GG} = V_{DD})$$

$$V_{OL} = \boxed{0.2V} \quad \text{Same as above if } V_{GG} \text{ applied to all inputs.} \quad (2 \text{ pts.})$$

$$= \boxed{10.3V} \quad (V_{GG} = V_{DD})$$

**Problem 2.4 (8 points) Circuit Sizing.** Using the transistor parameters in Table 1, the pullup sizing in Figure 2, assuming  $V_{GG} = 1.2V$ ,  $V_{DD} = 1V$ , and the voltages on inputs  $A$  and  $B$  are between  $V_{DD}$  and  $0V$ , find the smallest  $W/L$  ratios for the pulldown transistors which result in a valid low output that satisfies  $V_{OL} \leq 0.1V_{DD}$ . Solve exactly for  $W/L$ .

PUN current:  $V_G = V_{GG} = 1.2V$   $V_S = V_{OL} = 0.1V_{DD} = 0.1V$   
 (3 pts.)  $V_D = V_{DD} = 1.0V$   $V_{GS} = 1.1V$ ,  $V_{GS} - V_{T,n} = 0.8V < V_{DS} = 0.9V$  sat

$$I_{PUN} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)_{PUN} (V_{GS} - V_{T,n})^2 = \frac{300 \mu A/V^2}{2} \left(\frac{2}{1}\right) (0.8V)^2$$

$$= 192 \mu A$$

PDN current:  $V_G = V_{DD}$ ,  $V_S = 0V$ ,  $V_D = V_{OL} = 0.1V$ ,  $V_{GS} - V_{T,n} = 0.7V > V_{DS} = 0.1V$  linear  
 (4 pts.)

$$I_{PDN} = \mu_n C_{ox} \left(\frac{W}{L}\right)_{PDN} \left[ (V_{GS} - V_{T,n})V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$= \frac{300 \mu A}{V^2} \left(\frac{W}{L}\right)_{PDN} \cdot \frac{1}{2} \left[ (0.7V)(0.1V) - \frac{(0.1V)^2}{2} \right] = 9.75 \mu A \left(\frac{W}{L}\right)_{PDN}$$

↑  
series

$$\left(\frac{W}{L}\right)_{PDN} = \frac{I_{PUN}}{9.75 \mu A} = 19.7 \approx \boxed{20} \quad (1 \text{ pt.})$$

Various approximations get partial credit.

**Problem 2.5 (2 points) Static Power "Activity" Factor.** Assume inputs  $A$  and  $B$  are independent, identically distributed, binary random variables with equal probability of being a 0 or a 1. What percentage of time does the circuit in Figure 2 dissipate static power? Justify your answer.

Static power when output low:  $A=B=1$

$$Pr(F=0) = P_A \cdot P_B = \frac{1}{4} \quad \boxed{25\%}$$

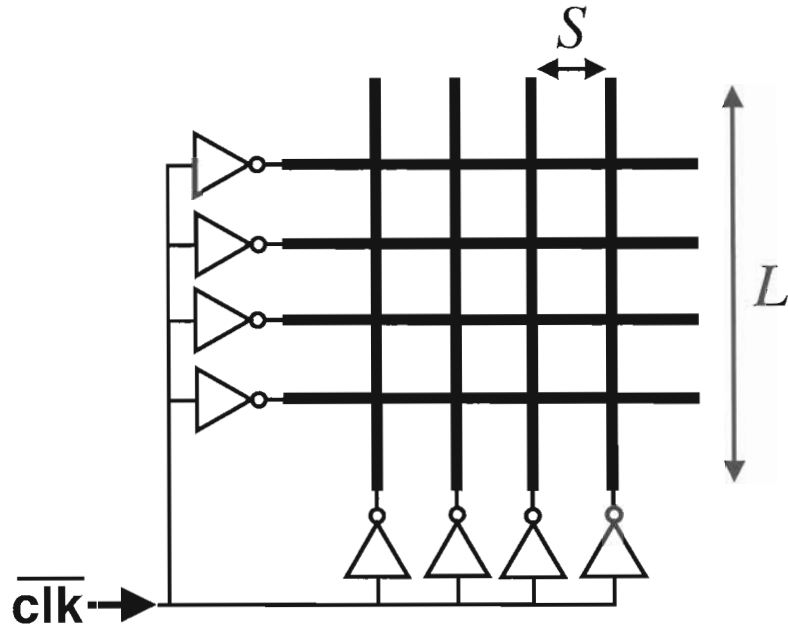


Figure 3: Final inverter stage for driving clock grid with wires of length  $L$ .

### 3 Clock Grid

Parameter	Metal 2
Sheet Resistance ( $R_{sq.}$ )	$0.1 \Omega/sq.$
Spacing ( $S$ )	4 mm
Thickness ( $T$ )	$0.1 \mu\text{m}$
Height ( $H$ , above substrate)	200 nm
Dielectric Constant ( $\epsilon_r$ )	$4.3 \times 8.85e-12 \text{ F/m}$
Length ( $L$ , on figure)	2.0 cm
Width ( $W$ )	$2.0 \mu\text{m}$

Table 2: Problem 2 Interconnect Parameters.

Figure 3 shows the final (parallel) inverter stage for driving a clock grid of long wires of length  $L$  running horizontally and vertically and shorted together at the intersections. Assume the transistor parameters listed in Table 1 and the wire dimensions and parameters shown in Figure 3 and listed in Table 2. Also assume  $V_{DD} = 1.0\text{V}$ .

**Problem 3.1 (2 points) Wire Capacitance: No Coupling.** Calculate the total capacitance for the clock grid. Ignore any contribution of fringing fields or coupling capacitance. You may assume that any intersection of wires makes a negligible difference to the total capacitance.

$$C_{\text{TOT}} = 8 \cdot \epsilon_r \frac{WL}{h} = 8 \cdot 4.3 \cdot (8.85 \times 10^{-12} \text{ F/m}) \frac{(2 \times 10^{-6} \text{ m})(2 \times 10^{-2} \text{ m})}{200 \times 10^{-9} \text{ m}} \quad (1 \text{ pt.})$$

$$= \boxed{60.9 \text{ pF}} \quad (1 \text{ pt.})$$

**Problem 3.2 (2 points) Wire Capacitance: Including Coupling.** Suppose there is 50 fF of coupling capacitance for each mm of distance that adjacent wires travel (i.e., 50 fF/mm coupling capacitance between adjacent wires) in the clock grid. Calculate the new total capacitance for the clock grid. You may assume that any intersection of wires makes a negligible difference to the total capacitance.

3 coupling caps for vertical wires + 3 for horizontal (1 pt.)

$$C_{\text{COUP}} = (3+3) (50 \text{ fF/mm}) (20 \text{ mm}) = 6 \text{ pF} \quad (1 \text{ pt.})$$

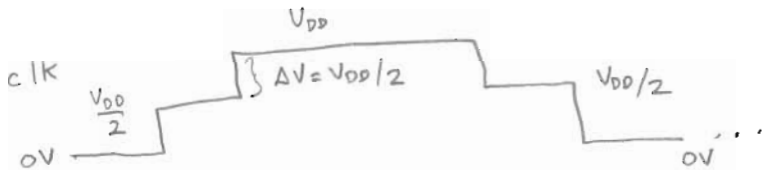
$$C_{\text{TOT}} = \boxed{66.9 \text{ pF}}$$

**Problem 3.3 (3 points) Dynamic Power.** Compute the dynamic power of driving the clock grid, assuming the capacitance you found in Problem 3.1, and assuming  $f = 2\text{GHz}$ , and  $V_{DD} = 1.0\text{V}$ .

$$P = \alpha C V_{DD}^2 f = (1)(60.9 \text{ pF})(1 \text{ V})^2 (2 \text{ GHz}) = \boxed{121.8 \text{ mW}} \quad (1 \text{ pt.})$$

(2 pts.)

**Problem 3.4 (3 points) Dynamic Power: Stepwise Driver.** Suppose the inverters in Figure 3 are replaced by stepwise drivers which first charge the clock grid to  $V_{DD}/2$  and then  $V_{DD}$  on a rising transition and then reverse this sequence on the falling transition. What is the new dynamic power assuming the capacitance you found in Problem 3.1?



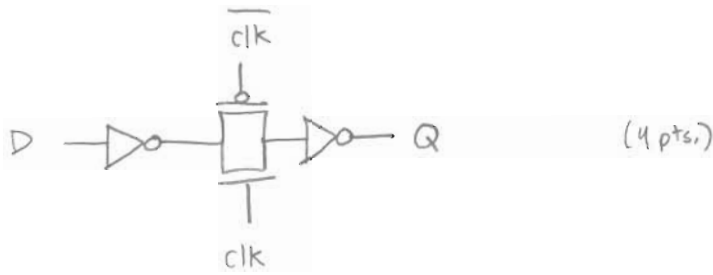
$$P_{\text{dyn}} = 2 \cdot C (\Delta V)^2 f \alpha = 2 \cdot (60.9 \text{ pF}) (0.5 \text{ V})^2 (2 \text{ GHz}) (1) \quad (2 \text{ pts.})$$

$$= \boxed{60.9 \text{ mW}} \quad (1 \text{ pt.})$$

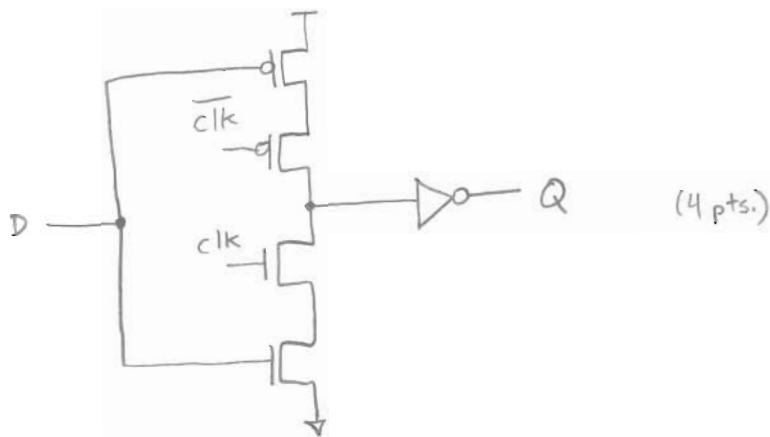


**Problem 4.3 (8 points) Simplified Latches.** The latch design in Figure 4 can be simplified in at least two ways to create positive transparent latches with fewer transistors. Draw circuit schematics for two alternative solutions below. Your solutions can be either static or dynamic. You do not have to size the transistors.

Solution #1:



Solution #2:



other solutions possible

**Problem 4.4 (3 points) Discussion.** Assume the transistor parameters in Table 1 and that you size the transistors in your solutions to Problem 4.3 such that all circuit nodes have equal rise and fall times while minimizing transistor gate capacitance. Which of your solutions is lower power (circle one)? Justify your answer.

Solution #1

Pass gates can be sized smaller than  $C^2MOS$   
so less dynamic power on clock

Solution #2