EEC 216 W08 Problem Set #1 Solutions

Rajeevan Amirtharajah
Dept. of Electrical and Computer Engineering
University of California, Davis

February 11, 2008

Problem 1

1.1 Figure 1 shows the layout for a minimum-sized NMOS device for computing the width, source/drain area, and source/drain perimeter, based on the MOSIS DEEP submicron rules for $\lambda = 0.024\mu m$. The formulas and their values are entered into Table 1. It is also acceptable to use the alternative contact rules (Rule 6.2.b), in which case the ACTIVE overlap of CONTACT is 1λ for a minimum NMOS width of 4λ and the minimum extension of ACTIVE beyond the polysilicon gate is 5λ (**5 points**).

Two possible ways of determining the sizing are to perform a DC sweep of the inverter input voltage and size the PMOS so that the transition from high to low occurs when the input is at $\frac{V_{DD}}{2}$. This approach is shown in Figure 2 which displays the V_{in} versus V_{out} curve for three possible sizings. An alternative is to tie the output of the inverter back to the input and adjust the PMOS sizing until it settles to $\frac{V_{DD}}{2}$. This approach is shown for three PMOS sizes in Figure 2, which displays the inverter output voltage in feedback. A P/N ratio of 1, 2, or 3 is reasonably close, but a ratio of 2 is probably the most appropriate choice since it roughly balances the mobility ratios without using too much area for the PMOS device. This ratio is used to compute the PMOS parameters in Table 1 (**5 points**) Similar approaches can be used to size the inverters for thresholds of $V_{DD}/4$ (which requires a nonminimum channel length PMOS) and $3V_{DD}/4$ (which requires a very large width PMOS device) (**10 points**).

V_{SW}	**Device**	**Length**	**Width**	**PD/PS**	**AD/AS**
$\frac{V_{DD}}{2}$	NMOS	0.048 μm	$5\lambda = 0.12\mu$m	$1 \cdot 5\lambda + 2 \cdot 5.5\lambda = 0.384\mu$m	$5 \cdot 5.5\lambda^2 = 0.01584\mu\text{m}^2$
	PMOS	0.048 μm	$10\lambda = 0.24\mu$m	$1 \cdot 10\lambda + 2 \cdot 5.5\lambda = 0.504\mu$m	$10 \cdot 5.5\lambda^2 = 0.03168\mu\text{m}^2$
$\frac{V_{DD}}{4}$	NMOS	0.048 μm	$5\lambda = 0.12\mu$m	0.384μm	$0.01584\mu\text{m}^2$
	PMOS	$27\lambda = 0.648\mu$m	$5\lambda = 0.12\mu$m	0.384μm	$0.01584\mu\text{m}^2$
$\frac{3V_{DD}}{4}$	NMOS	0.048 μm	$5\lambda = 0.12\mu$m	0.384μm	$0.01584\mu\text{m}^2$
	PMOS	0.048 μm	$200\lambda = 4.8\mu$m	5.064μm	$0.6336\mu\text{m}^2$

Table 1: CMOS Inverter Sizing.

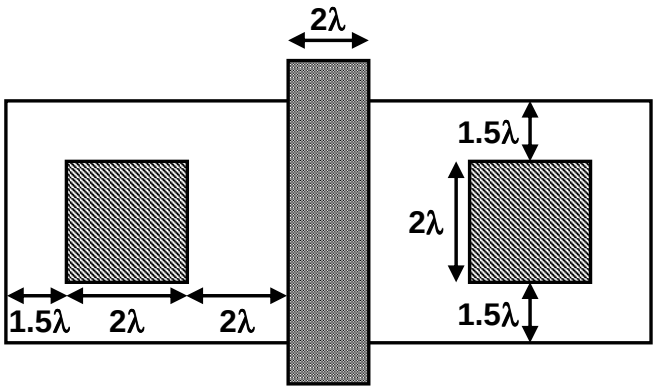

Figure 1: Layout of minimum-sized NMOS device.

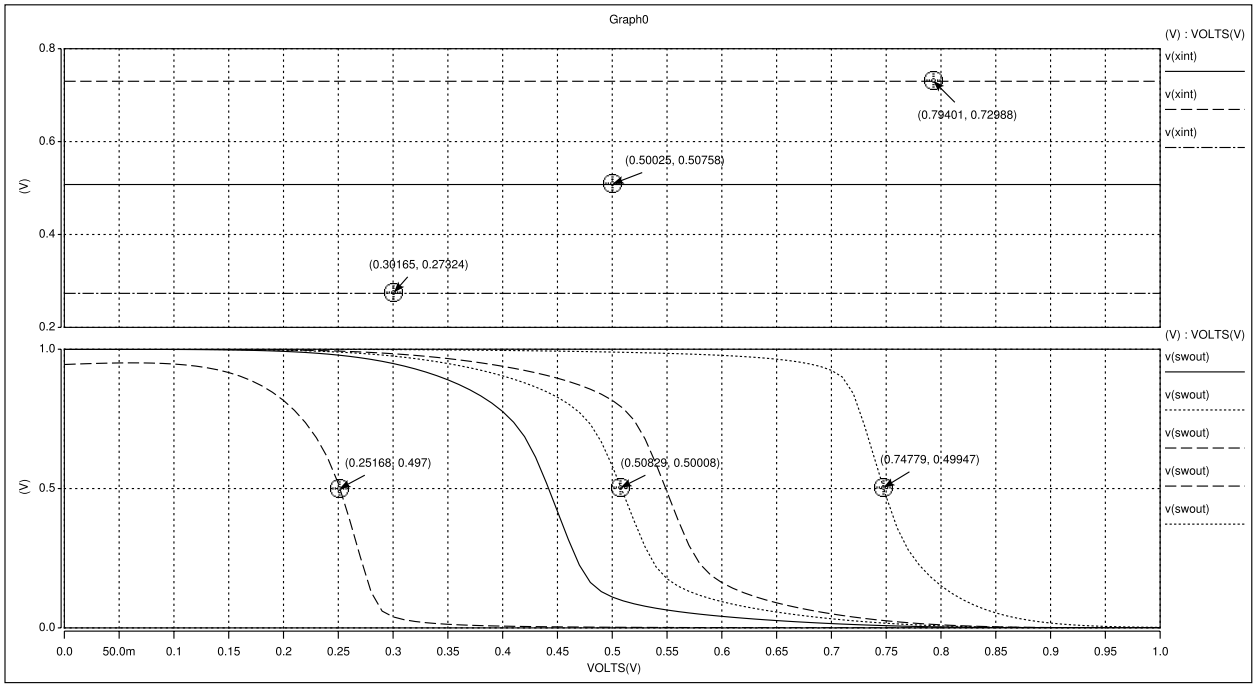

Figure 2: Inverter sizing based on inverter output feedback and on DC input voltage sweep.

The following Hspice deck was used to generate the figures for this solution (note that in some SPICE implementations, the .alter commands result in incorrect simulation, in that case just cut-and-paste the different macros into separate SPICE files and simulate them individually):

```
* EEC 216 W08 Problem Set 1 Number 1.1
* File: ps1n1d1.sp
* Author:  Raj Amirtharajah (ramirtha@ece.ucdavis.edu)
* Date: 02/09/08
**
**
** Problem Set 1
**
** Problem 1.1: Static CMOS Sizing
** Last edited: Feb 10 09:18 2008 (ramirtha)
**--------------------------------------------------------------------------

.include '45nm_MGHiK.sp'
.param lambda=24nm vdd=1.0V vsweep=0V

.options accurate post
.temp 27

.tran 2ps 10.0ns
.dc vsweep start=0V stop=1.0V step=10mV

.global vdd gnd
.probe
.op
.nodeset swout=vdd

* Power Supplies
Vvdd vdd    gnd dc=vdd
Vsweep swin gnd dc=vsweep

* NOTE: DEEP submicron scalable rules for contacts set the minimum width
* as 1.5+2+1.5=5 lambda, and minimum S/D area as 5 lambda x 2+2+1.5=5.5
* lambda = 27.5 lambda^2.  S/D perimeter is 5+2x5.5 lambda = 16 lambda.

* Parameters
* ----------
.param Wmin='5*lambda'

* Three terminal FET macros
* -------------------------
```

```
.macro nfet s g d Le='2*lambda' Wi=Wmin
MN0 s g d gnd nmos L=Le W=Wi AS='5.5*lambda*Wi' PS='2*5.5*lambda+Wi'
+ AD='5.5*lambda*Wi' PD='2*5.5*lambda+Wi'
.eom

.macro pfet s g d Le='2*lambda' Wi=Wmin
MP0 s g d vdd pmos L=Le W=Wi AS='5.5*lambda*Wi' PS='2*5.5*lambda+Wi'
+ AD='5.5*lambda*Wi' PD='2*5.5*lambda+Wi'
.eom

* Inverter
* --------
.macro inv in out
Xp0 vdd in out pfet Wi='2*5*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom inv

* Sizing Test: Feedback
* ---------------------
Xdut0 xint xint inv

* Sizing Test: DC Sweep
* ---------------------
Xdut1 swin swout inv

.alter
* Inverter: Traditional Sizing
* ----------------------------
.macro inv in out
Xp0 vdd in out pfet Wi='3*5*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom inv

.alter
* Inverter
* --------
.macro inv in out
Xp0 vdd in out pfet Wi='1*5*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom

.alter
* Inverter: Vdd/4
* ---------------
.macro inv in out
```

```
Xp0 vdd in out pfet Wi='1*5*lambda' Le='27*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom

.alter
* Inverter: 3Vdd/4
* ---------------
.macro inv in out
Xp0 vdd in out pfet Wi='200*lambda' Le='2*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom

.end
```

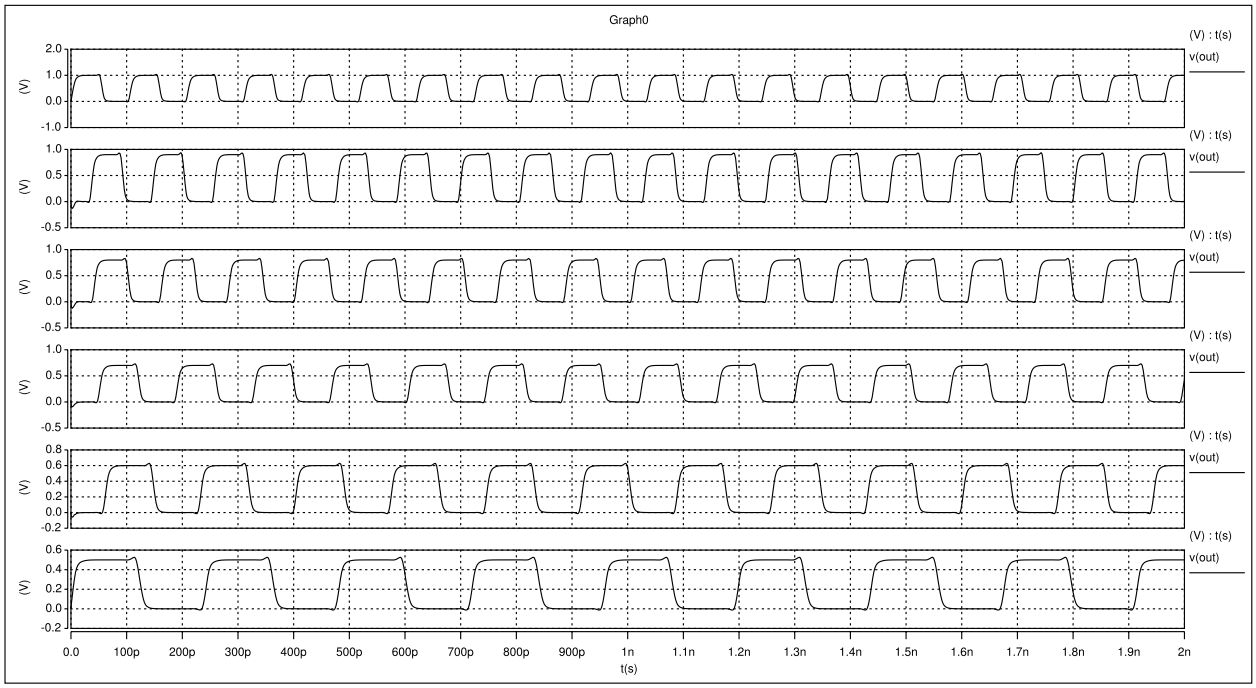

Figure 3: Ring oscillator waveforms at different supply voltages ($\frac{V_{DD}}{2}$ switching threshold).

1.2 Figure 3, 4, and 5 show the ring oscillator waveform outputs at the supply voltages tested for all three inverter thresholds. As the threshold is decreased below $V_{DD}/2$, the high-low transition occurs faster and the low-high transition is slower. The opposite effect occurs when the threshold is raised above $V_{DD}/2$. The inverter delays are listed in Tables 2, 4, and 3 (**10 points**). Note that using the 50%-50% delay specification can lead to spurious results (negative delays) for skewed inverter sizes. This occurs because the output switches through the $V_{DD}/2$ point before the input completes its transition or reaches the same point. Another approach to measuring inverter delay is to divide the ring oscillator period by twice the number of inverter stages (a transition must propagate twice through the ring to go through two inversions). These results are tabulated in the fourth column of the tables and give a more correct average delay for the circuit. Figures 6, 7, and 8 plot the inverter delay as V_{DD} is varied from 0.5 V to 1.0 V as the solid line for each of the three inverter sizings (**10 points**).

An example spice deck for measuring inverter delays using ring oscillators follows (**5 points**). Note that there may be issues in using the .alter card. Also, you may need to edit the .measure cards to reference the correct rising and falling edges when measuring delays as some simulators will have different initial transients on the circuit nodes.

```
* EEC 216 W08 Problem Set 1 Number 1.2
* File: ps1n1d2.sp
* Author:  Raj Amirtharajah (ramirtha@ece.ucdavis.edu)
* Date: 01/15/08
**
```

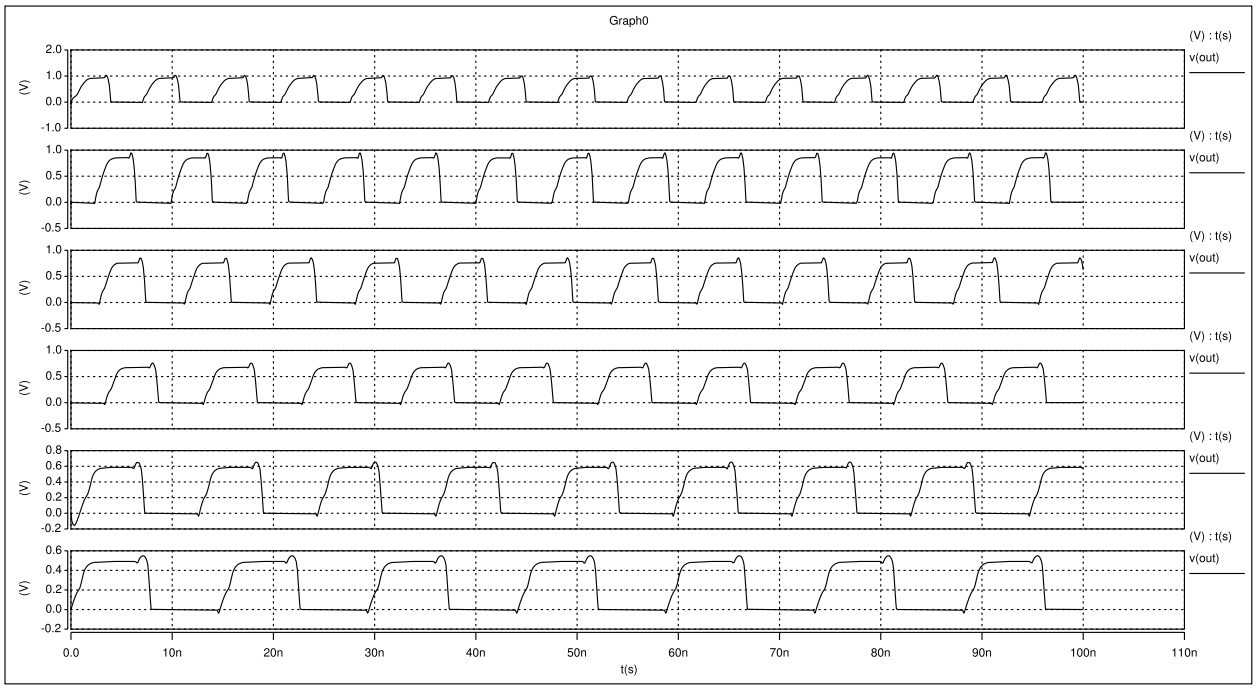

Figure 4: Ring oscillator waveforms at different supply voltages ($\frac{V_{DD}}{4}$ switching threshold).

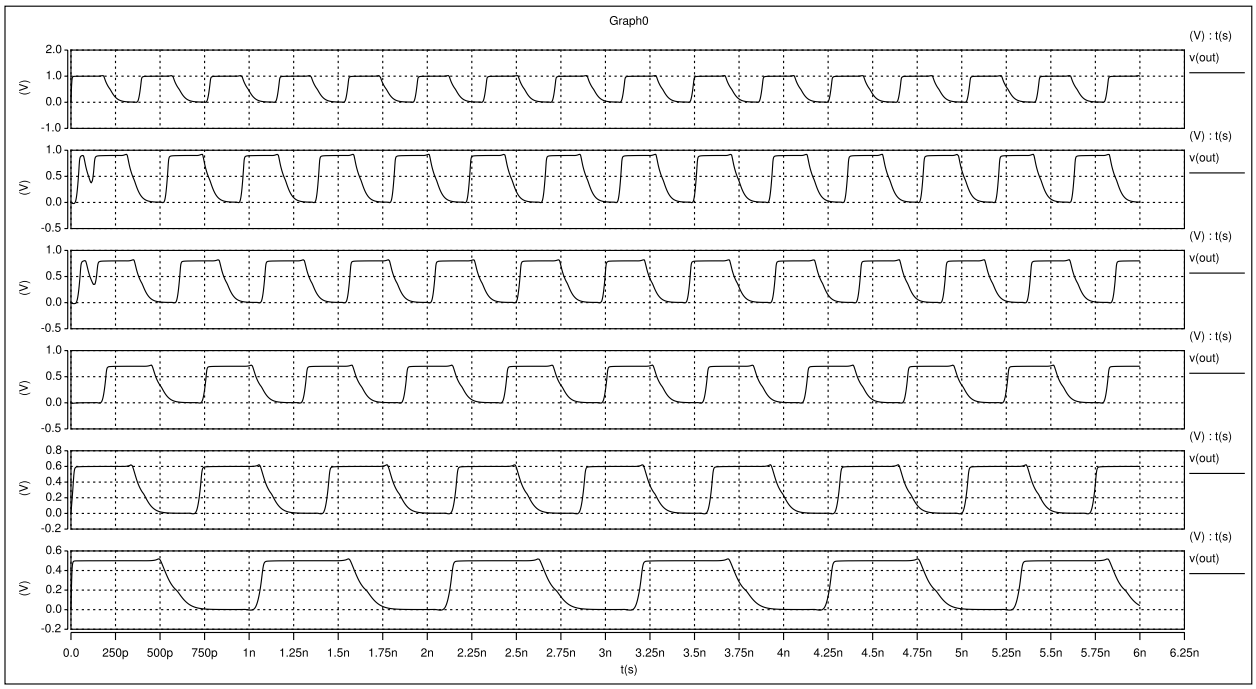

Figure 5: Ring oscillator waveforms at different supply voltages ($\frac{3V_{DD}}{4}$ switching threshold).

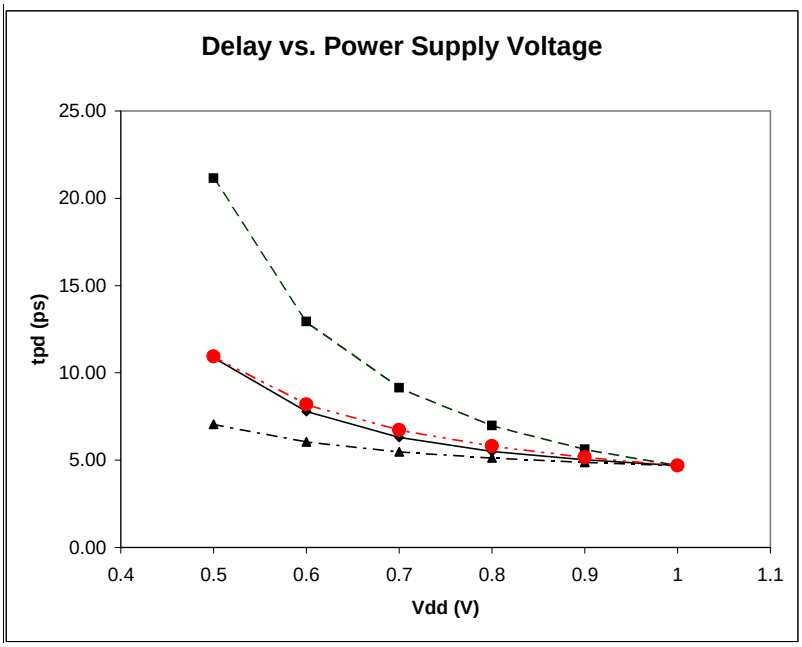

Figure 6: Inverter delay versus supply voltage ($\frac{V_{DD}}{2}$ switching threshold).

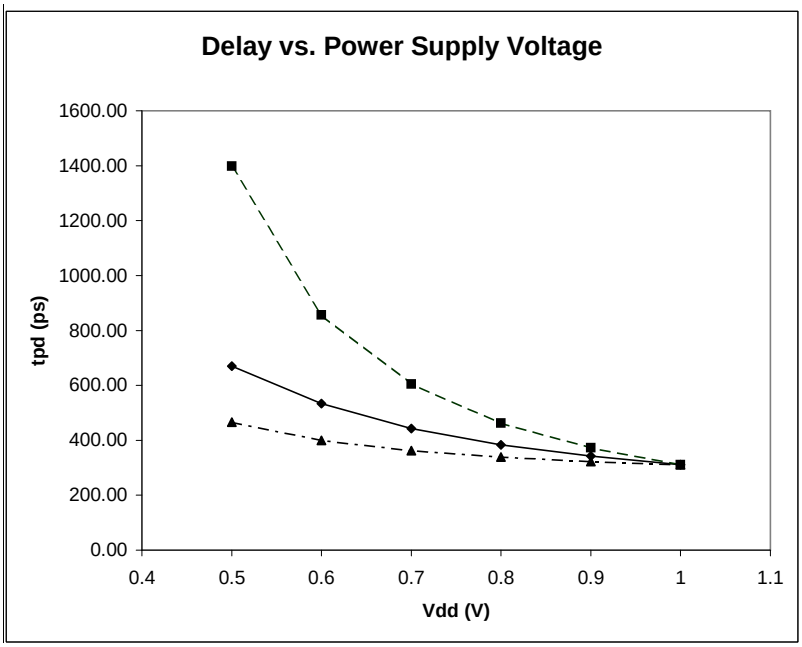

Figure 7: Inverter delay versus supply voltage ($\frac{V_{DD}}{4}$ switching threshold).

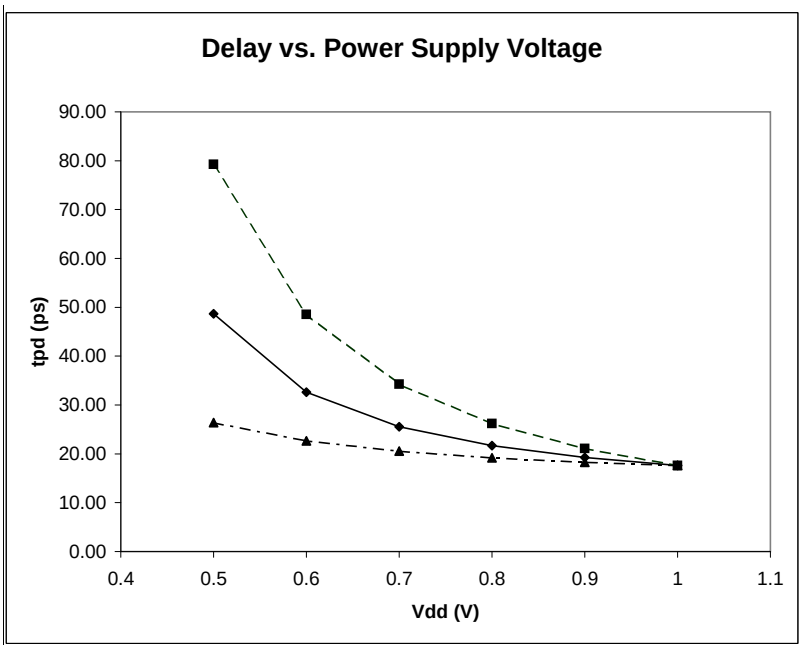

Figure 8: Inverter delay versus supply voltage ($\frac{3V_{DD}}{4}$ switching threshold).

```
**
** Problem Set 1
**
** Problem 1.2: Voltage-Delay Tradeoff
** Last edited: Jan 16 10:58 2008 (ramirtha)
**-------------------------------------------------------------------------

.include 'macros.sp'
.include '45nm_MGHiK.sp'
.param lambda=24nm vdd=0.5V

.options accurate post probe
.temp 27

.tran 1ps 2.0ns

.global vdd gnd
.probe v(n0) v(n1) v(n2) v(out)

* Power Supplies
Vvdd vdd   gnd dc=vdd

* Inverters
* ---------
```

	$V_{SW} = \frac{V_{DD}}{2}$			
V_{DD}	t_{PHL} (ps)	t_{PLH} (ps)	$T_{RO}/22$ (ps)	**Delay** (ps)
0.5 V	11.6	10.2	10.9	10.9
0.6 V	8.1	7.5	7.8	7.8
0.7 V	6.5	6.1	6.3	6.3
0.8 V	5.6	5.4	5.5	5.5
0.9 V	5.0	5.1	5.0	5.0
1.0 V	4.6	4.8	4.7	4.7

Table 2: CMOS Inverter Delay at Different Supply Voltages for Half V_{DD} Switching Threshold.

	$V_{SW} = \frac{3V_{DD}}{4}$			
V_{DD}	t_{PHL} (ps)	t_{PLH} (ps)	$T_{RO}/22$ (ps)	**Delay** (ps)
0.5 V	82.6	14.3	48.6	48.6
0.6 V	59.3	5.9	32.6	32.6
0.7 V	50.2	0.9	25.6	25.6
0.8 V	45.8	953	21.7	21.7
0.9 V	43.4	843	19.3	19.3
1.0 V	41.9	-6.7	17.6	17.6

Table 3: CMOS Inverter Delay at Different Supply Voltages for Three-Quarter V_{DD} Switching Threshold.

```
.macro inv in out
Xp0 vdd in out pfet Wi='2*5*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom

.macro invT in out
Xp0 vcc in out pfetT Wi='2*5*lambda'
Xn0 gnd in out nfetT Wi='5*lambda'
.eom

* 11-Stage Ring Oscillator
* ------------------------
.ic out=0V
.ic n1=0V
.ic n2=vdd
Xinv0 out n0  inv
Xinv1 n0  n1  inv
Xinv2 n1  n2  inv
Xinv3 n2  n3  inv
Xinv4 n3  n4  inv
```

	$V_{SW} = \frac{V_{DD}}{4}$			
V_{DD}	t_{PHL} (ps)	t_{PLH} (ps)	$T_{RO}/22$ (ps)	**Delay** (ps)
0.5 V	83.9	1260	670	670
0.6 V	8.4	1060	533	533
0.7 V	-47.3	933	443	443
0.8 V	-92.2	859	384	384
0.9 V	-129	814	342	342
1.0 V	-162	783	311	311

Table 4: CMOS Inverter Delay at Different Supply Voltages for Quarter V_{DD} Switching Threshold.

```
Xinv5 n4  n5  inv
Xinv6 n5  n6  inv
Xinv7 n6  n7  inv
Xinv8 n7  n8  inv
Xinv9 n8  n9  inv
Xinv10 n9  out inv

.measure tran tpdn trig v(n1) val='vdd/2' rise=2
+                  targ v(n2) val='vdd/2' fall=2
.measure tran tpup trig v(n1) val='vdd/2' fall=2
+                  targ v(n2) val='vdd/2' rise=2

.measure tran tpeu trig v(out) val='vdd/2' rise=2
+                  targ v(out) val='vdd/2' rise=3
.measure tran tped trig v(out) val='vdd/2' fall=2
+                  targ v(out) val='vdd/2' fall=3

.alter
.param vdd=0.6V

.alter
.param vdd=0.7V

.alter
.param vdd=0.8V

.alter
.param vdd=0.9V

.alter
.param vdd=1.0V
```

```
.alter
.param vdd=0.5V
* Inverter: Vdd/4
* ---------------
.macro inv in out
Xp0 vdd in out pfet Wi='1*5*lambda' Le='27*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom

.alter
.param vdd=0.6V

.alter
.param vdd=0.7V

.alter
.param vdd=0.8V

.alter
.param vdd=0.9V

.alter
.param vdd=1.0V

.alter
.param vdd=0.5V
* Inverter: 3Vdd/4
* ---------------
.macro inv in out
Xp0 vdd in out pfet Wi='200*lambda' Le='2*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom

.alter
.param vdd=0.6V

.alter
.param vdd=0.7V

.alter
.param vdd=0.8V

.alter
.param vdd=0.9V
```

```
.alter
.param vdd=1.0V

.end
```

1.2 (cont.) Figures 6, 7, and 8 also plot two alternative models for delay scaling with V_{DD}. The dashed curve assumes a quadratic dependence for I_{DS} on $V_{GS} - V_T$, corresponding to the classical model. The dash-dot curve represents a linear dependence. As can be seen from the first graph, the measured delay scaling is less than quadratic, indicating that the classical model is not necessarily applicable. However, it does scale faster than the linear curve. Velocity saturation is the most likely cause for the deviation from the classical MOS model. A similar curve occurs for the third graph (switching threshold $3V_{DD}/4$). (**5 points**). A fitted curve is shown in red and marked with circles in Figure 6, which corresponds to a dependence to the power 1.4.

1.3 Figures 9, 10, and 11 display the single inverter switching cycle and the corresponding supply current (**6 points**). The current shape matches intuition in that the current is drawn from the supply during charging of the output to V_{DD}. The other positive current spikes correspond to capacitive coupling on the output (the small blips can be seen on the output node) pushing charge into the supply. Note that the current is not particularly triangular in shape, so there is a component corresponding to the dynamic power and a component corresponding to short circuit current, which is especially important in the $V_{DD}/4$ case since the rise time is so long. (**3 points**). For the $V_{DD}/2$ switching threshold, the average current is given by a measure card as 10.71μA which corresponds to an average power of 10.71μW (**2 points**). For the $V_{DD}/4$ switching threshold, the average current is given by a measure card as 934 nA which corresponds to an average power of 934 nW (**2 points**). For the $3V_{DD}/4$ switching threshold, the average current is given by a measure card as 38.63μA which corresponds to an average power of 38.63μW (**2 points**). The average current for the $V_{DD}/4$ case is so low because it's switching frequency is much lower than the $V_{DD}/2$ case. Note also the significant leakage current for this inverter sizing. Although the oscillator frequency of the $3V_{DD}/4$ design is also very low, it has so much more switched capacitance that the average power is higher.

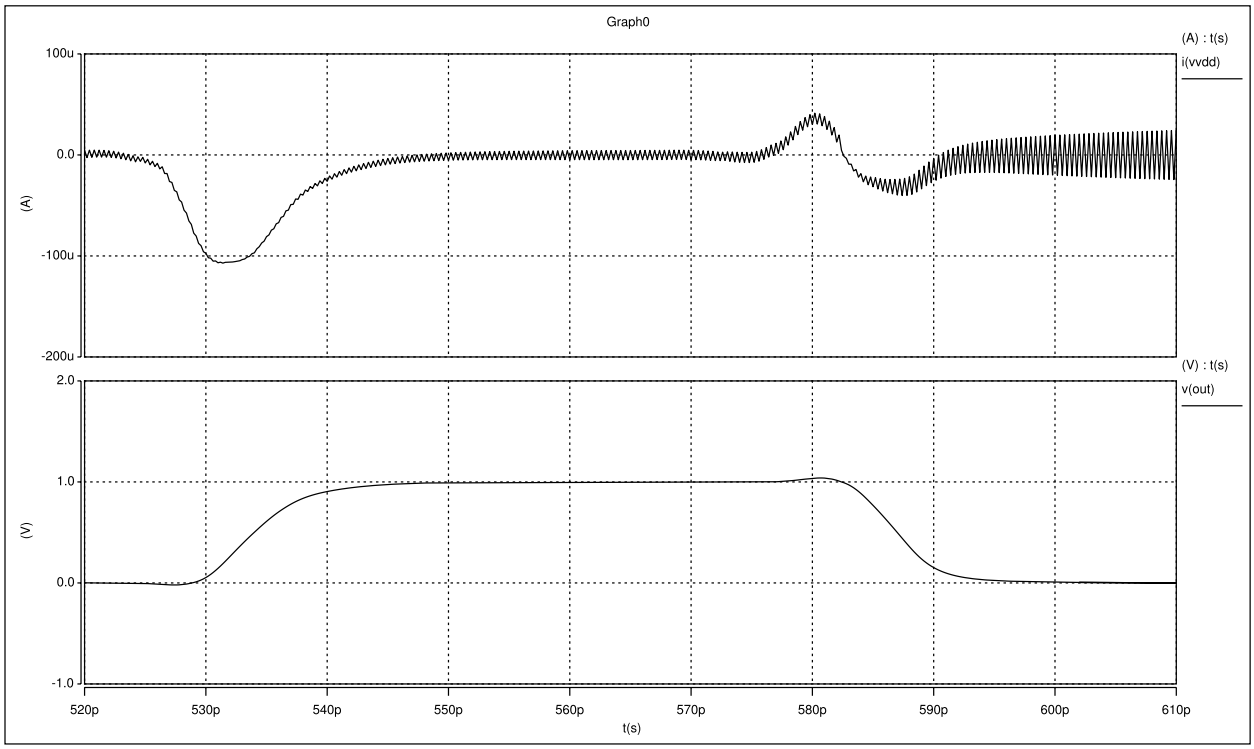

Figure 9: Single charge-discharge cycle and corresponding power supply current for a single inverter in the ring oscillator (switching threshold $V_{DD}/2$).

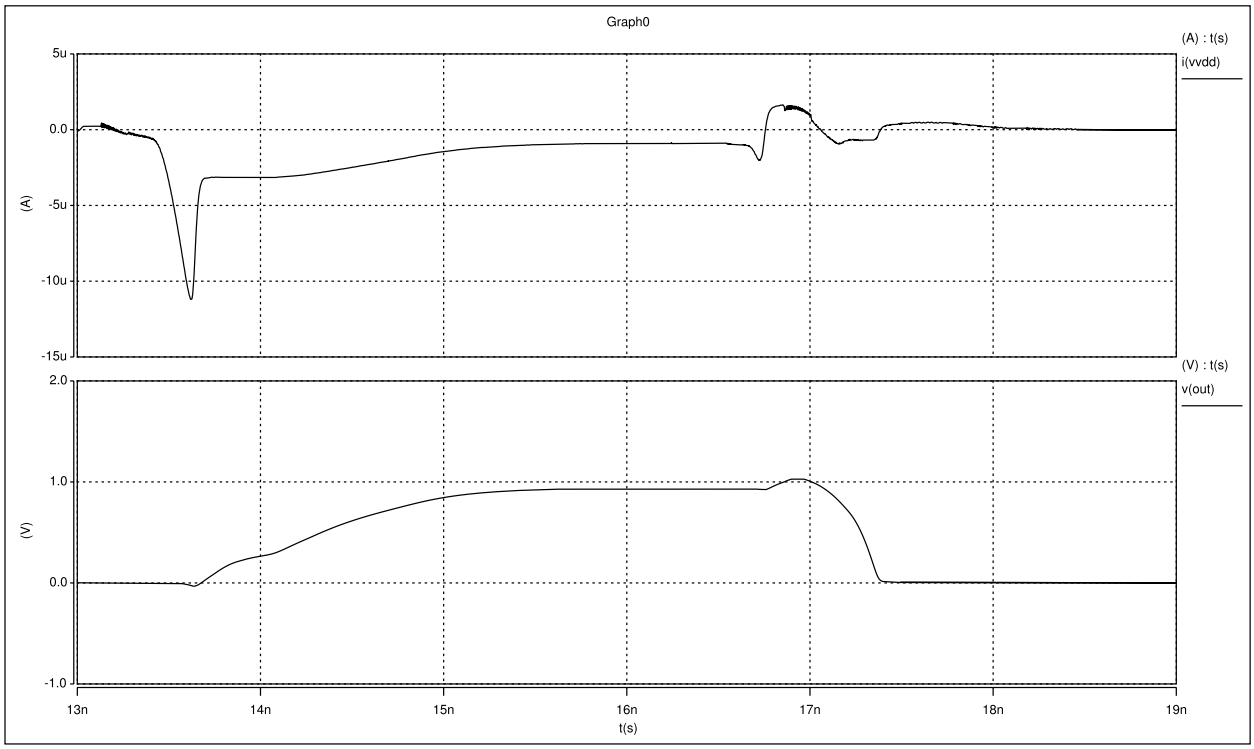

Figure 10: Single charge-discharge cycle and corresponding power supply current for a single inverter in the ring oscillator (switching threshold $V_{DD}/4$).

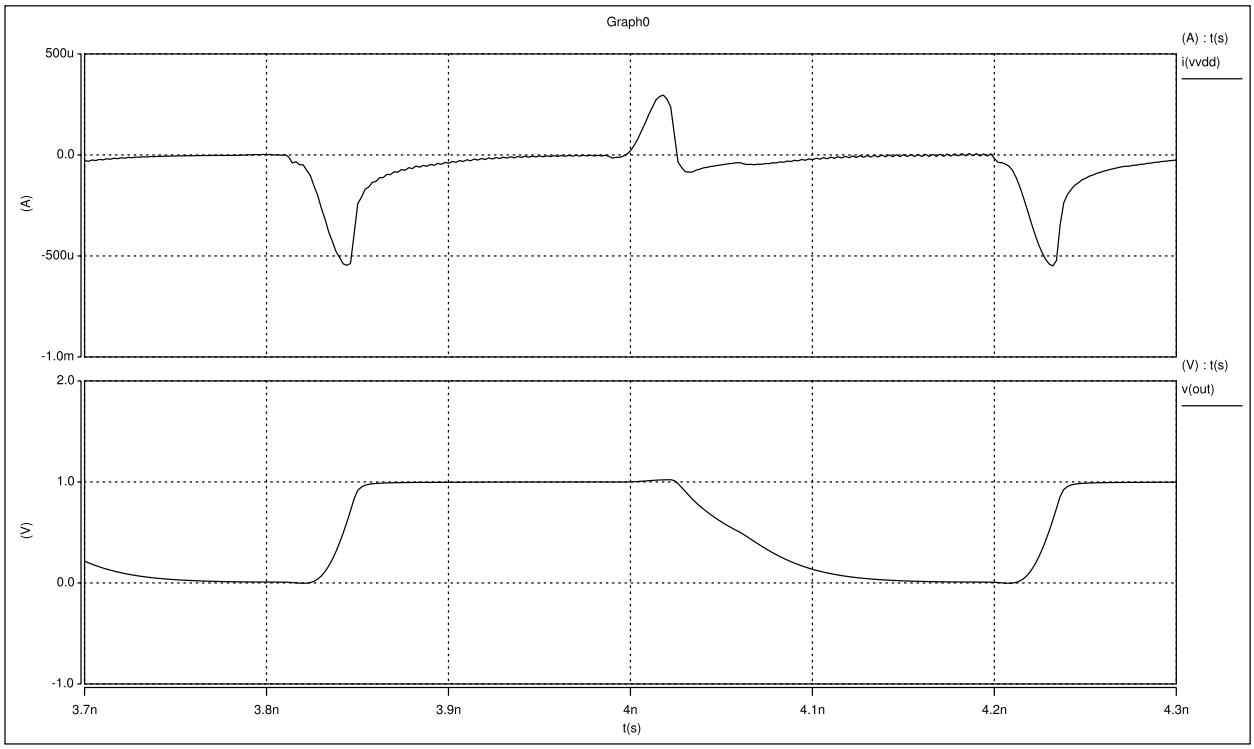

Figure 11: Single charge-discharge cycle and corresponding power supply current for a single inverter in the ring oscillator (switching threshold $3V_{DD}/4$).

The spice deck which generated the plots in Figures 9, 10, and 11 and the measured currents is (**3 points**):

```
* EEC 216 W08 Problem Set 1 Number 1.3
* File: ps1n1d3.sp
* Author:  Raj Amirtharajah (ramirtha@ece.ucdavis.edu)
* Date: 01/17/05
**
**
** Problem Set 1
**
** Problem 1.3: Power Consumption
** Last edited: Feb 10 21:07 2008 (ramirtha)
**--------------------------------------------------------------------------

.include 'macros.sp'
.include '45nm_MGHiK.sp'
.param lambda=24nm vdd=1.0V

.options accurate post probe absmos=1e-15 relmos=0.001 abstol=1e-15
.temp 27

.tran 1ps 100.0ns

.global vdd vcc gnd
.probe v(n0) v(n1) v(n2) v(out)

* Power Supplies
Vvdd vdd   gnd dc=vdd
Vvcc vcc   gnd dc=vdd

* Inverters
* ---------
.macro inv in out
Xp0 vdd in out pfet Wi='2*5*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom

.macro invT in out
Xp0 vcc in out pfetT Wi='2*5*lambda'
Xn0 gnd in out nfetT Wi='5*lambda'
.eom

* 11-Stage Ring Oscillator
* ------------------------
```

```
.ic out=0V
.ic n1=0V
.ic n2=vdd
Xinv0 out n0  invT
Xinv1 n0  n1  invT
Xinv2 n1  n2  invT
Xinv3 n2  n3  invT
Xinv4 n3  n4  invT
Xinv5 n4  n5  invT
Xinv6 n5  n6  invT
Xinv7 n6  n7  invT
Xinv8 n7  n8  invT
Xinv9 n8  n9  invT
Xinv10 n9  out inv

.measure tran avgcur AVG i(Vvdd)

.alter
* Inverter: Vdd/4
* ---------------
.macro inv in out
Xp0 vdd in out pfet Wi='1*5*lambda' Le='27*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom

.macro invT in out
Xp0 vcc in out pfetT Wi='1*5*lambda' Le='27*lambda'
Xn0 gnd in out nfetT Wi='5*lambda'
.eom

.alter
.ic out=vdd
* Inverter: 3Vdd/4
* ---------------
.macro inv in out
Xp0 vdd in out pfet Wi='200*lambda' Le='2*lambda'
Xn0 gnd in out nfet Wi='5*lambda'
.eom

.macro invT in out
Xp0 vcc in out pfetT Wi='200*lambda' Le='2*lambda'
Xn0 gnd in out nfetT Wi='5*lambda'
.eom

.end
```

Problem 2

2.1 Each of the equations in Chandrakasan's paper reflect purely dynamic power: $P = CV^2f$ [1]. We add to each of the equations a leakage term which is proportional to area, such that total power is now $P_{TOT} = CV^2f + kI_0AV$ (**2 points**). The modified equations and the relative leakage currents I_0 follow.

Reference datapath (**2 point**):

$$P_{ref} = C_{ref}V_{ref}^2 f_{ref} + kI_0AV_{ref} \quad (1)$$

$$I_0(ref) = \frac{C_{ref}V_{ref}f_{ref}}{kA} \quad (2)$$

Parallel datapath (**2 point**):

$$P_{par} = (2.15C_{ref})(0.58V_{ref})^2\left(\frac{f_{ref}}{2}\right) + kI_0(3.4A)(0.58V_{ref}) \quad (3)$$

$$\begin{aligned} I_0(par) &= \frac{(2.15C_{ref})(0.58V_{ref})f_{ref}}{kA(2)(3.4)} \\ &= (0.1834)I_0(ref) \end{aligned} \quad (4)$$

Pipelined datapath (**2 point**):

$$P_{pipe} = (1.15C_{ref})(0.58V_{ref})^2 f_{ref} + kI_0(1.3A)(0.58V_{ref}) \quad (5)$$

$$\begin{aligned} I_0(pipe) &= \frac{(1.15C_{ref})(0.58V_{ref})f_{ref}}{kA(1.3)} \\ &= (0.51)I_0(ref) \end{aligned} \quad (6)$$

Parallel-Pipelined datapath (**2 point**):

$$P_{parpipe} = (2.5C_{ref})(0.4V_{ref})^2\left(\frac{f_{ref}}{2}\right) + kI_0(3.7A)(0.4V_{ref}) \quad (7)$$

$$\begin{aligned} I_0(parpipe) &= \frac{(2.5C_{ref})(0.4V_{ref})f_{ref}}{kA(2)(3.7)} \\ &= (0.1351)I_0(ref) \end{aligned} \quad (8)$$

By increasing the number of devices through parallelism and pipelining, the designer also increases the amount of leakage current since all of those extra devices will leak when not in use. Thus, the most area-intensive architecture (parallel-pipelined) only needs 13% of the per-device leakage of the reference datapath for leakage power to contribute equally to dynamic power for total power consumption. Partly this is due to reducing the dynamic power and partly this is due to increased senstivity to leakage through a larger number of devices. Now the tradeoff is not just area for power, but area plus leakage power for dynamic power (**2 points**). Because there is now a power penalty associated with these architectural changes, one is less likely to be as aggressive utilizing them, which means in general the optimal supply voltage will be higher for the overall system (**2 points**). The designer is more likely to use a single datapath with less pipelining, and so will keep the power supply voltage higher, expending more dynamic power but keeping leakage to a minimum (**1 points**).

References

[1] A. Chandrakasan, S. Sheng, and R. W. Broderson, "Low-power CMOS digital design," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 4, pp. 473–84, April 1992.