

# Performance Comparison of SRAM Cells Implemented in 6, 7 and 8-Transistor Cell Topologies

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**Abstract**—Cell stability and area are among the major concerns in SRAM cell designs. This paper compares the performance of three SRAM cell topologies, which include the conventional 6T-cell and the recently published 7T and 8T-cell implementations. In particular, the static-noise-margin (SNM) of each cell design is examined. Even though 7T and 8T cell implementation result in a reported 13% and 30% area increase, respectively, these two topologies allow for better cell stability due to their read-disturb-free operation, which is beneficial as process technologies continue to scale down.

## I. SRAM CELL IMPLEMENTATION

### A. 6T-Cell and 8T-Cell Design

The conventional 6T-cell schematic is shown in Fig. 1(a). This most commonly used SRAM cell implementation has the advantage of low static power dissipation. However, the potential stability problem of this design is such that during the read operation, a stored “0” can be overwritten by a “1” when the voltage at node V1 reaches the  $V_{th}$  of NMOS N2 to pull node V2 down to “0” and in turn pull node V1 up even further to “1” due to the mechanism of positive feedback.

To overcome the problem of data storage destruction during the read operation, an 8T-cell implementation was proposed [1], for which separate read/write bit and word signal lines are used [Fig. 1(b)] to separate the data retention element and the data output element. In turn, the cell implementation provides a read-disturb-free operation. However, this implementation uses eight transistors, which results in a cell area increase of 30% in comparison to the conventional 6T-cell design.

### B. 7T-Cell Design

The recently published 7T-cell design [2] also employs separate read and write signal lines but uses only one extra NMOS transistor to achieve read-disturb-free operation, thus increasing the cell area by 13%. NMOS transistor N5, whose gate is controlled by signal /WL, is added between node V2 and NMOS transistor N2, to the 6T-cell design as seen in Fig. 1(c). While the cell is being accessed, /WL is set to “0” to turn off NMOS transistor N5. In the case of a “0” read, even if the voltage at node V1 reaches the  $V_{th}$  of NMOS transistor N2, node V2 cannot be pulled down to “0” and thus preserving the stored data. During data retention period, /WL is set to “1”, and the cell operates in the same way as the 6T-cell circuit.

## II. STATIC-NOISE-MARGIN (SNM)

The SNM is used to measure the SRAM cell stability. It is the maximum value of a dc disturbance that can be

tolerated by the cell before changing states [3]. Graphically, the SNM is represented by the largest square box that can be fitted in the butterfly characteristic curves of the SRAM cell [3]. The three designs in Fig. 1 were simulated such that all transistors are minimum-sized devices to achieve minimum cell area. During the read operation, the SNM is much smaller for the 6T design (Fig. 2 in red) because the characteristic curves are degraded by the voltage divider between the access transistors (N3 and N4) and the drive transistors (N1 and N2). Without the read-disturb, the characteristic curves of the 8T design is that of two cross-coupled inverters, which provide a larger SNM (Fig. 2 in blue). Figure 3 shows the characteristic curves for the 7T design during its retention period (in red) and read access period (in blue). For a “0” read, the SNM for the 7T design is much larger than that for the 6T design, and thus improving the stability of the SRAM cell.

Figure 4 shows that SNM decreases with decreasing voltage supply ( $V_{DD}$ ) (using 6T cell as an example). However, if a time limit is set (word line is only active for a finite amount of time), the SNM actually increases as  $V_{DD}$  decreases (Fig. 5). This is because at a lower  $V_{DD}$ , the cell current drawn from the bit line is smaller during a “0” read, so the charge stored onto the parasitic capacitance at node V1 is less, thus a lower voltage at node V1 is reached after a short amount of time, which means more static noise voltage can be tolerated before the cell change state. Here, SNM is the largest  $V_n$  (Fig. 6) that causes a state change in the cell after 400ps. Note that SNM is affected by the device ratio between the access transistors (N3 and N4) and the drive transistors (N1 and N2). Finally, Fig. 7 demonstrates that device mismatch degrades the SNM. Here, mismatch is introduced to the drive transistor N1. (1% mismatch is equivalent to  $W_{N1} = 0.99W_{min}$ ). In practice, process induced variations is not only limited to device geometry mismatch but also includes threshold voltage variability, which is not modeled in the simulations of this project. Therefore, SNM degradation can be more severe in reality.

## III. CONCLUSION

The stability performances of three SRAM cell topologies have been presented. As process technologies continue to advance, the speed of SRAMs will increase, but devices will be more susceptible to mismatches, which worsen the static-noise margin of SRAM cells. Due to stability concerns, the dual port designs that implement read-disturb-free feature such as that seen in the 7T and 8T cell implementation might become more practical in the future SRAM cell implementation.

## REFERENCES

- [1] L. Chang et al., “Stable SRAM Cell Design for the 32nm Node and Beyond,” *Symp. VLSI Tech. Dig.*, pp. 292-293, Jun., 2005.
- [2] K. Takeda et al., “A Read-Static-Noise-Margin-Free SRAM Cell for Low-Vdd and High-Speed Applications,” *IEEE JSSC*, pp. 113-121, Jan., 2006.
- [3] E. Seevinck et al., “Static-Noise Margin Analysis of MOS SRAM Cells,” *IEEE JSSC*, pp.748-754, Oct., 1987.

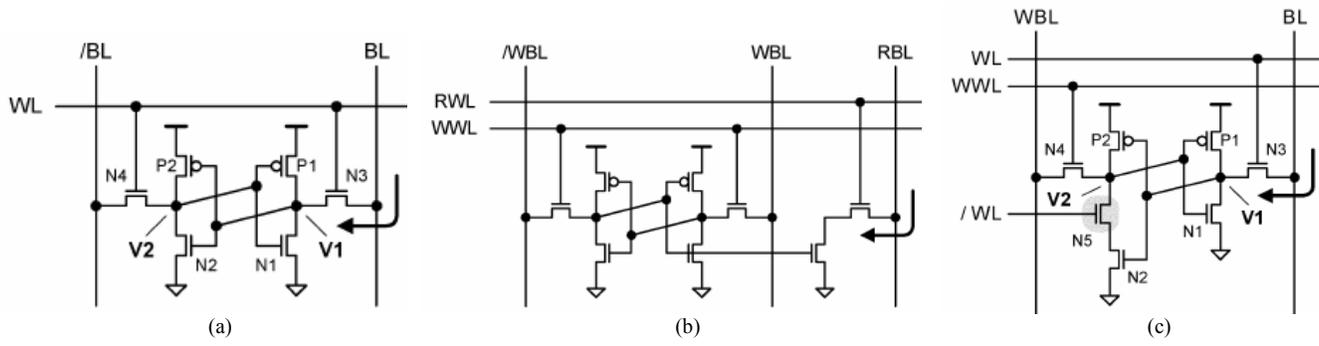


Figure 1. SRAM cell implementations (a) Conventional 6T-cell design; (b) 8T-cell design; and (c) 7T-cell design.

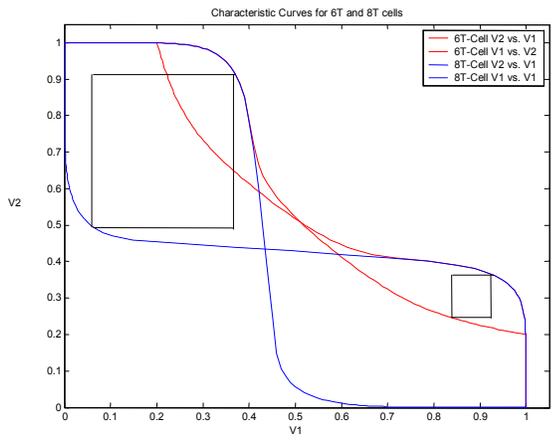


Figure 2. SNMs for 6T and 8T cell designs.

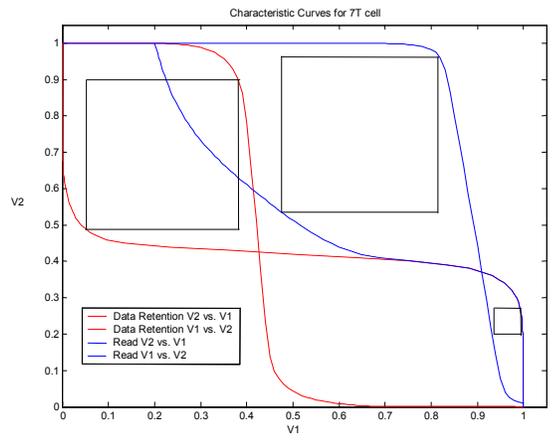


Figure 3. SNMs for 7T cell designs.

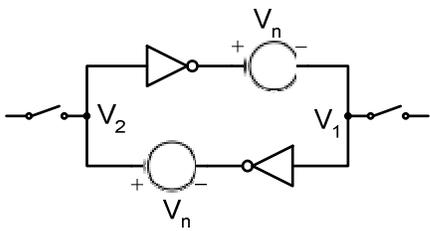


Figure 6. Simulation setup used to find SNM.

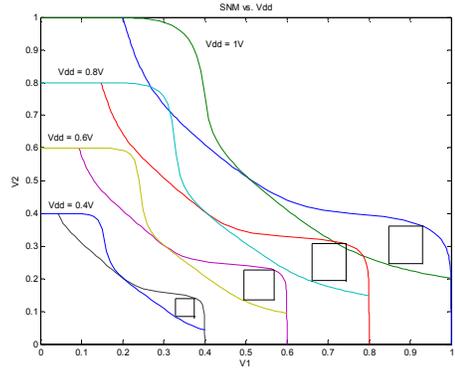


Figure 4. SNM vs.  $V_{DD}$  for 6T cell design.

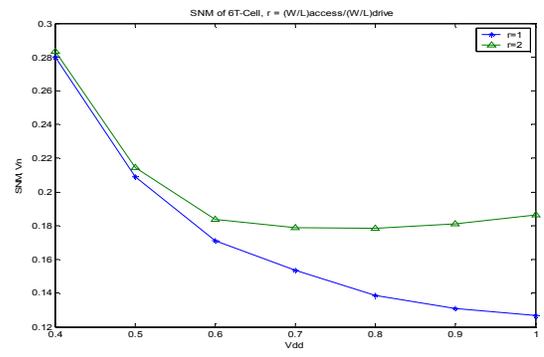


Figure 5. SNMs vs.  $V_{DD}$  for 6T cell design with time limit.

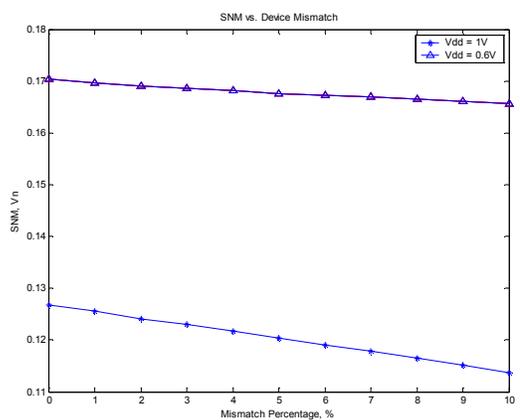


Figure 7. SNM vs. Device mismatch for 6T cell.