Performance Comparison of SRAM Cells Implemented in the 6, 7 and 8-Transistor Topologies

K. Takeda et al. *JSSC* Jan., 2006

L. Chang et al. *Symp. VLSI Tech. Dig.,* Jun., 2005

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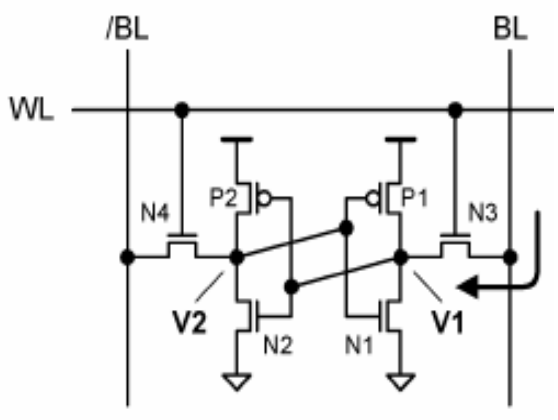
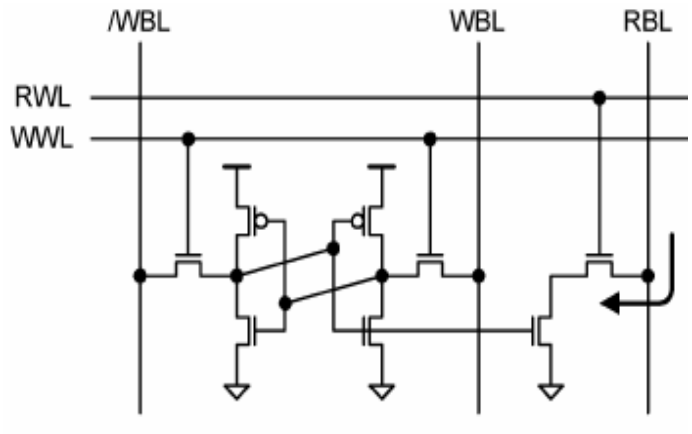
Final Project Presentation

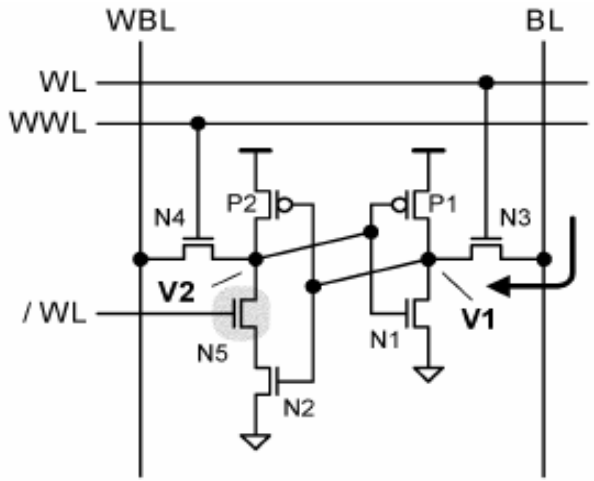
SRAM Cell Implementations



(a) Conventional 6T SRAM Cell



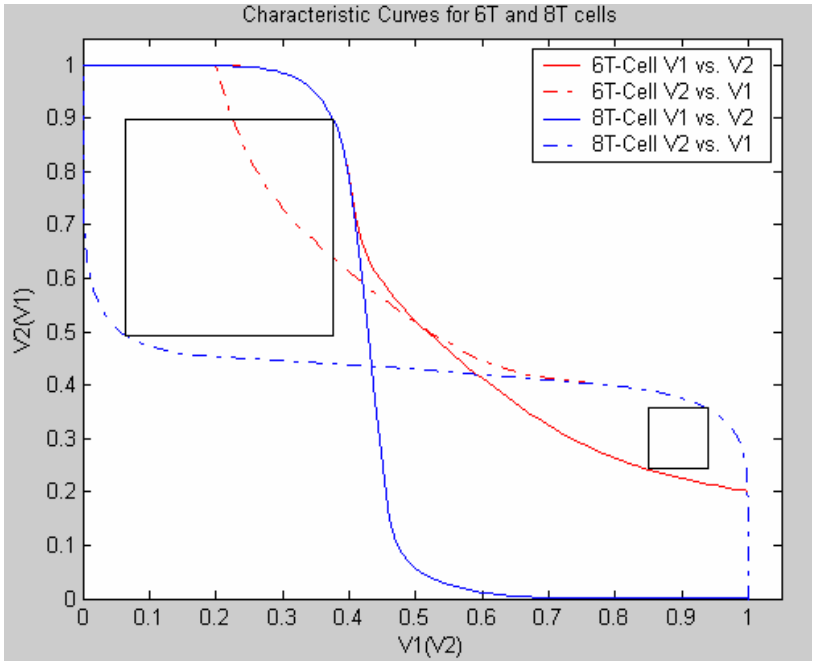
(b) Read-Disturb-Free 8T SRAM Cell

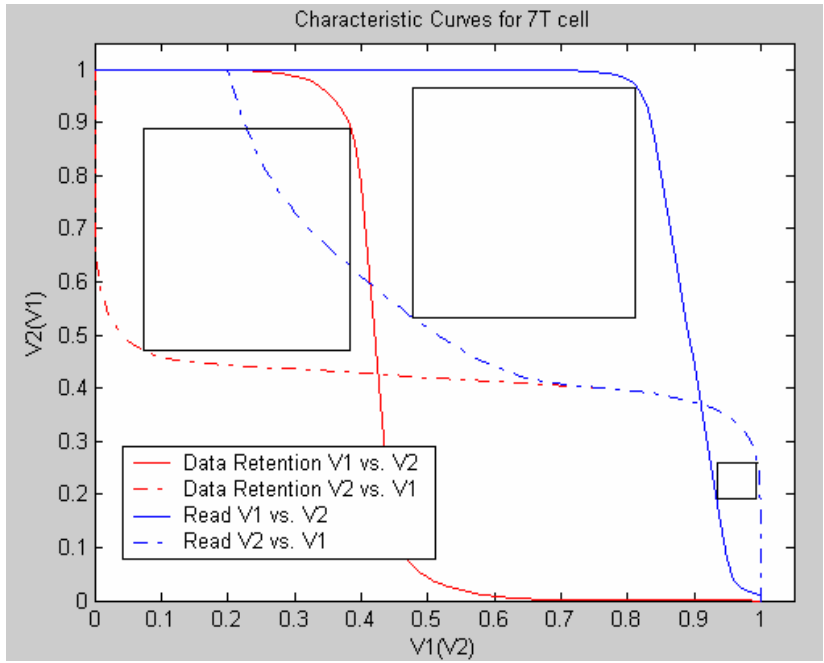


(c) Read-Disturb-Free 7T SRAM Cell

- Cell stability concern: storage data destruction during Read operation.
- Dual-port 8T cell: 30% increase in cell area
- 7T SRAM cell uses one extra NMOS transistor to achieve loop-cutting, while only increases cell area by 13%

Simulation Results





- Mismatch worsens static-noise-margin
- Dual port design more practical for deep submicron technologies