

# EEC 216 Winter 2007 Midterm

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February 9, 2007

Name:

**Instructions:** This test consists of 3 problems and 10 pages, including the cover sheet. Please make sure that you have all of them. This is an open-book, open-notes test. State any assumptions you make and show complete work to receive credit. The time limit is 50 minutes. The problems are weighted as shown below:

**Grading:**

Problem	Maximum	Score
1	17	
2	15	
3	18	
Total	50	

# 1 Logic Gate Design

For this problem, use the transistor parameters in Table 1.

Parameter	NMOS	PMOS
$V_t$	1 V	-1 V
$k' = \mu C_{ox}$	$300 \mu\text{A}/\text{V}^2$	$100 \mu\text{A}/\text{V}^2$
$W_{min}$	$2 \mu\text{m}$	$2 \mu\text{m}$
$L_{min}$	$1 \mu\text{m}$	$1 \mu\text{m}$

Table 1: Problem 1 Transistor Parameters.

**Problem 1.1 (6 points) Static CMOS.** Design a static CMOS gate to implement the following logical expression using a minimum number of transistors:

$$F = \overline{A \cdot D + B \cdot C \cdot D} \quad (1)$$

**Problem 1.2 (4 points) Static CMOS Sizing.** Size the transistors in the circuit you designed for Problem 1.1 such that the worst case rise and fall times are equal while minimizing the input capacitance to the logic gate. Label the sizes in your schematic for Problem 1.1.

**Problem 1.3 (4 points) Pseudo NMOS Design.** Design a pseudo-NMOS gate to implement Equation 1 such that the pullup network has the same resistance as the worst case pullup resistance for Problem 1.2 and  $V_{OL} \leq 0.2V_{DD}$  (assume  $V_{DD} = 2V$ ). Assume that the PMOS and NMOS devices are in the saturation regime of operation at all times and neglect channel length modulation.

**Problem 1.4 (3 points) Discussion.** Which of the two circuits is better for low power design? Justify your answer.

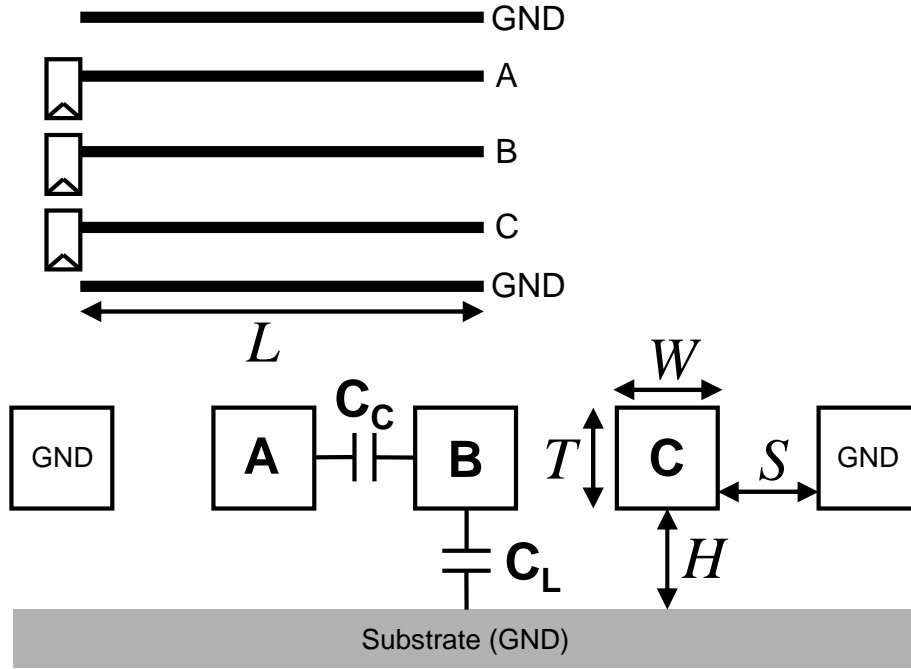


Figure 1: Three signal shielded bus. Plan view (top) and cross-section (bottom).

Parameter	Metal 1
Sheet Resistance ( $R_{sq.}$ )	$0.1 \Omega/sq.$
Spacing ( $S$ )	500 nm
Thickness ( $T$ )	$3 \mu\text{m}$
Height ( $H$ )	500 nm
Dielectric Constant ( $\epsilon_r$ )	$4.3 \times 8.85\text{e-}12 \text{ F/m}$
Length ( $L$ , on figure)	1.0 cm
Width ( $W$ )	$4.0 \mu\text{m}$

Table 2: Problem 2 Interconnect Parameters.

## 2 Bus Power

Figure 1 shows a three signal bus driven by positive edge-triggered flip-flops with two ground shields on the metal 1 layer. Assume that the dimensions shown in Figure 1 and listed in Table 2 hold for every line in the bus.

**Problem 2.1 (3 points) Coupling Capacitance.** Calculate the line-to-line capacitance  $C_C$ . Ignore any contribution of fringing fields.

**Problem 2.2 (3 points) Substrate Capacitance.** Using the same data as Problem 2.1, calculate the line-to-substrate capacitance  $C_L$ . Ignore any contribution of fringing fields.

**Problem 2.3 (6 points) Worst Case Power.** Draw a timing diagram of the data pattern on signals  $A$ ,  $B$ , and  $C$ , which results in the worst case power dissipation on line  $B$ . Calculate this worst case power based on the  $C_C$  and  $C_L$  you calculated earlier. Assume the flip-flops are clocked at 200 MHz with  $V_{DD} = 1.5\text{V}$ .

**Problem 2.4 (3 points) Clock Skew.** Suppose that there is significant clock skew at the flip-flops driving  $A$ ,  $B$ , and  $C$ . How would this affect the worst case power you computed in Problem 2.3? Justify your answer.



**Problem 3.2 (6 points) Dynamic Logic Timing.** Sketch timing diagrams of signals  $\Phi$ ,  $\overline{G}$ ,  $\overline{P}$ , and  $C_i$  for both input scenarios which result in  $C_o$  evaluating to logic 1. Ignore the circuit inside the dotted lines.

**Problem 3.3 (3 points) Dynamic Activity Factor.** What is the activity factor for node  $C_o$ , taking into account the action of signal  $\Phi$ ? Ignore the circuit inside the dotted lines.

**Problem 3.4 (2 points) Mystery Circuit.** What is the intended purpose of the circuit within the dotted lines?

**Problem 3.5 (3 points)** Suppose that the switching threshold of the inverter in Figure 2 is  $V_{DD}/2$ . Assume that the mobility of the PMOS devices is  $\frac{2}{5}$  of the mobility of the NMOS devices, i.e.  $5\mu_p = 2\mu_n$ . Including the circuit within the dotted lines, will the transistor sizings ( $W/L$ ) shown in Figure 2 result in a working circuit? Justify your answer.