EEC 216 Lecture #9:
Energy Recovery Circuits

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Outline

- **Announcements**
- Wrap Up: Low Leakage Circuits
- Review: Energy Dissipation
- Adiabatic Charging
- Energy Recovery Circuit Basics
- Dynamic Energy Recovery Logic
- Power and Clock Waveform Generation

Announcements

- **Design Project 2 due next Friday, February 29**
- **Typo: “minimum delay” should be “minimum energy”**
- **Extra Office Hours: Wednesday, 2/27, 1-3 PM**
- **Final Projects: start thinking about them!**

Suggested Final Projects

- **Circuits Topics**
  1. Low power modulated or low-swing interconnect
  2. Self-timed and asynchronous circuits for low power
  3. Asymmetric blip circuit for pulse-based registers
  4. Multiple-threshold logic design
  5. Circuits for closed-loop energy harvesting
  6. Low leakage memory techniques
  7. Low-swing, dual-edge triggered flip-flops

Suggested Final Projects

- **Architecture Topics**
  1. Quantifying energy scalability and power awareness
  2. Information theoretic and statistical power estimation
  3. Power aware instruction set design
  4. Fault-tolerance and power consumption
  5. Coding for low power
- **Miscellaneous Topics**
  1. Energy efficiency of biological computing
  2. Energy efficiency of quantum computing
  3. Fundamental energy limits of computation
  4. Power and energy density implications of molecular electronics

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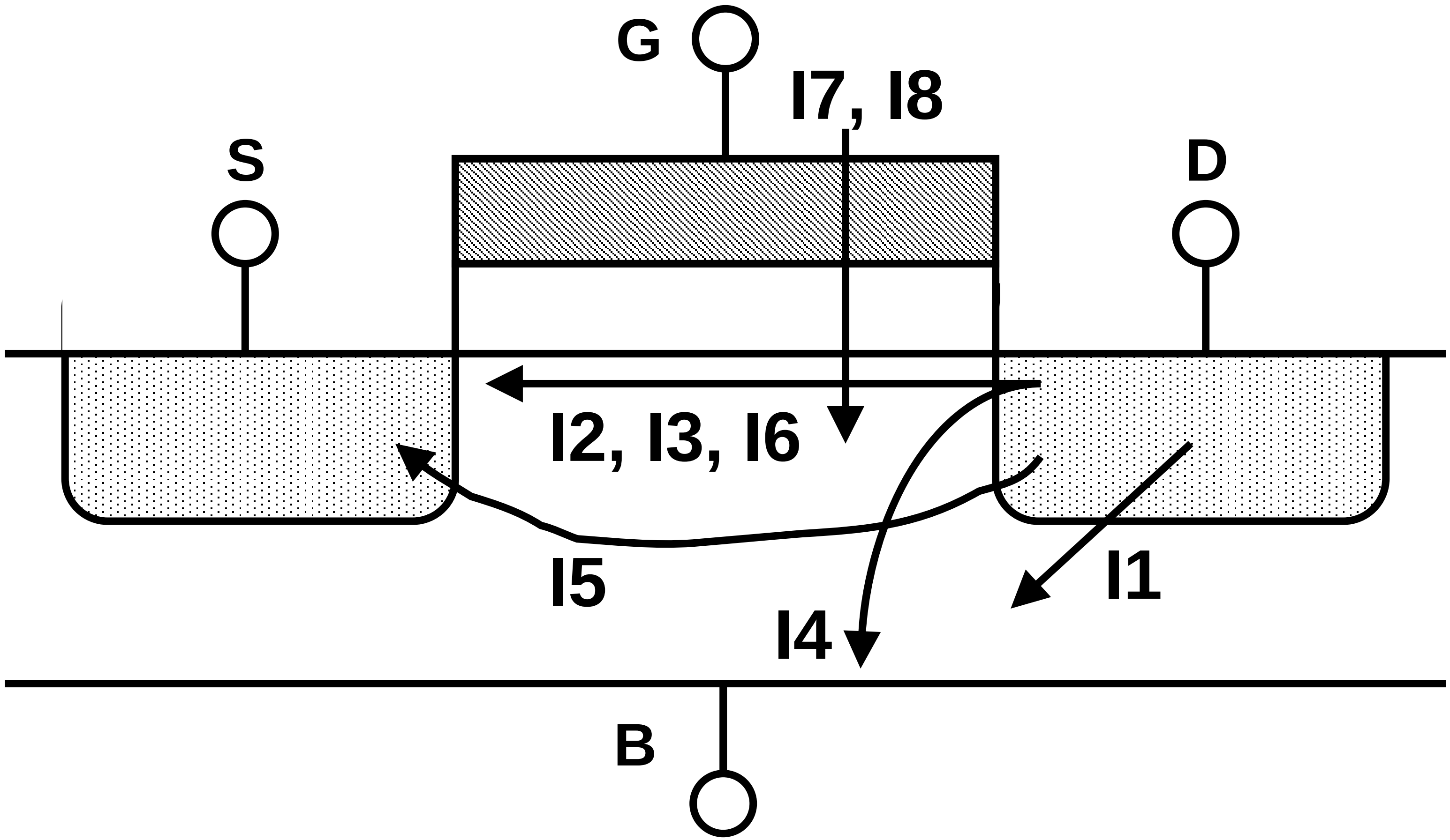
Leakage Currents in Deep Submicron



Transistor Leakage Mechanisms

1. pn Reverse Bias Current (I1)
2. Subthreshold (Weak Inversion) (I2)
3. Drain Induced Barrier Lowering (I3)
4. Gate Induced Drain Leakage (I4)
5. Punchthrough (I5)
6. Narrow Width Effect (I6)
7. Gate Oxide Tunneling (I7)
8. Hot Carrier Injection (I8)

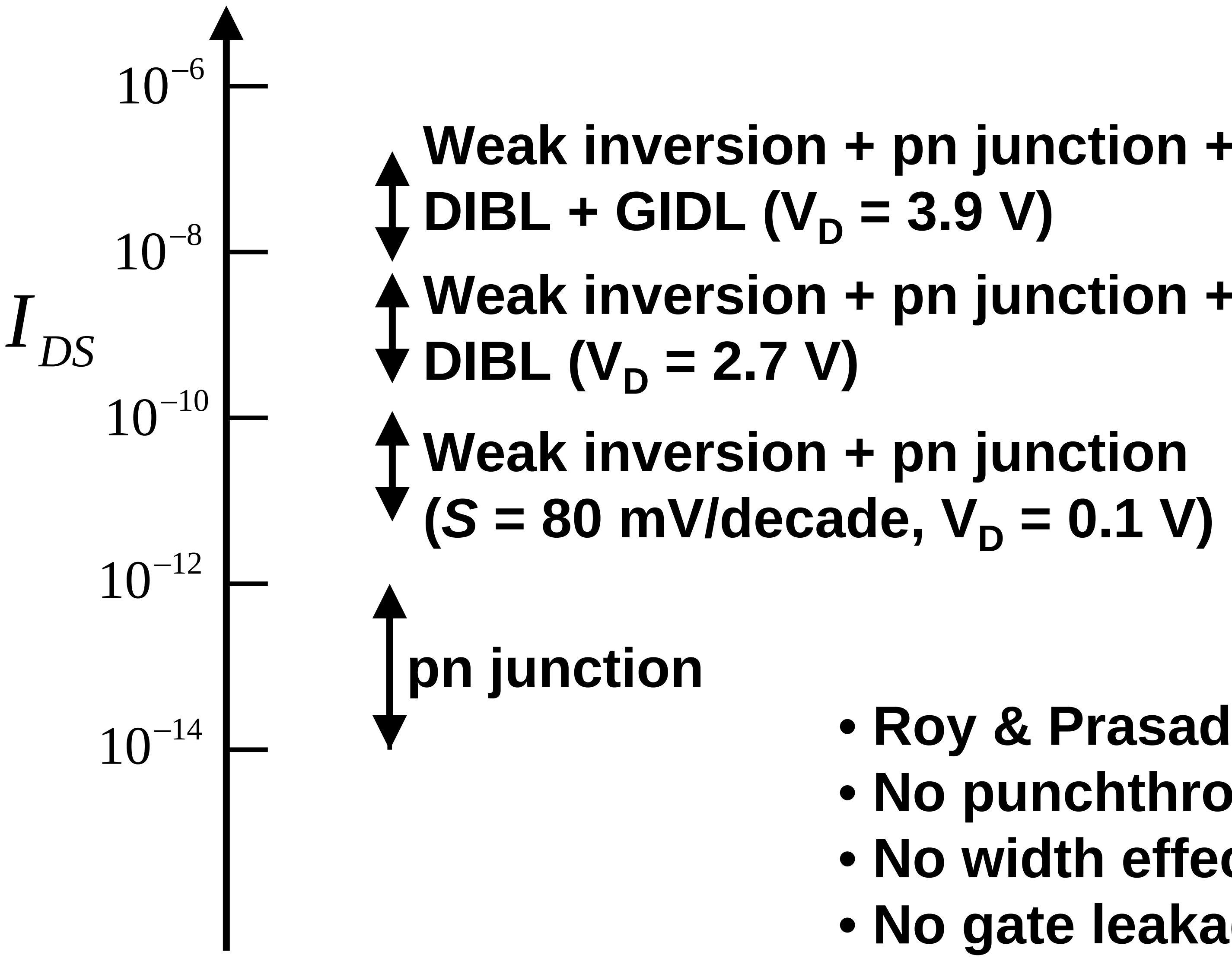
Detailed Subthreshold Current Equation

$$I_D = A \exp\left(\frac{q}{nkT}\left(V_{GS} - V_{T0} - \gamma V_S + \eta V_D\right)\right)\left(1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right)$$

$$A = \mu_0 C_{ox} \frac{W}{L}\left(\frac{kT}{q}\right)^2 e^{1.8}$$

- **V_{T0} = zero bias threshold voltage,**
- **$\mu 0$ = zero bias mobility**
- **Cox = gate oxide capacitance per unit area**
- **γ = linear body effect coefficient (small source voltage)**
- **η = DIBL coefficient**

Leakage Summary



- **Roy & Prasad, p. 219**
- **No punchthrough**
- **No width effect**
- **No gate leakage**

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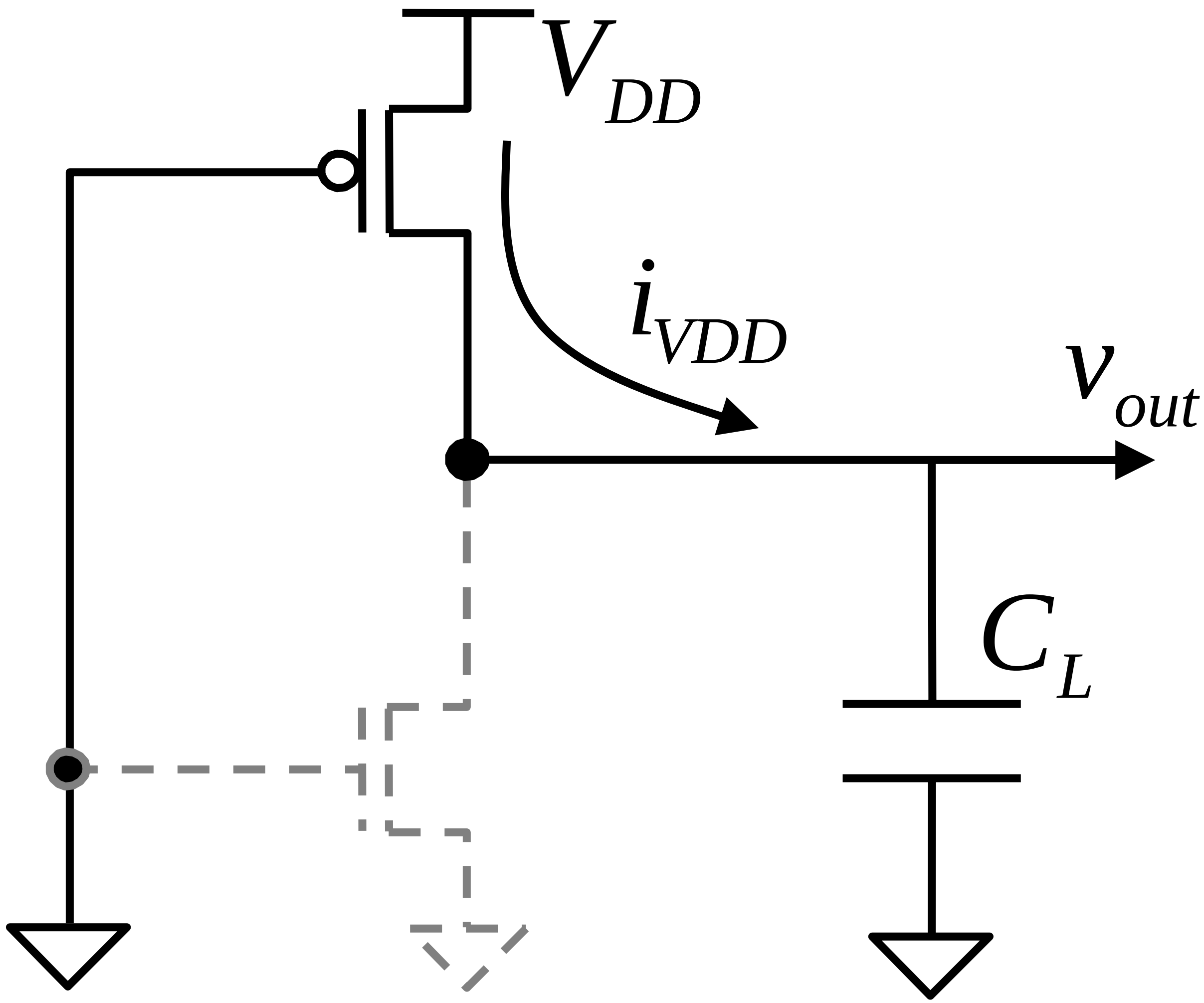
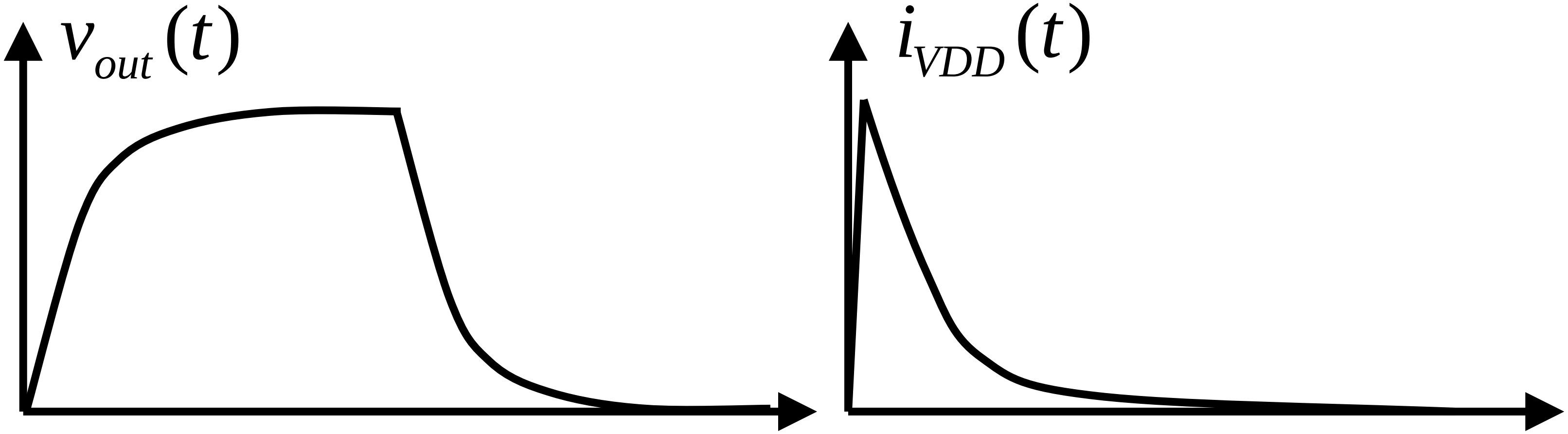
Low-to-High Transition Equivalent Circuit



Energy Drawn From Power Supply



$$E_{VDD} = \int_0^{\infty} P_{VDD}(t)dt = \int_0^{\infty} i_{VDD}(t)V_{DD}dt$$

$$= V_{DD}\int_0^{\infty} C_L \frac{dv_{out}}{dt}dt = C_L V_{DD}\int_0^{V_{DD}} dv_{out}$$

$$= C_L V_{DD}^2$$

Energy Stored on Load Capacitor

$$E_C = \int_0^{\infty} i_{VDD}(t) v_{out} dt$$

$$= \int_0^{\infty} C_L \frac{dv_{out}}{dt} v_{out} dt = C_L \int_0^{V_{DD}} v_{out} dv_{out}$$

$$= \frac{1}{2} C_L V_{DD}^2$$

- **Compared to E_{VDD}, we see that $\frac{C_L V_{DD}^2}{2}$ dissipated**
- **Same amount dissipated when capacitor discharged**
- **Independent of MOSFET resistance**

Can We Do Better on Energy?

- **Seems that $C_L V_{DD}^2$ is pretty fundamental**
  - Independent of resistance, circuit delay
- **Static CMOS logic basically configures FETs as switches connected to voltage sources**
  - Transient determined by capacitor dynamics, RC_L
- **But, suppose we use a current source to charge the capacitor instead…**

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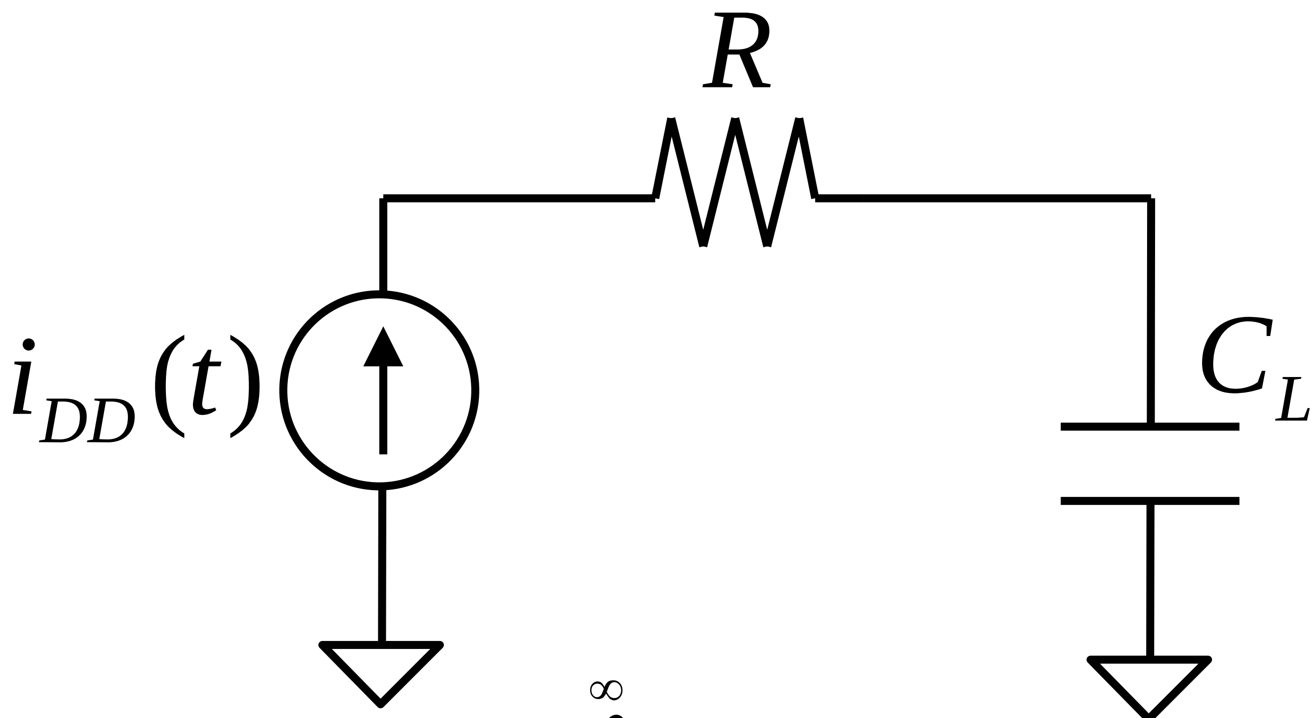
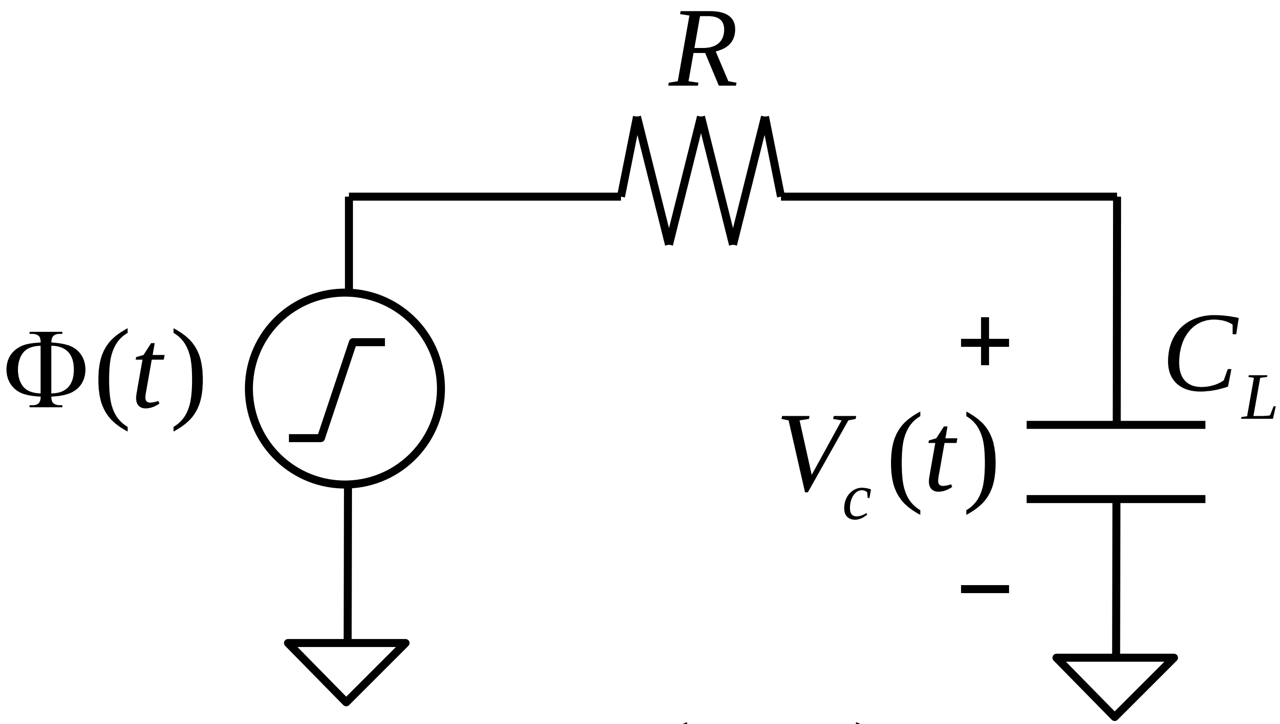
Principle of Adiabatic Charging



$$E_{IDD} = \int_0^\infty i_{DD}(t) v_{IDD}(t)\, dt$$

- **By controlling the current, we can control the voltage developed across the resistor, and reduce power consumption by charging slowly**

Adiabatic Charging Analysis



$$\Phi = RC\left(\frac{dV_c}{dt}\right) + V_c$$

- **Solve differential equation assuming input is ramp with duration T**

Input Voltage Equation

$$\Phi(t) = \begin{cases} 0 & t < 0 \\ \dfrac{V_{DD}}{T} t & 0 \le t < T \\ V_{DD} & t \ge T \end{cases}$$

- $\Phi(t)$ **ideal linear voltage ramp ending in VDD steady-state voltage**
- **Later: how to implement** $\Phi(t)$ **impacts energy dissipation and limits energy recovery efficiency**

Output Voltage Solution

$$V_c(t) = \begin{cases} 0 & t < 0 \\ \Phi - \dfrac{RC}{T} V_{DD}\left(1 - e^{-t/RC}\right) & 0 \le t < T \\ \Phi - \dfrac{RC}{T} V_{DD}\left(1 - e^{-T/RC}\right) e^{-(t-T)/RC} & t \ge T \end{cases}$$

- **Solve for instantaneous resistor power using** $V_c(t)$
- **Integrate to find dissipated energy as function of T**

Energy Dissipated With Ramp Driver

$$E_{diss} = \int_0^{\infty} i_R(t) V_R(t)\,dt = \int_0^{\infty} \frac{\left(\Phi - V_c(t)\right)^2}{R}\,dt$$

$$= \int_0^{T} \frac{\left(\Phi - V_c(t)\right)^2}{R}\,dt + \int_T^{\infty} \frac{\left(\Phi - V_c(t)\right)^2}{R}\,dt$$

$$= \frac{RC}{T} C V_{DD}^2 \left[1 - \frac{RC}{T} + \frac{RC}{T} e^{-T/RC}\right]$$

- **Consider the extreme cases of *RC* with respect to *T***

Limiting Cases of Slow and Fast Ramps

- **For very slow ramp** $T >> RC$ **:**

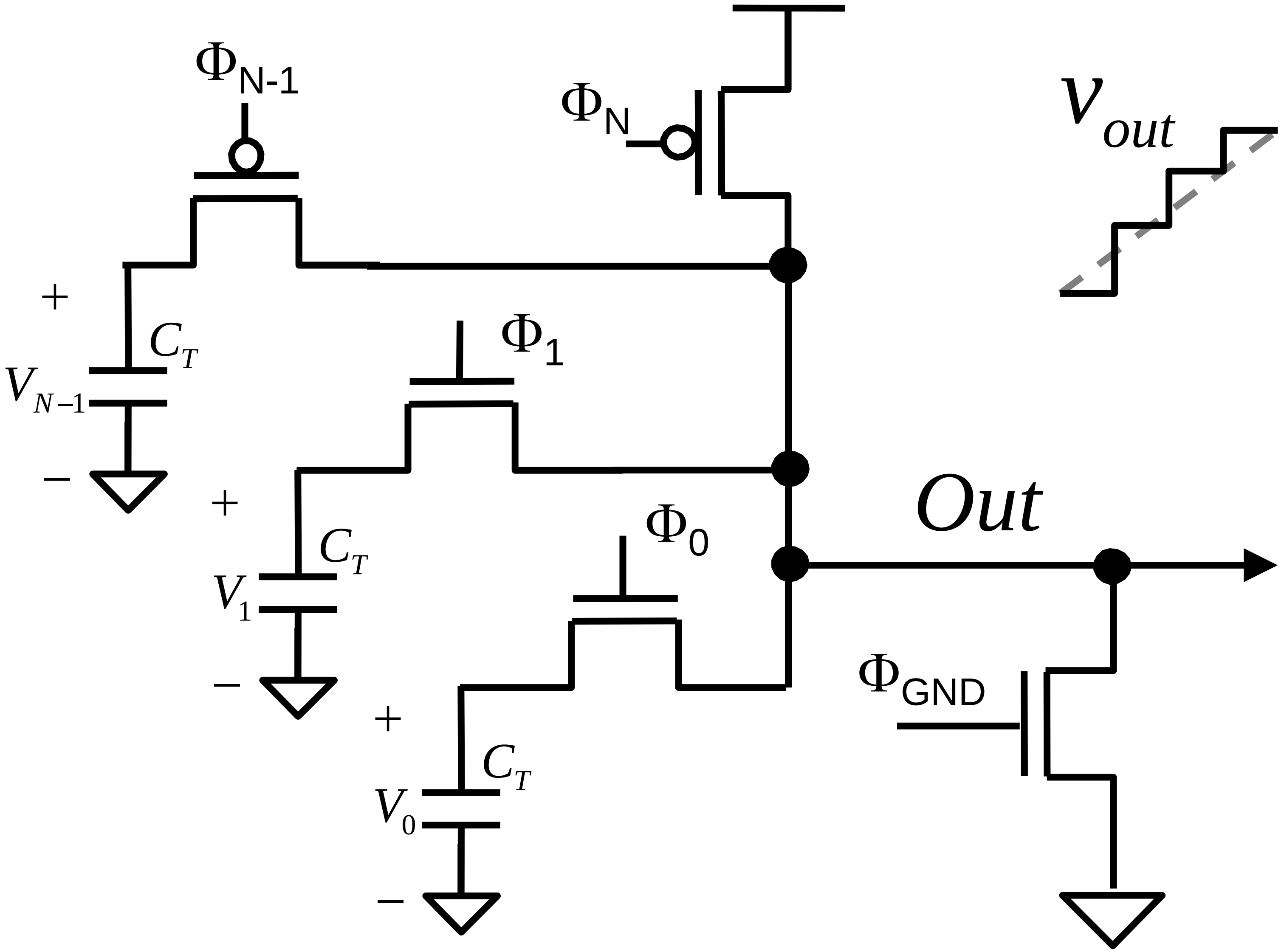
$$E_{diss} = \frac{RC}{T} CV_{DD}^2$$

- **For very fast ramp** $T << RC$ **(original CMOS case):**

$$E_{diss} = \frac{1}{2} CV_{DD}^2$$

- **Energy dissipation can be made arbitrarily small by making transition time *T* arbitrarily long**

Example Voltage Ramp: Stepwise Charging



Stepwise Charger Operation

- **Basic idea: charge large capacitance in small incremental steps**
  - Voltage swing between steps small, so small power dissipation between intermediate voltage levels
  - Falls off quadratically with number of levels *N*
  - *N* steps required, so total dissipation for entire transition goes as 1 / *N*

$$P = f\,C_L \sum_{k=1}^{N} \left(\frac{V_{DD}}{N} \right)^2$$

$$= C_L \frac{V_{DD}^2}{N} f$$

Adiabatic Switching Intuition

- **Power dissipated when current flows across potential (voltage difference)**
  - Voltage difference between nodes kept small, so small power dissipation as node transitions
  - Slow voltage transition on capacitor implies low currents flowing, so low voltages developed on parasitic resistances
- **Inherent energy and speed tradeoff**
  - Long transitions imply slower operation but less energy dissipation
  - Independent of supply scaling unlike dynamic power for traditional CMOS circuits

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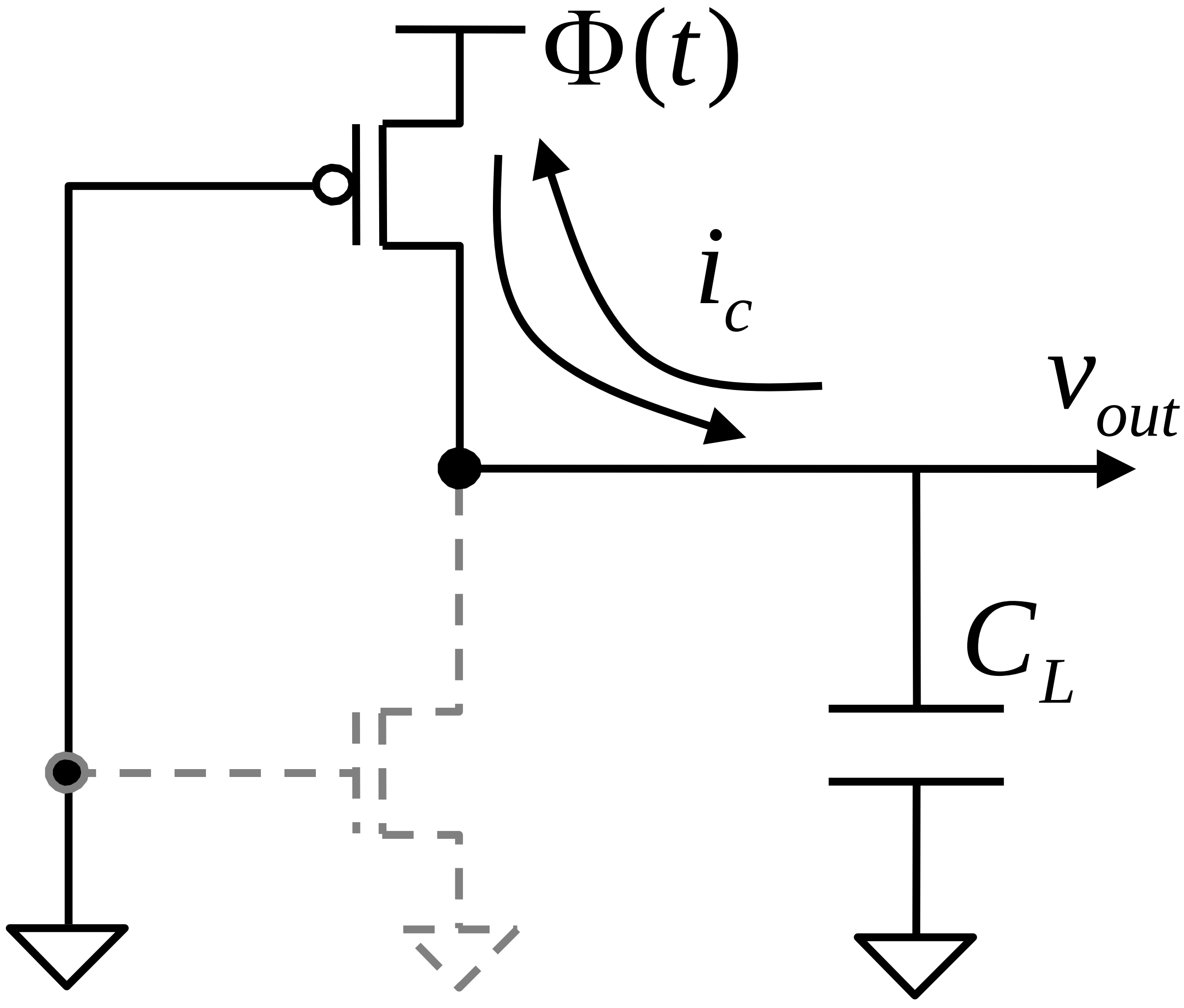
Energy Recovery Basics

- **Energy stored by placing charge on capacitive circuit nodes**
  - Would like to recover that energy and return it to power supply for use again
  - Adiabatic charging and discharging minimizes losses as charge moved to and from power supply
- **Energy recovery vs. adiabatic charging**
  - Terms sometimes confused in literature
  - *Adiabatic charging* refers to slow (thermodynamically reversible) movement of charge across vanishingly small voltages for minimal power dissipation
  - *Energy (charge) recovery* means moving charge back and forth from a power supply or charge reservoir

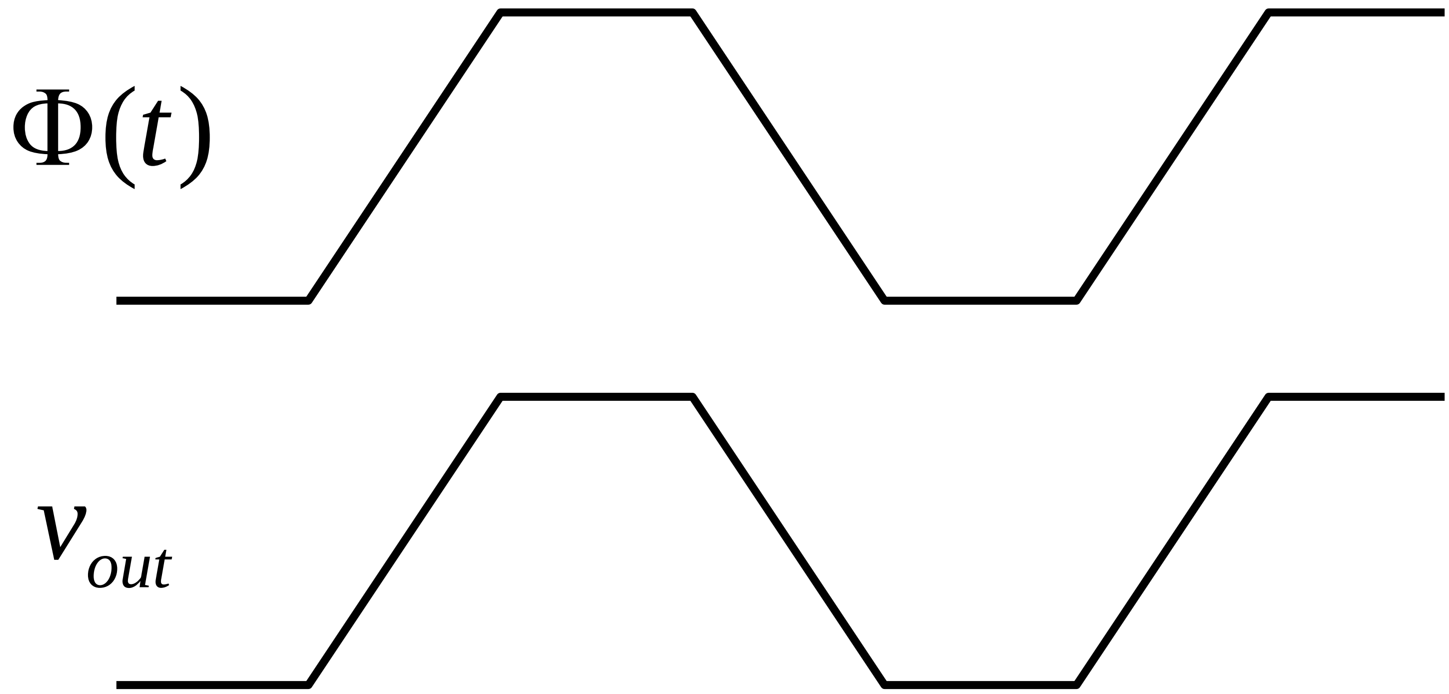
Energy Recovery Process



Energy Recovery Timing Phases

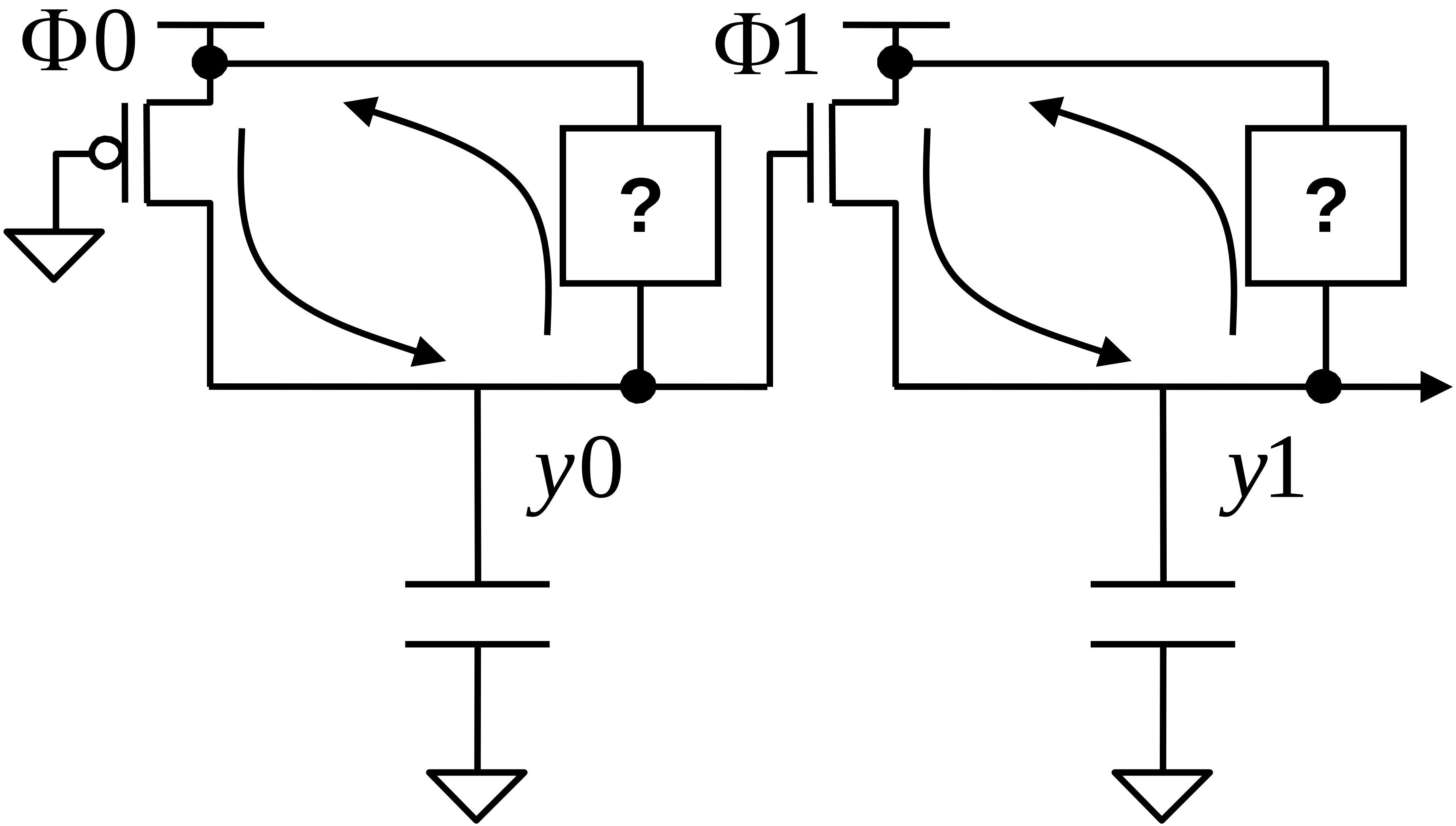
- **Similar to dynamic logic or level sensitive (latch-based) clocking, except power supply is also the clock signal**
- **Four phases of operation**
  - *Idle Phase*: (Φ = 0) Circuit state before evaluation
  - *Evaluation Phase*: (Φ transitions from 0 V to V_{DD}) Circuit nodes evaluate to final value
  - *Hold Phase*: ($\Phi = V_{DD}$) Circuit nodes maintain state after evaluation
  - *Restoration Phase*: (Φ transitions from V_{DD} to 0 V) Circuit nodes restored to initial value

Energy Recovery Process Timing

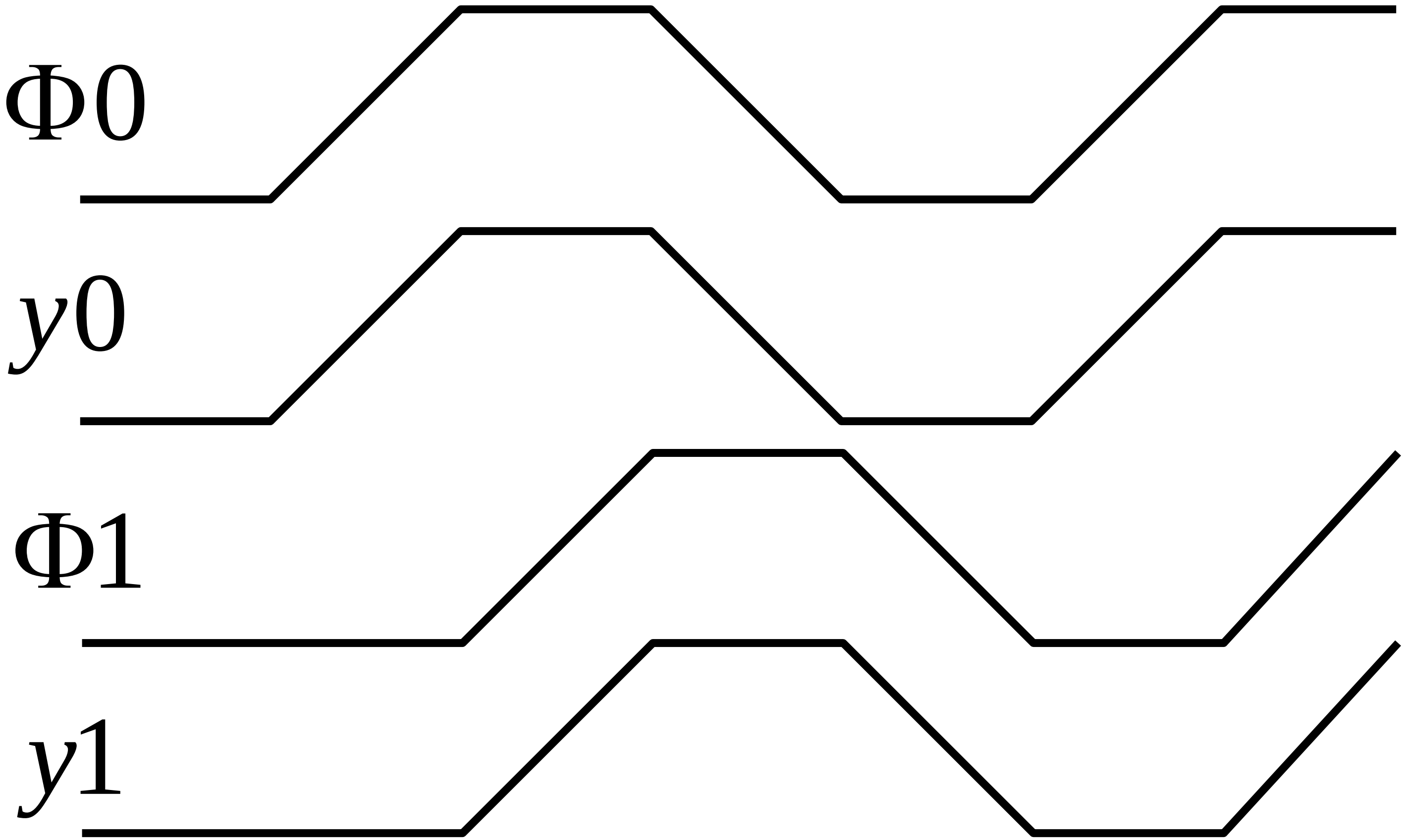


- **Want output voltage to transition slowly with power/clock waveform**
- **How do we cascade logic stages?**

Cascading Energy Recovery Stages



Cascaded Logic Energy Recovery Timing

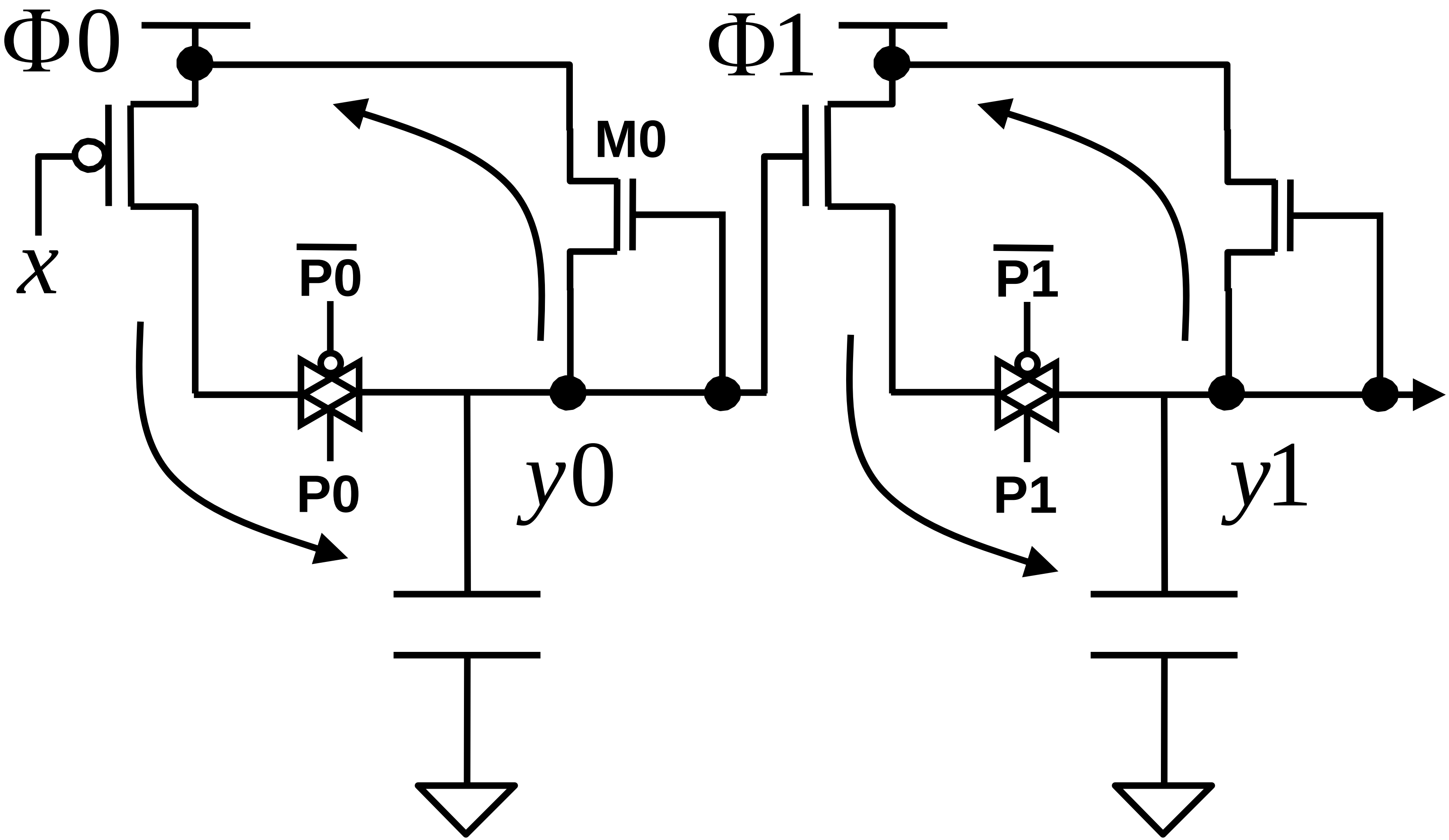


- **Charge nth stage nodes and then discharge (n-1)th stage nodes**
- **How do we implement the energy recovery phase?**

Cascaded Logic Timing Issues

- **Must isolate input from output node**
  - Otherwise inputs cannot change until output has been sampled by succeeding stage
  - Constraint ripples to end of logic pipeline, i.e. no input can change until final stage evaluates
- **Isolation requires an alternative path (? Box) for reverse current flow for energy recovery**
  - Reverse path must be controlled by gate output
  - If y0 = 1, then must discharge y0 slowly using $\Phi 0$ (returning charge to power supply)
  - If y0 = 0, reverse path must be open circuit to prevent leakage from $\Phi 0$ contaminating output y0

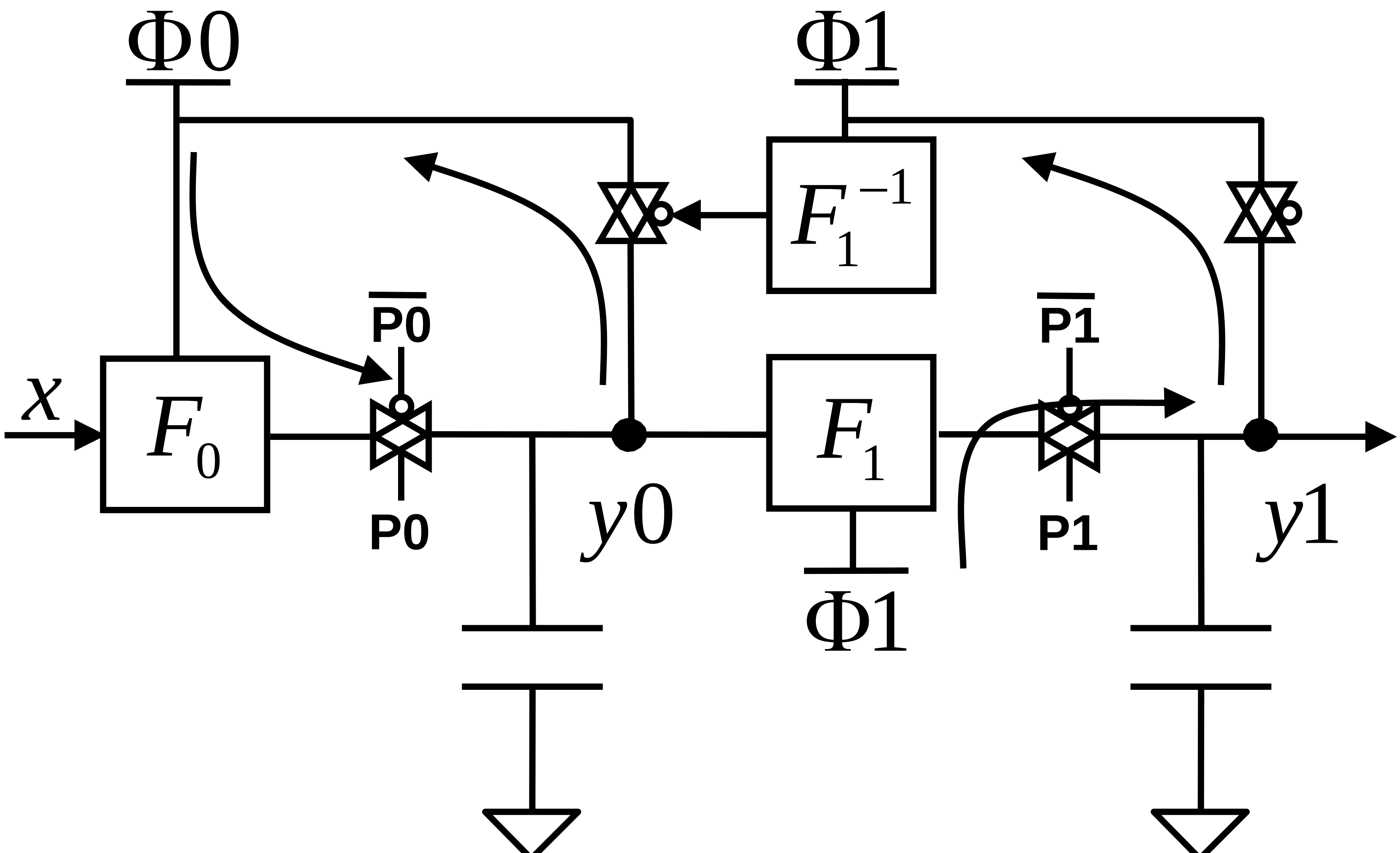
Self-Controlled Energy Recovery



Self-Controlled Recovery Issues

- **Use full transmission gates to isolate outputs**
- **Diode connect FETs between output and clock / power node provide reverse current path for energy recovery**
  - Simple to implement with low area overhead
  - Control signal varying with output voltage transition
  - Requires V_{TH} voltage drop to forward bias diode M0, increasing power dissipation
- **Would like recovery path control signal to maintain state throughout restoration phase**
- **Alternative: use succeeding stage output to compute control**

Next Stage Controlled Energy Recovery

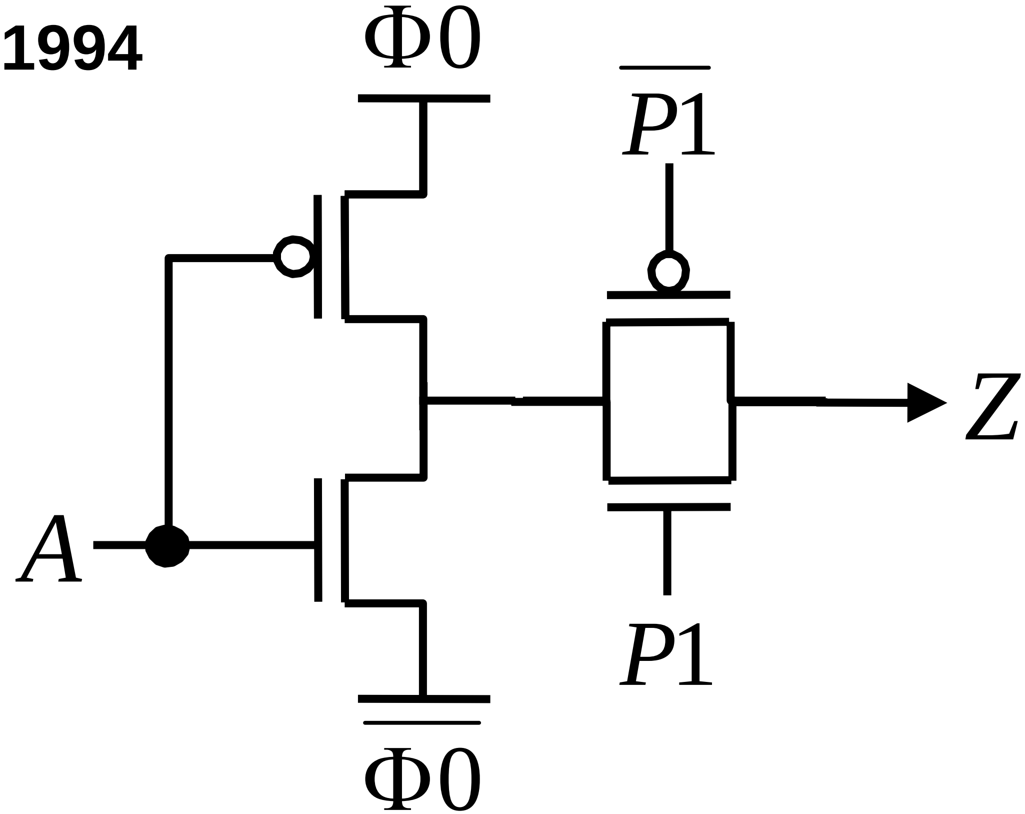


Next Stage Controlled Recovery Issues

- **Control signal for energy recovery path generated from succeeding stage output**
  - Requires computing inverse function of nth stage to reproduce state of (n-1)th stage output
  - Full pass gate isolation means that control signal held constant during full restoration phase transition
- **Overhead for this logic style can be high**
  - Computing inverse could be even more area intensive than computing desired function
- **True physically and logically reversible computation**
  - Pass gate reverse current path has little loss, adiabatic transition
  - Style results in minimum overall energy dissipation

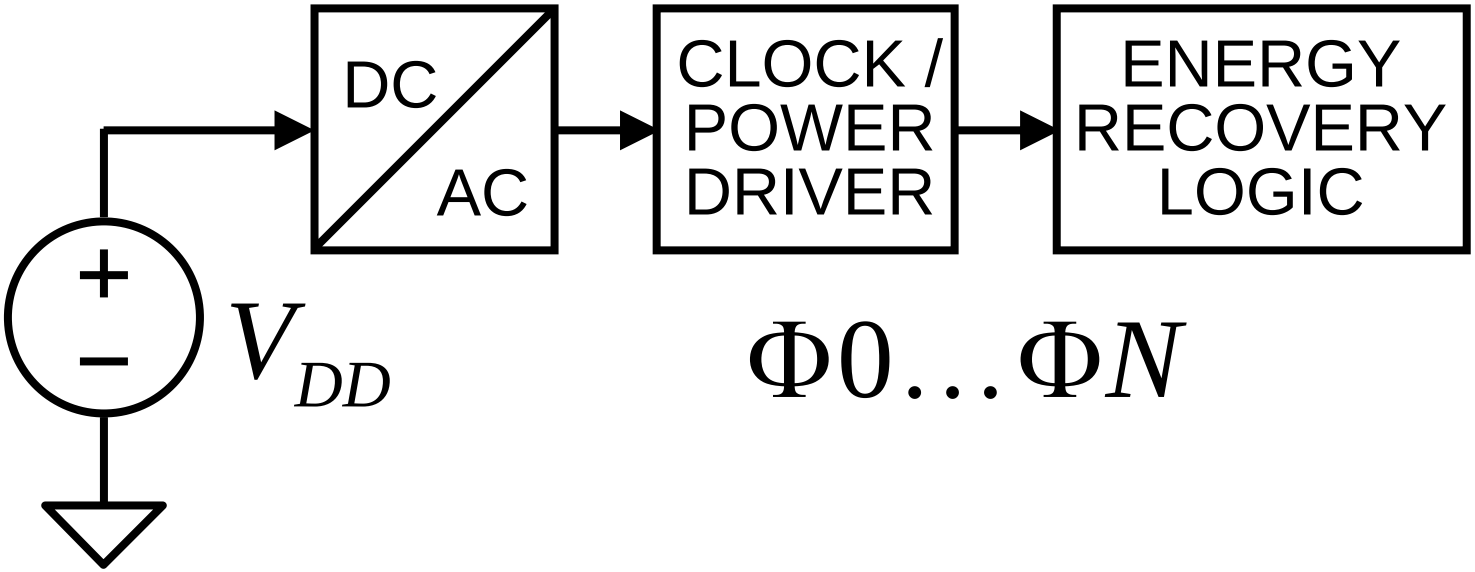
Example: Split-Level Charge Recovery Logic

- **Younis 1994**



- **Uses rails which split up and down from half V_{DD} rather than single rail ramping from 0V to V_{DD}**
- **Can use many clock phases to build pipeline**

Energy Recovery System Block Diagram



- **Use circuits to generate power / clock waveforms**
- **Generators must use as little power as possible**
  - Resonant RLC circuits often used in these applications
  - Minimize parasitic losses in power / clock generator

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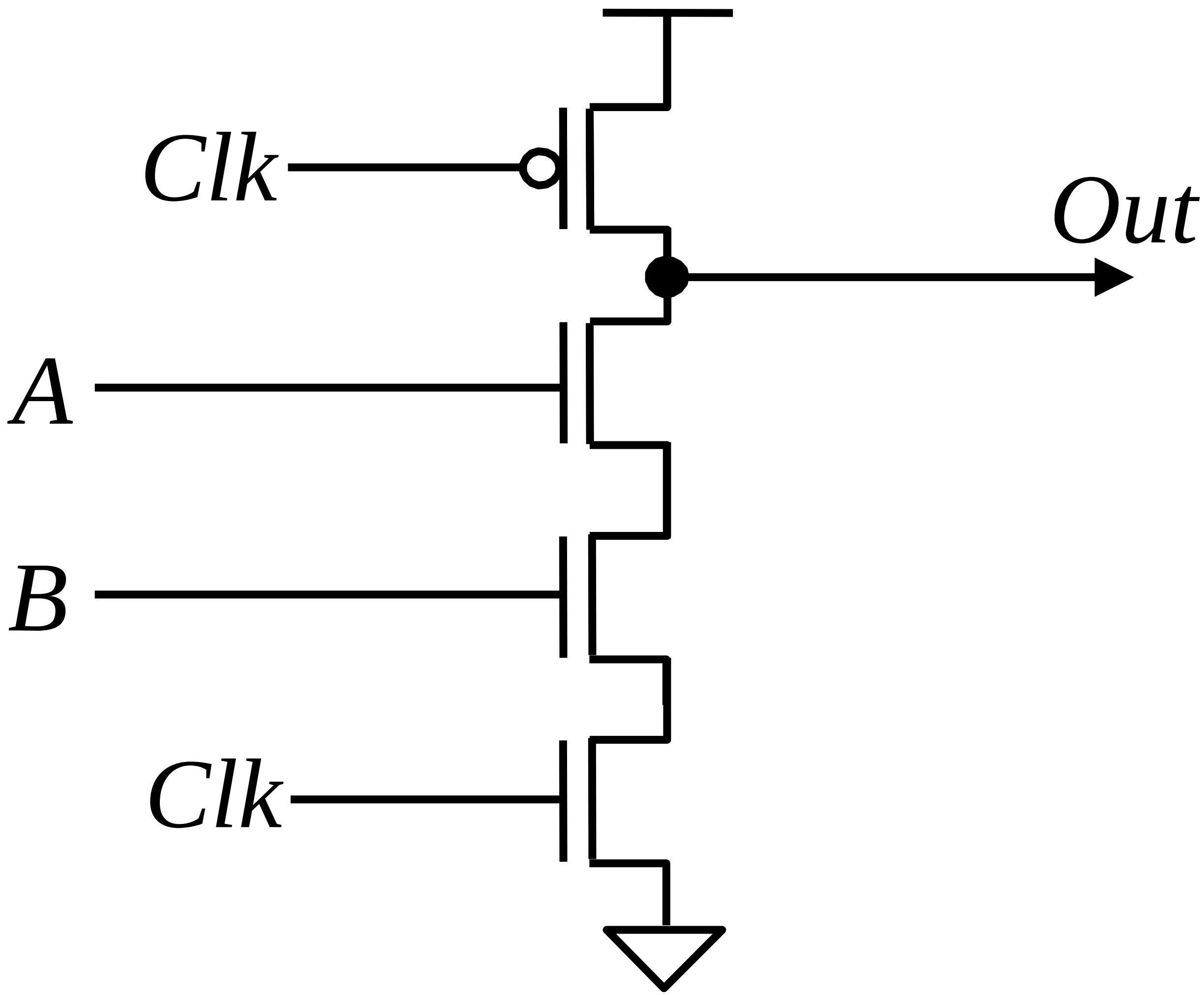
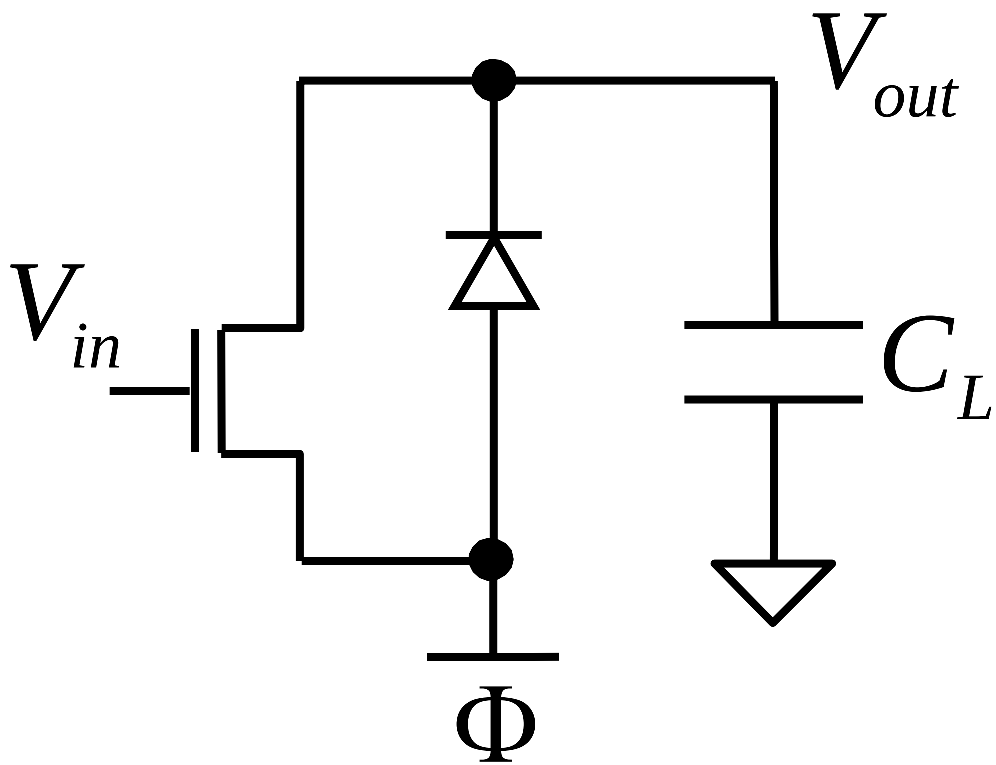
Dynamic CMOS Two-Input NAND Gate



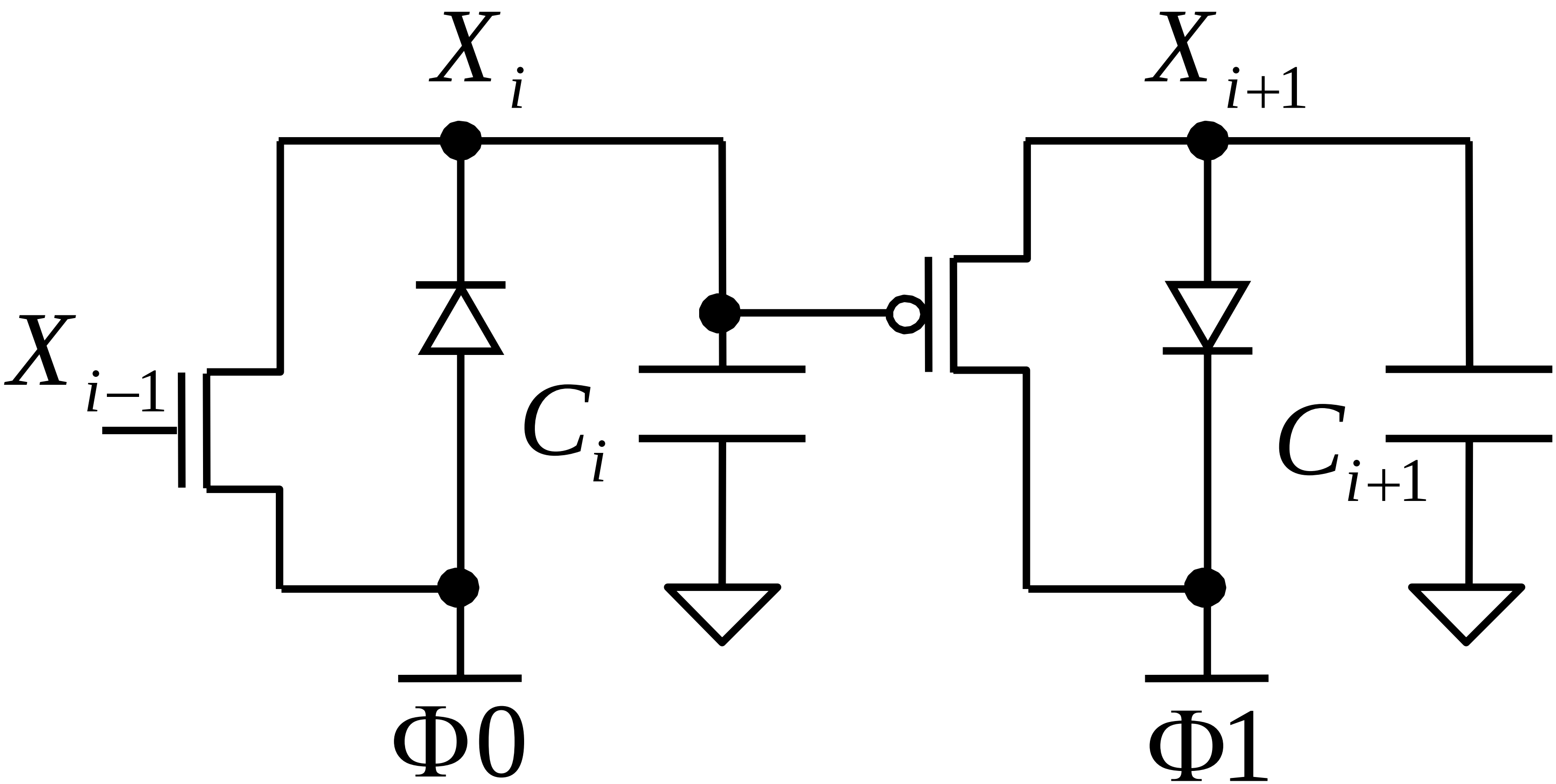
- **PMOS precharges (Clk low), NMOS evaluates (Clk high)**

Adiabatic Dynamic Logic (ADL) Inverter



- **Precharge Phase: Φ0 is long voltage ramp from 0V to V_{DD} charging V_{out} to V_{DD}- V_{diode}**
- **Evaluate Phase: Φ0 swings slowly low, discharging if input is high otherwise leaving output high**

Cascading Adiabatic Dynamic Logic Gates

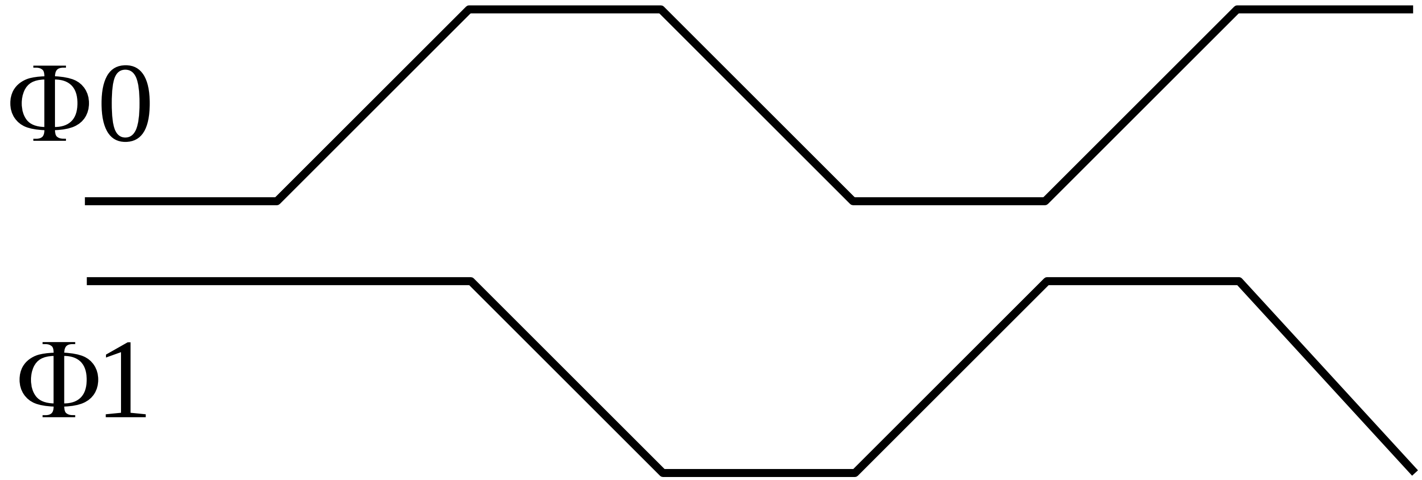


- **Similar to NP-CMOS design style: cascade N-blocks with P-blocks**

Adiabatic Dynamic Logic Design Issues

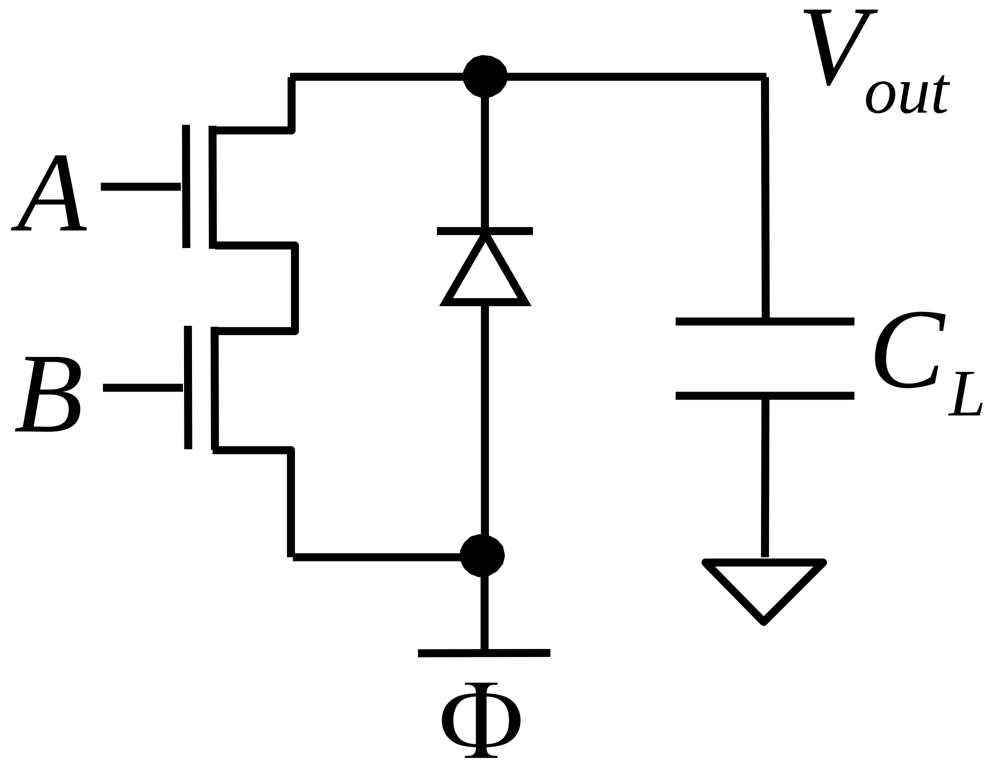
- **Clocking methodology similar to all adiabatic designs: four phases required**
  - Clocks for consecutive stages must be synchronized such that when the output of first stage is latched (*hold* phase) the second stage starts *evaluate* phase
  - When first stage is evaluating, must ensure no non-adiabatic transitions in second stage
- **Output voltages must be precharged high (low) enough to guarantee correct operation**
  - Reduces to guaranteeing diode drop is significantly less than FET threshold voltage ($V_{diode} < V_{TH}$)
  - Alternative is to add DC offset to power / clock voltages to compensate for diode drop

Cascaded Adiabatic Dynamic Logic Timing



- **Consecutive stages have opposite clock polarities**
  - Similar to NP-CMOS dynamic logic clocking
- **Four phases are actually necessary**
  - In this example, stage clocked by $\Phi 2$ evaluates while $\Phi 1$ holds and $\Phi 0$ restores
- **Feedback must occur every four stages for consistent timing (every 4th stage in same phase)**

Adiabatic Dynamic Logic NAND2



- **Complex ADL gate design similar to dynamic CMOS logic design:**
  - Implement arbitrary pulldown network with a diode in parallel

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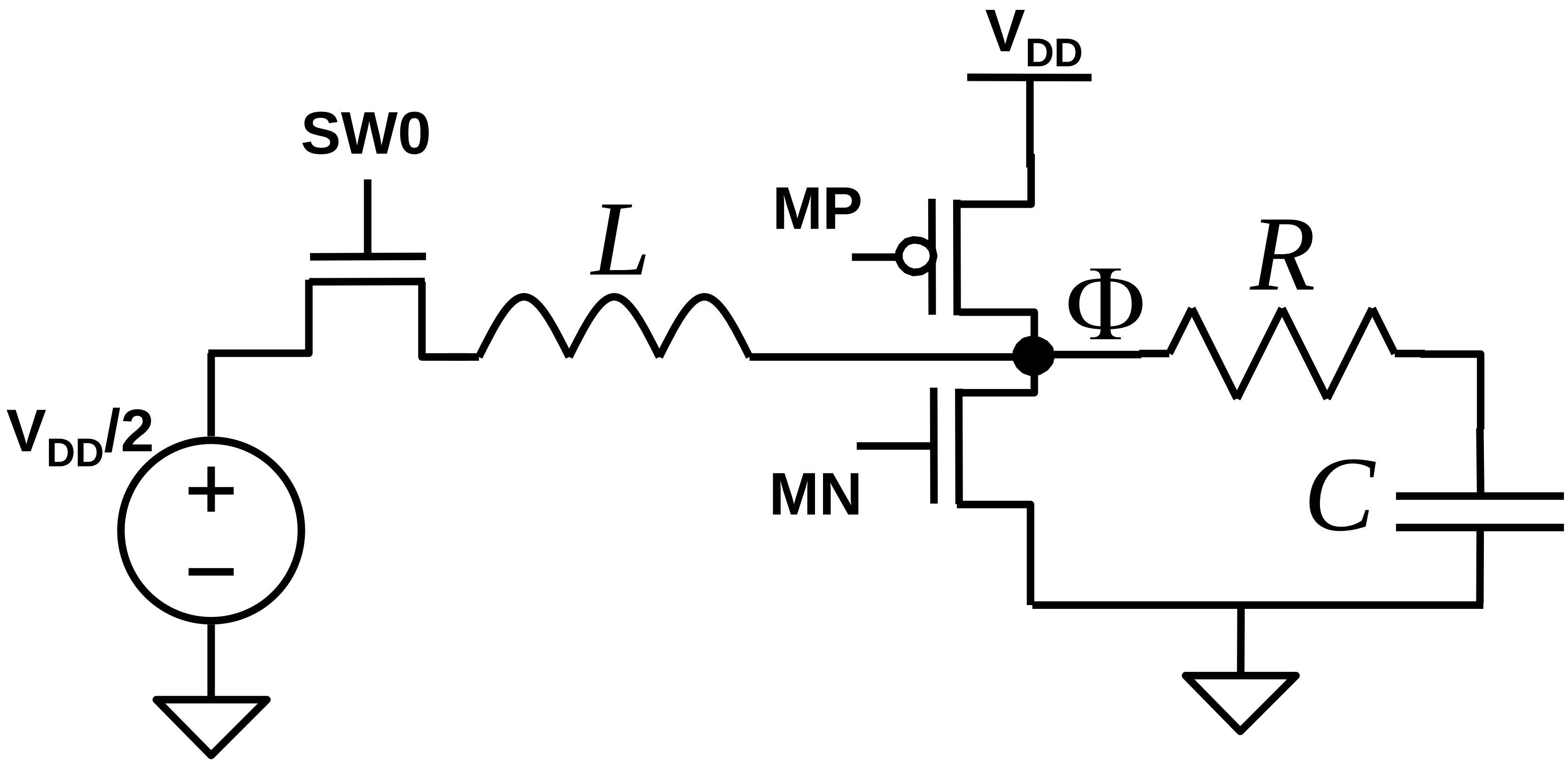
Supply Clock Generation Goals

- **Energy recovery logic requires efficient power / clock waveform generation**
  - Should operate with high efficiency (low loss) at high frequency
  - Must create long rise and fall times for adiabatic charging of capacitive circuit nodes
  - Must be able to deliver and receive charge to recover energy
- **Stepwise driver incorporates too many losses to satisfy these requirements well**
- **Most approaches use an RLC resonant circuit**
  - Sinusoidal slope approximates linear ramp
  - Energy moved between capacitive nodes and inductor

Basic Resonant Clock Generator



- SW0 closes, Φ rings up to V_{DD} or down to ground
- MP or MN turns on to hold Φ at steady state
- ***RC*** **models clock net,** ***L*** **chosen to set frequency**

Problems With Basic Generator

- **Series connected switch SW0 has finite resistance**
  - Loss dramatically decreases energy efficiency
- **Control signals for MP and MN must be generated by extra circuitry**
- **Additional voltage reference $V_{DD}/2$ required**
- **Energy dissipated in driving gates of SW0, MP, and MN decreases efficiency**
  - Devices must be large to not put too much series resistance in power supply network
- **Generates single phase clock**
  - Multiple clock phases require multiple generators

Half Blip Circuit Operation

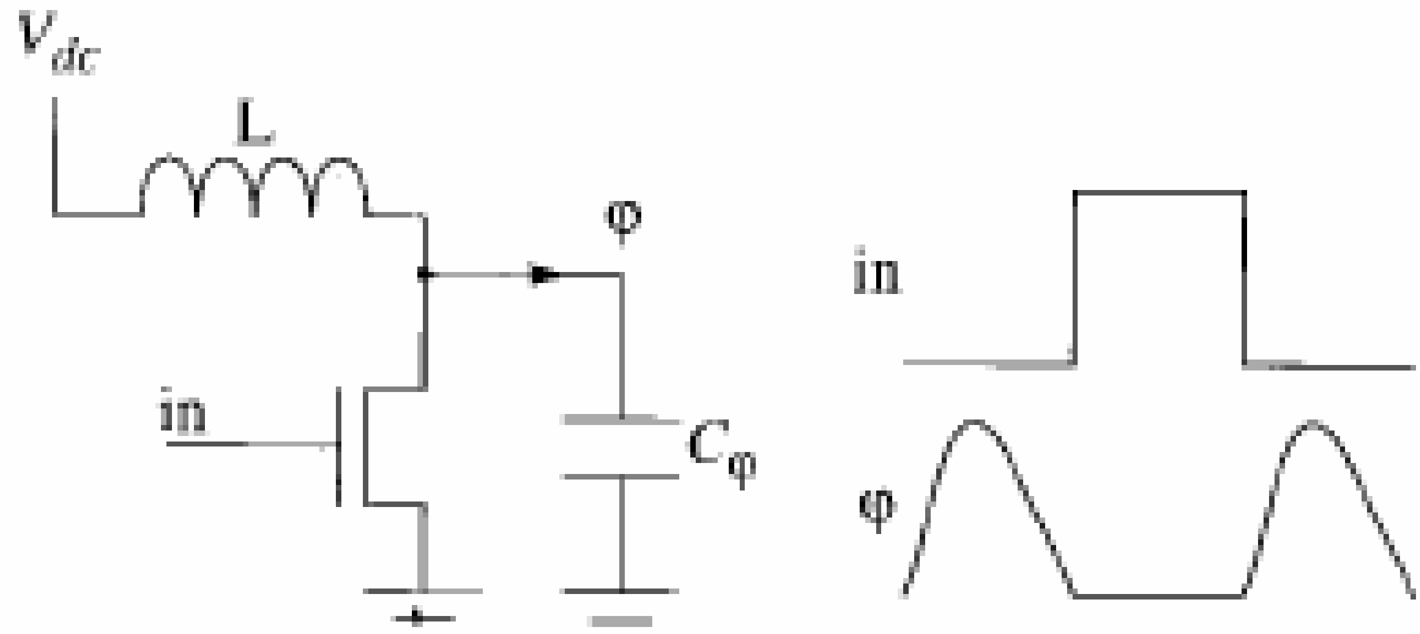
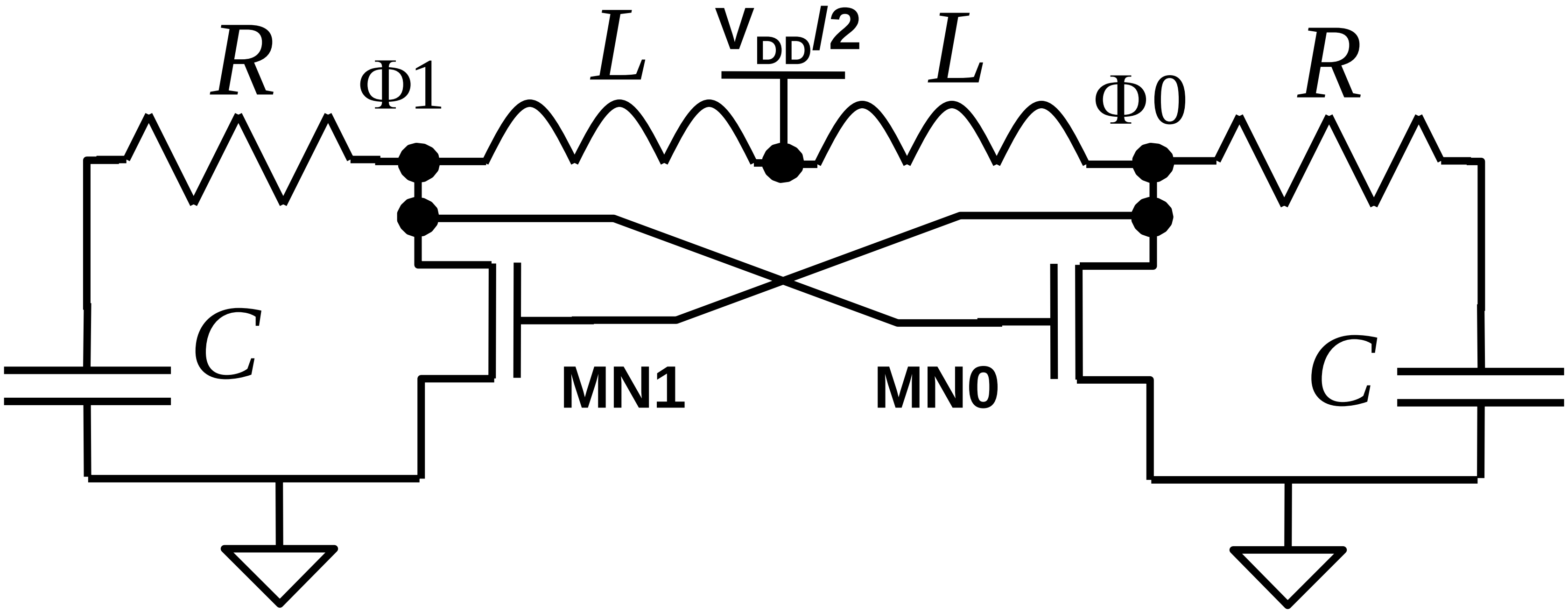


Fig. 1. A single-rail resonant clock driver.

- **Alternative topology for a single rail resonant driver**
- **Eliminates series losses since reset NMOS in parallel**
- **Athas et al., JSSC 97**

Original Blip Circuit



- **Transistors MN0 and MN1 restore energy to oscillator dissipated by lossy elements**
- **Generates two almost nonoverlapping clock phases**
- **Gates are also driven resonantly by circuit**

Full Blip Circuit Operation

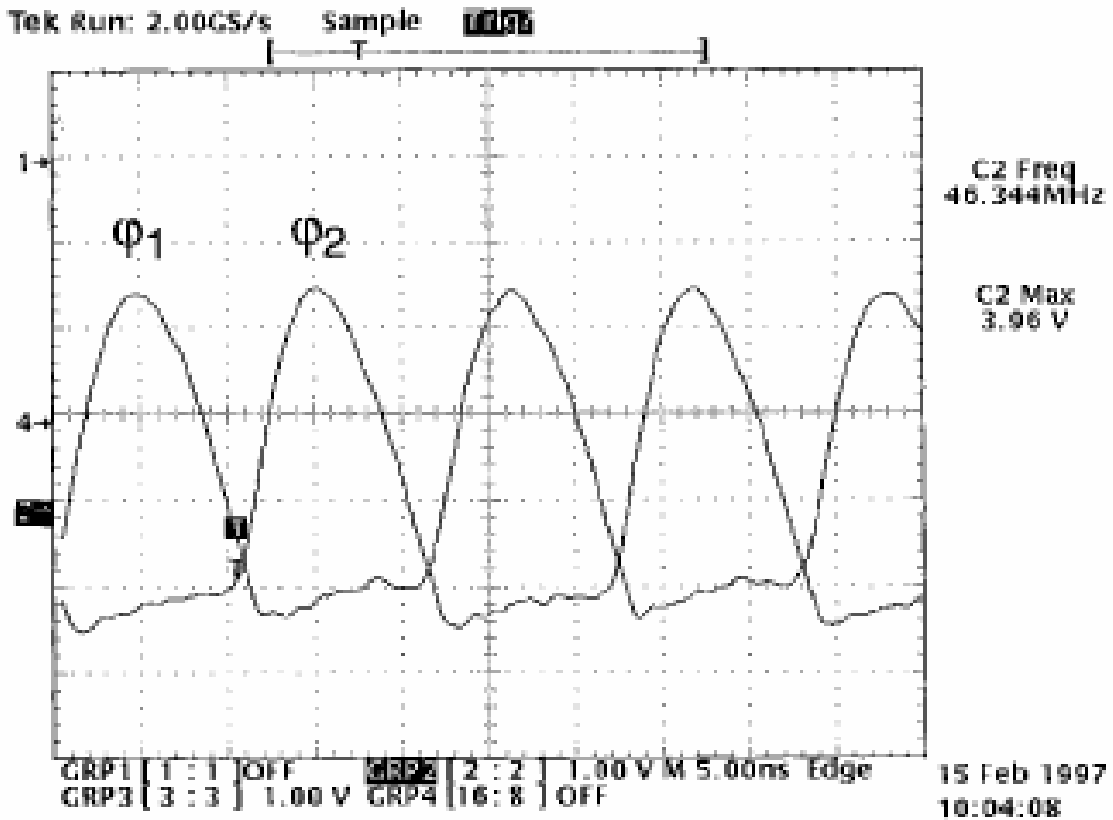


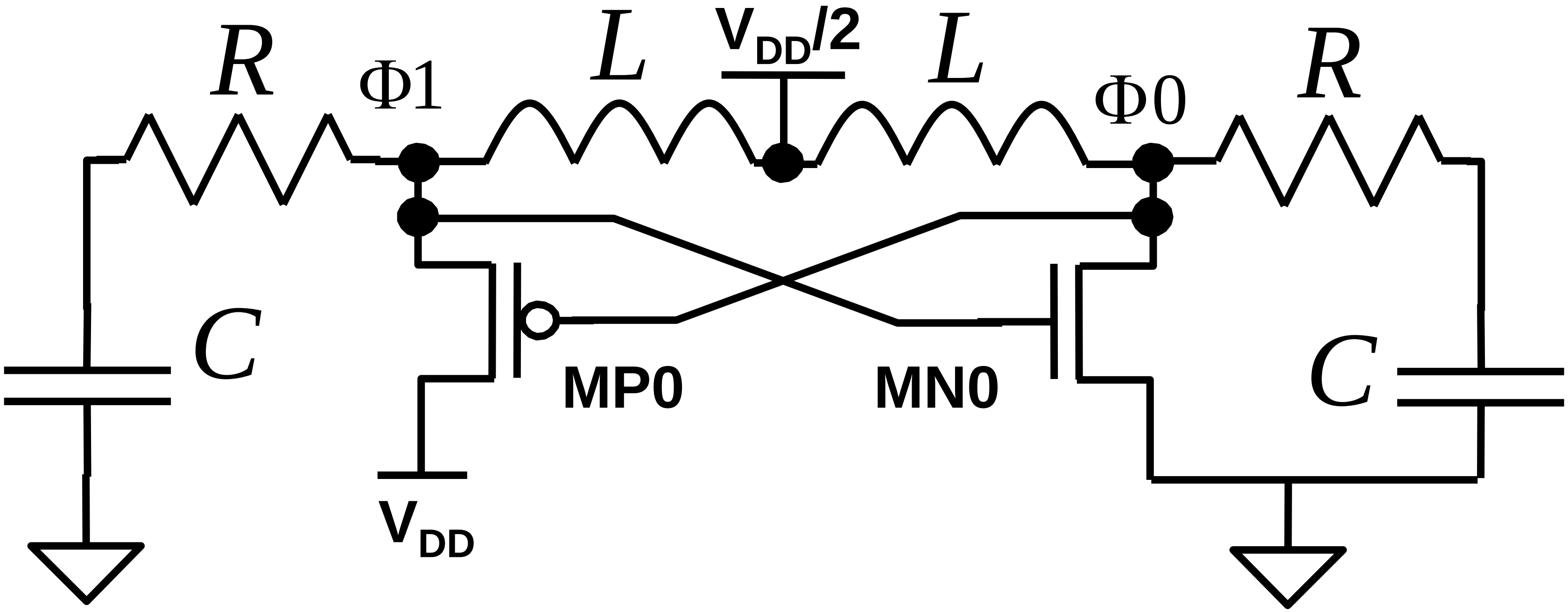
Fig. 3. Scope trace of the *almost*-nonoverlapping two-phase clock waveforms of AC-1's blip circuit.

- **Nonoverlapping clock generation measured traces**
- **Athas et al., JSSC 97**

Blip Circuit Issues

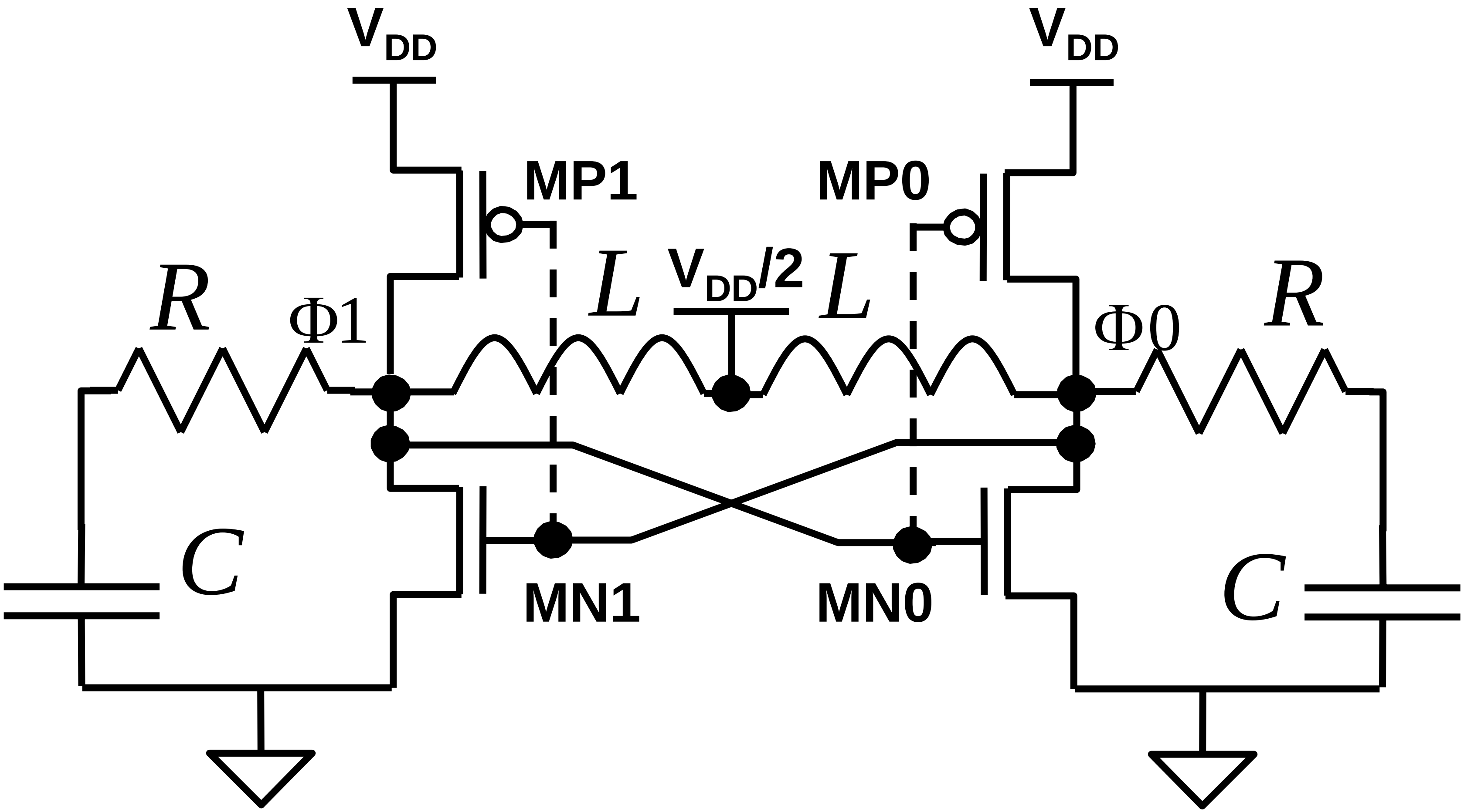
- **Nonsinusoidal "blip" waveforms produced since there are no pullup paths**
  - Sinusoidal waveform has highest energy recycling efficiency for a resonant circuit
  - Energy recovery is most efficient at fundamental frequency
  - Energy in higher order harmonics almost totally lost
- **Two inductors and half V_{DD} reference required for the basic circuit**

Blip Circuit Variation 1



- **PMOS pullup MP0 used in one branch of circuit**
- **Generates closer to sinusoidal output for better energy efficiency**
- **PMOS must be sized larger for same resistance, more loss when driving MP0 gate**

Blip Circuit Variation 2



- Pullup and pulldown devices used to restore energy
- Short circuit power an issue when both are on

Other Blip Circuit Variations

- **Control PMOS and NMOS gates separately**
  - Careful rise and fall time management of control signals improves efficiency, creates mostly sinusoidal output
  - Never on simultaneously so no short circuit power
  - Requires PLL to align control signals properly in time, whereas blip circuit control was fully self-timed
  - Control device gates not driven resonantly so additional power dissipation there
- **Other supply clock schemes proposed including using MEMS switches, MEMS resonators, etc.**

Mixing Energy Recovery and Standard Logic

- **Can apply energy recovery selectively to design**
- **Most useful for high capacitance nodes like clocks, enables, memory word lines and bit lines, other global signals**
- **Get some power benefits without overhead of circuit reversibility, especially for simple functions like clocks**
- **Decreased time for circuit redesign**
- **Requires careful interfacing between energy recovery and traditional circuit styles to guarantee correct operation**

AC-1 Microprocessor Example

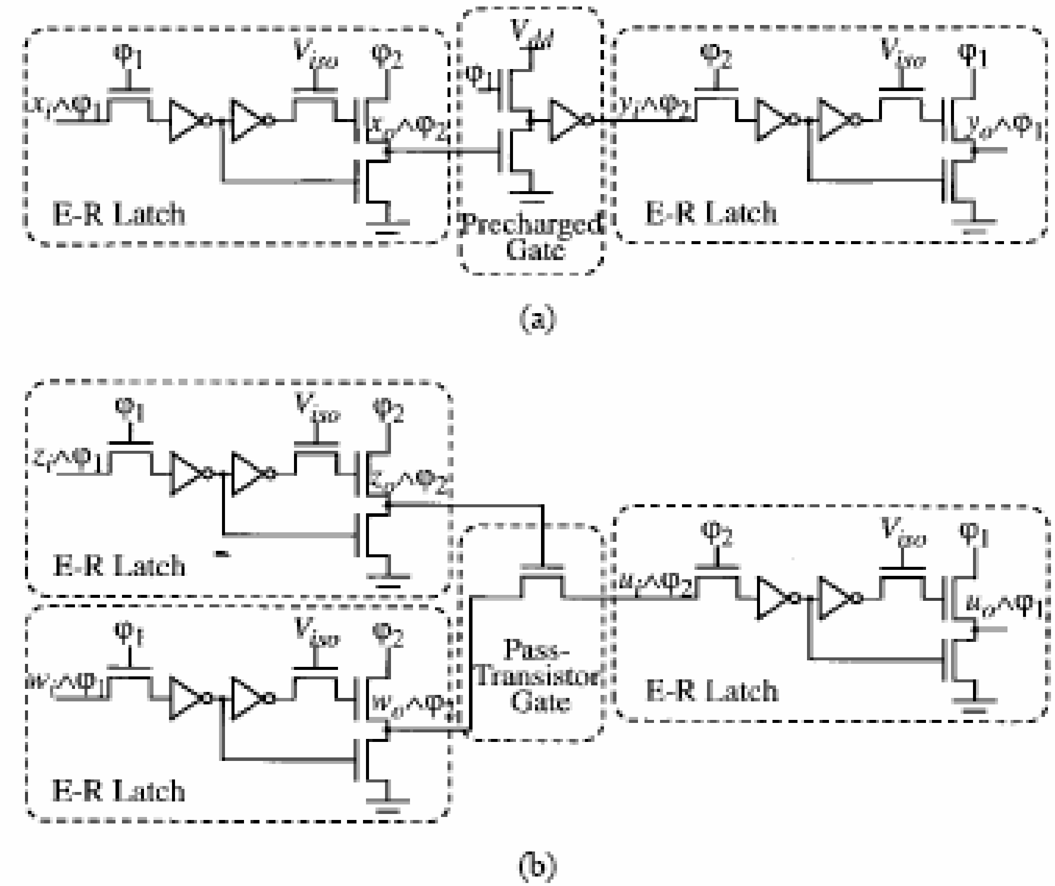


Fig. 9. E-R latches used with (a) precharged logic and (b) pass-transistor logic.

- **Used energy recovery latches with traditional logic**
- **Athas et al., JSSC 97**

Energy Recovery Logic Summary

- **Adiabatic charging and energy recovery can result in asymptotically zero energy dissipation**
  - Requires operation to be arbitrarily slow
  - Not all applications amenable to very low frequency operation
- **Diode based approaches dissipate more power**
  - Finite forward biased diode drops inherently burn power
  - Full transmission gate circuits are better from power perspective
- **Leakage power currently limits usefulness**
  - Energy recovery techniques apply to dynamic power only, if leakage dominates then not much gain
  - Active research to address these concerns