EEC 216 Lecture #8A: Subthreshold Circuit Design

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Outline

• Announcements
• Review: Low Power Interconnect
• Finish Lecture 7
• Leakage Mechanisms
• Circuit Styles for Low Leakage
• Cache SRAM Design Examples
• Next Time: Energy Recovery Circuits
Announcements

• Design Project 2 due February 29, 5 PM in 3173 Kemper Hall
Extremely Brief MOSFET Review

Saturation:  \[ I_D = \frac{\mu C_{ox} W}{2L} \left( V_{GS} - V_T \right)^2 \left( 1 + \lambda V_{DS} \right) \]

Triode:  \[ I_D = \mu C_{ox} \frac{W}{L} \left( \left( V_{GS} - V_T \right)V_{DS} - \frac{V_{DS}^2}{2} \right) \]

Subthreshold:  \[ I_D = I_S e^{\frac{V_{GS}}{n k T}} \left( 1 - e^{-\frac{V_{DS}}{k T}} \right) \]

“Classical” MOSFET model, will discuss deep submicron modifications as necessary
Subthreshold Current Equation

\[ I_D = I_S e^{\frac{V_{GS}}{n kT/q}} \left( 1 - e^{-\frac{V_{DS}}{kT/q}} \right) \left( 1 + \lambda V_{DS} \right) \]

- \( I_S \) and \( n \) are empirical parameters
- Typically, \( n \geq 1 \) often ranging around \( n \approx 1.5 \)
- Usually want small subthreshold leakage for digital designs
  - Define quality metric: inverse of rate of decline of current wrt \( V_{GS} \) below \( V_T \)
  - Subthreshold slope factor \( S \): \[ S = n \frac{kT}{q} \ln(10) \]
Detailed Subthreshold Current Equation

\[ I_D = A \exp \left( \frac{q}{nkT} (V_{GS} - V_{T0} - \gamma V_S + \eta V_D) \right) \left( 1 - \exp \left( \frac{-q V_{DS}}{kT} \right) \right) \]

\[ A = \mu_0 C_{ox} \frac{W}{L} \left( \frac{kT}{q} \right)^2 e^{1.8} \]

- \( V_{T0} = \) zero bias threshold voltage,
- \( \mu_0 = \) zero bias mobility
- \( C_{ox} = \) gate oxide capacitance per unit area
- \( \gamma = \) linear body effect coefficient (small source voltage)
- \( \eta = \) DIBL coefficient
Leakage Currents vs. Active Currents

\[ \frac{I_{\text{active}}}{I_{\text{leak}}} (I_{\text{on}}/I_{\text{off}}) \] ratio can be small in subthreshold.
Degraded Output Levels

• Balance current ratio through sizing, limiting fanin

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Degraded Logic Levels Impact Functionality

- $V_{DD} = 0.3 \text{ V}$
- $C_{lk} = 80 \text{ mV}$
- $\overline{C_{lk}} = 220 \text{ mV}$
- Driven by two inverters to intermediate voltage

$D$ \rightarrow \text{Inverter} \rightarrow \text{Capacitor} \rightarrow \text{Inverter} \rightarrow Q$
• Leakage paths can degrade read and write noise margins
Conclusions

• **Subthreshold design similar to ratioed ckt design**
  – Must guarantee active currents sufficiently greater than leakage currents to maintain valid logic levels
  – Degraded logic levels can cause failure in combinational and sequential circuits
  – All circuits (esp. SRAMs) sensitive to $V_{TH}$ variation

• **Be careful with subthreshold circuits**
  – Consider worst case leakage situations (data dependent) when analyzing $I_{on}/I_{off}$ ratio problems
  – Use nonminimum channel lengths, limit fanin
  – Watch sneak leakage paths through pass gates
  – Interrupt pass gate chains with static logic