EEC 216 Lecture #6: Clocking and Sequential Circuits

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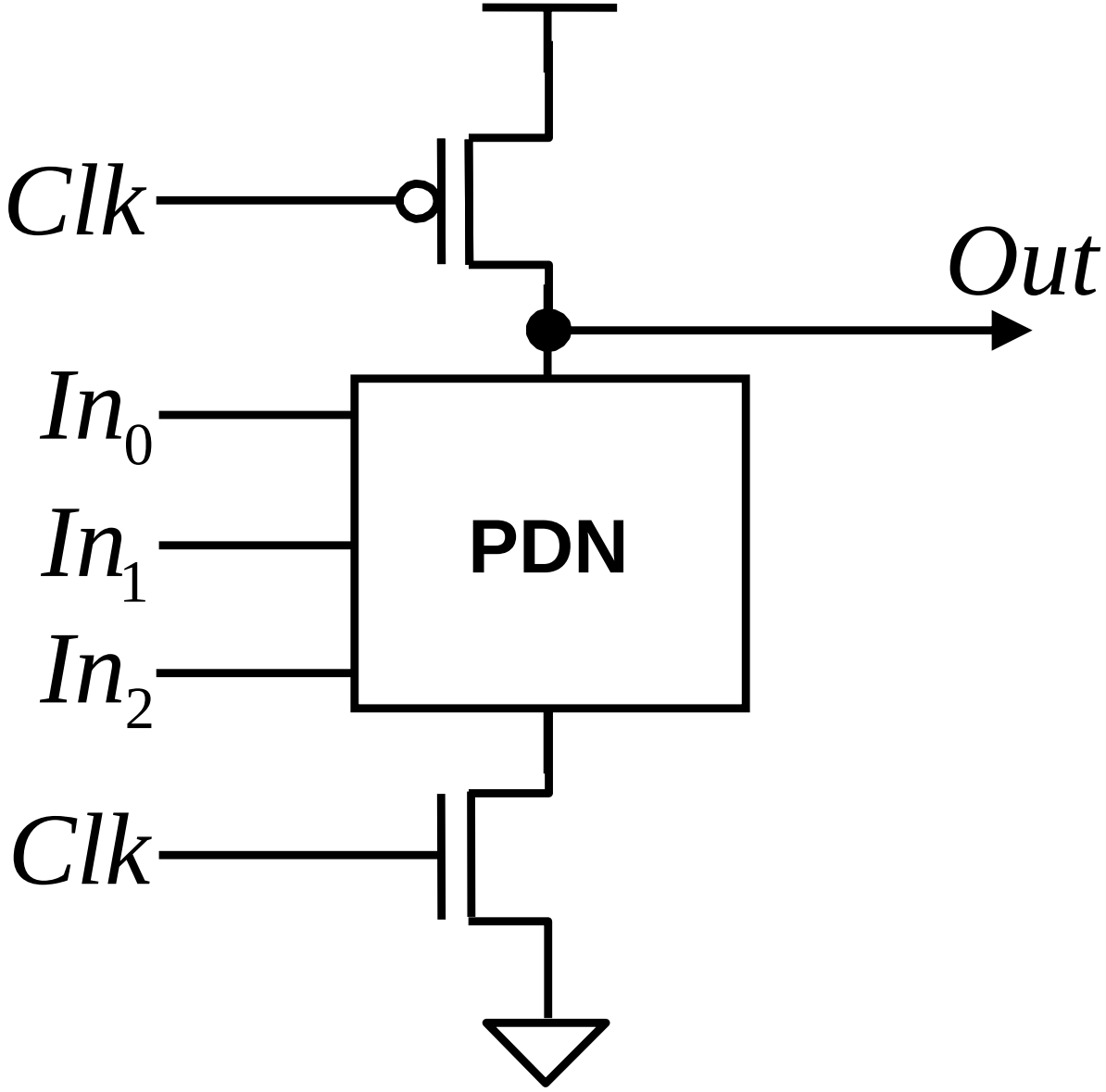
Outline

- Announcements
- **Review: Dynamic Logic, Transistor Sizing**
- Lecture 5: Finish Transistor Sizing
- Lecture 5: Clocking Styles Overview
- Lecture 5: Static Latches and Flip-Flops
- Dynamic Latches and Flip-Flops
- Alternative Flip-Flop Styles
- Self-Timed Circuits

Dynamic CMOS Logic Concepts

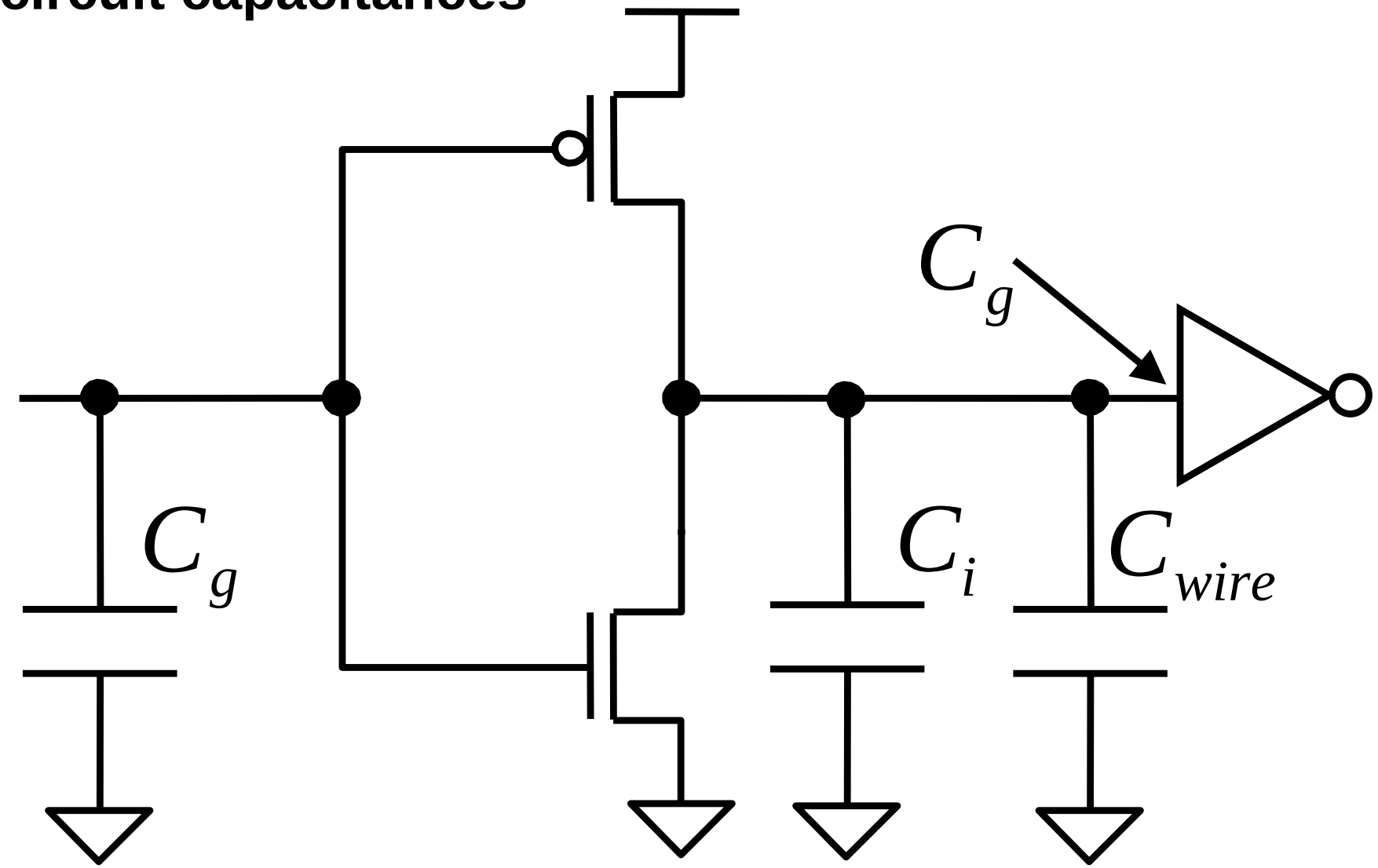
- **Precharge Phase**
  - Output node charged to reference voltage and left floating before evaluation
  - Load capacitance “stores” the precharge value
- **Evaluation Phase**
  - Path to change the output node voltage energized by turning on evaluation transistor
  - Depending on inputs, load capacitance “written” with final value (changed from precharge value or left unchanged)
- **Inputs must make at most one transition during evaluation**
- **Output can be left high impedance, unlike static CMOS**

Dynamic CMOS Logic

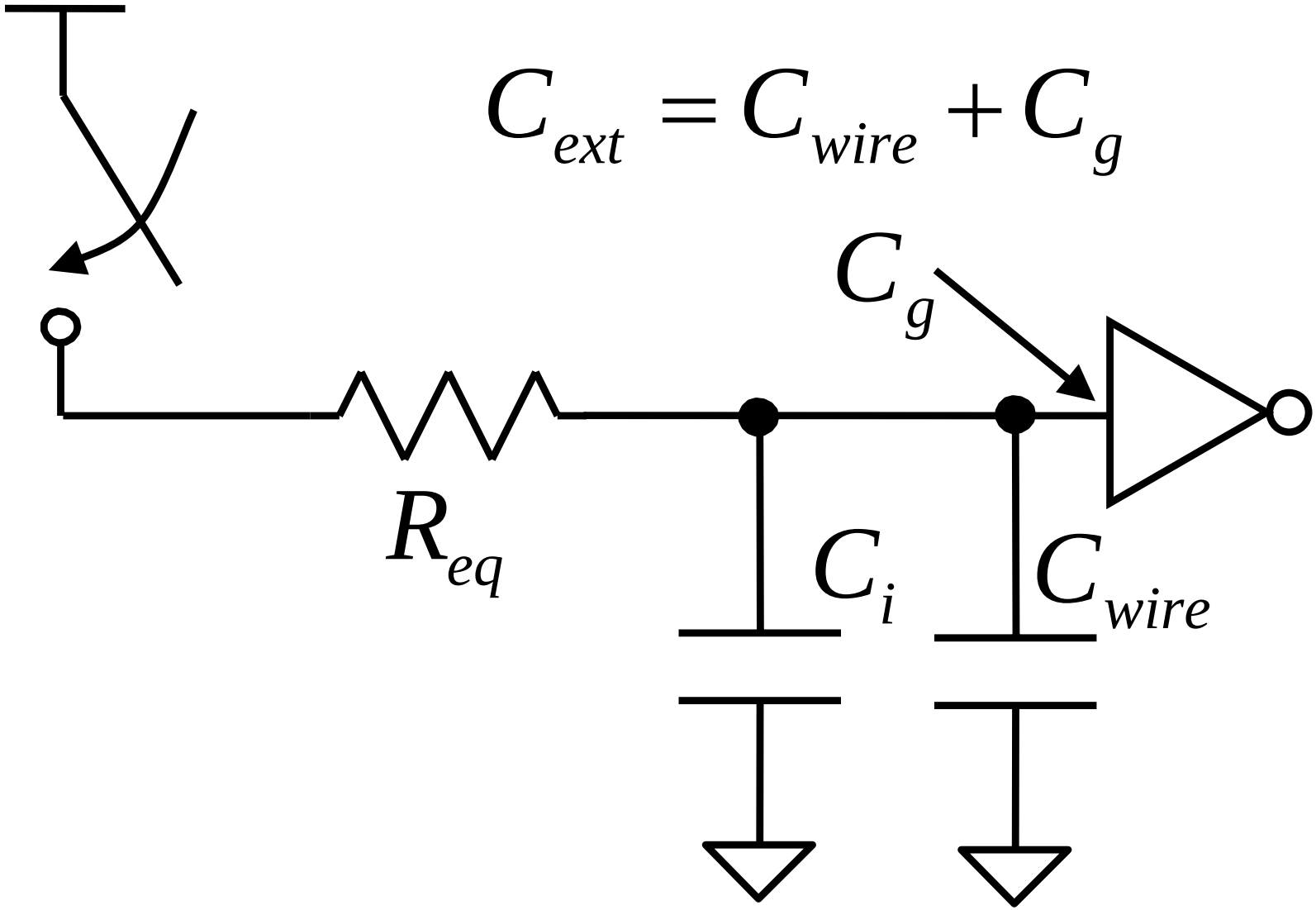


Intrinsic (Self-Load) and Extrinsic Capacitance

- **To analyze delay/sizing tradeoffs, must account for all circuit capacitances**

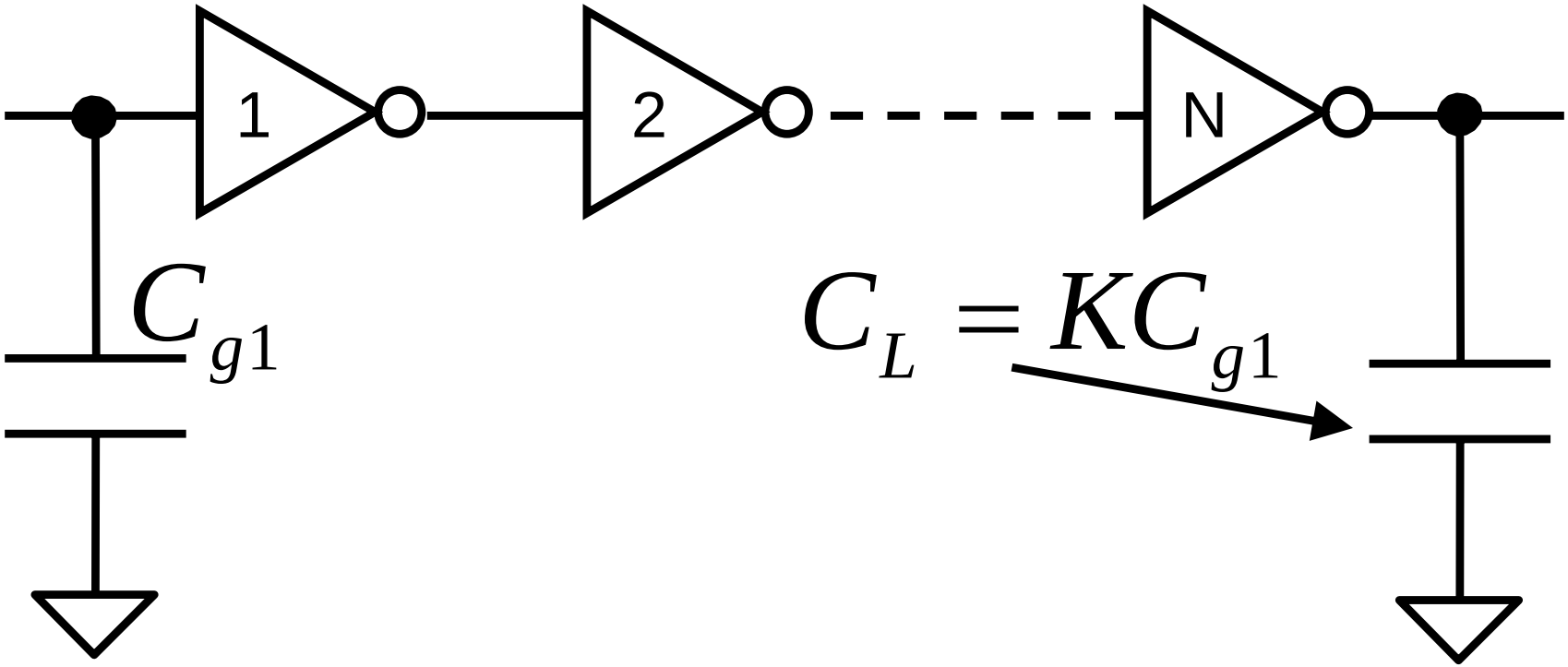


RC Switch Model for Inverter Sizing



- **Model delay using ideal switch and resistor for MOSFET**

Inverter Chain Sizing for Minimum Delay



- **Using inverter sizing, want to minimize delay of driving large load C_L**
- **Optimize using equivalent resistance delay equation derived in previous slides**

Optimal Inverter Stages for Minimum Delay

- **Delay trade off in the number of stages *N***
  - Too many stages, intrinsic delay term dominates
  - Too few stages, extrinsic term due to fanout ratio dominates
- **Taking derivative of T_{pd} wrt *N* and setting equal to zero yields scale up factor for optimal number of stages:**

$$k = e^{\left(1+\frac{\gamma}{k}\right)}$$

- **Closed form solution when** $\gamma = 0$, $N = \ln(K)$

$$k = e = 2.71828$$

- **For more typical case of** $\gamma = 1, k = 3.6$
- **Often choose** $k = 4$

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- **Dynamic Latches and Flip-Flops**
- Alternative Flip-Flop Styles
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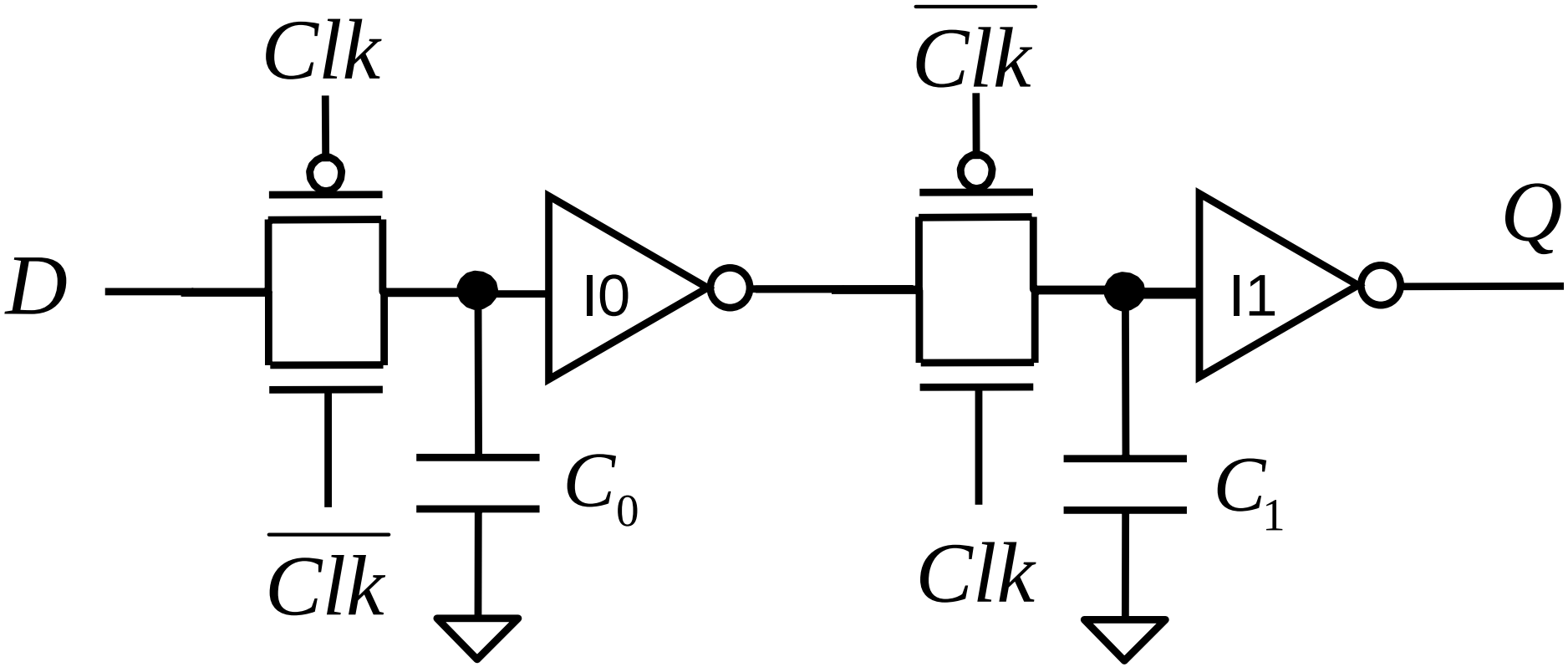
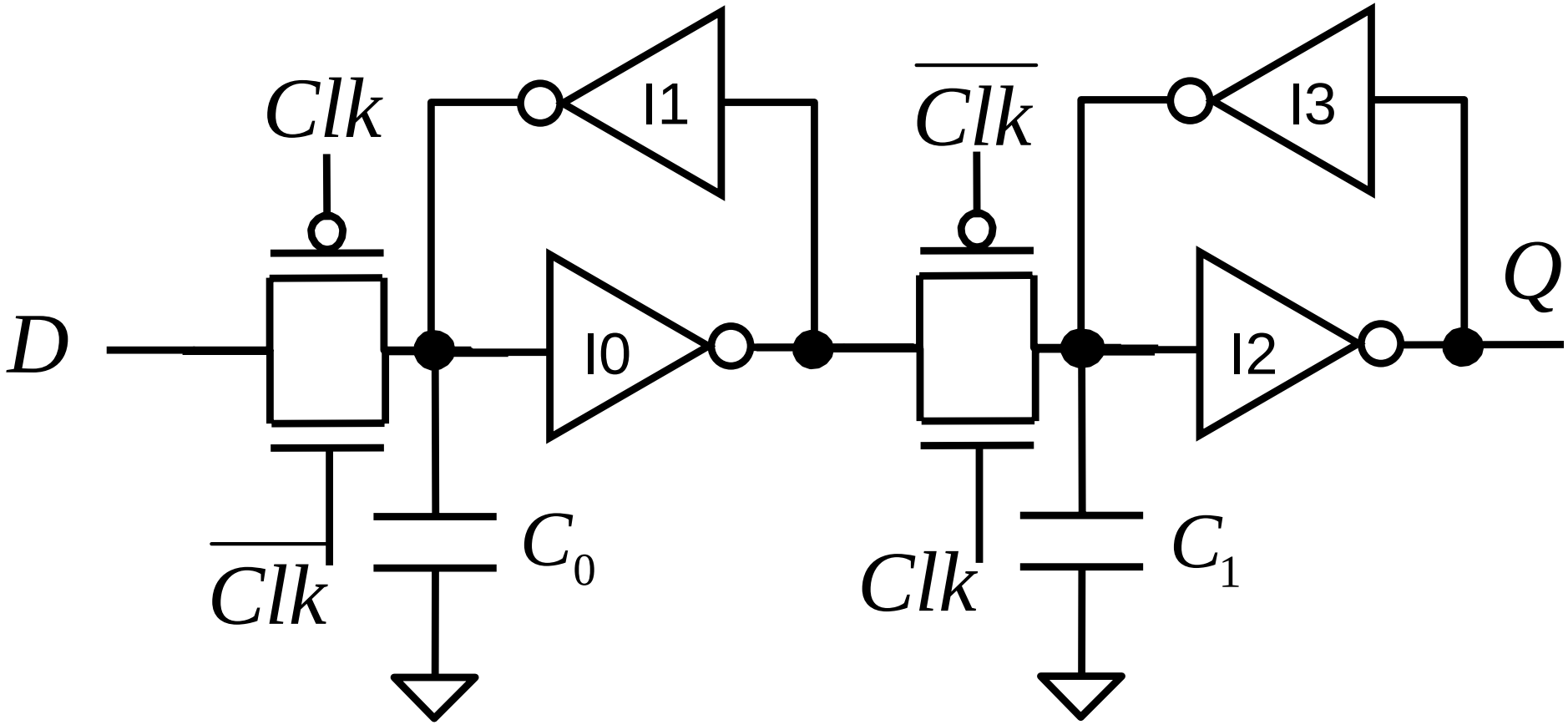
Dynamic Positive Edge-Triggered FF



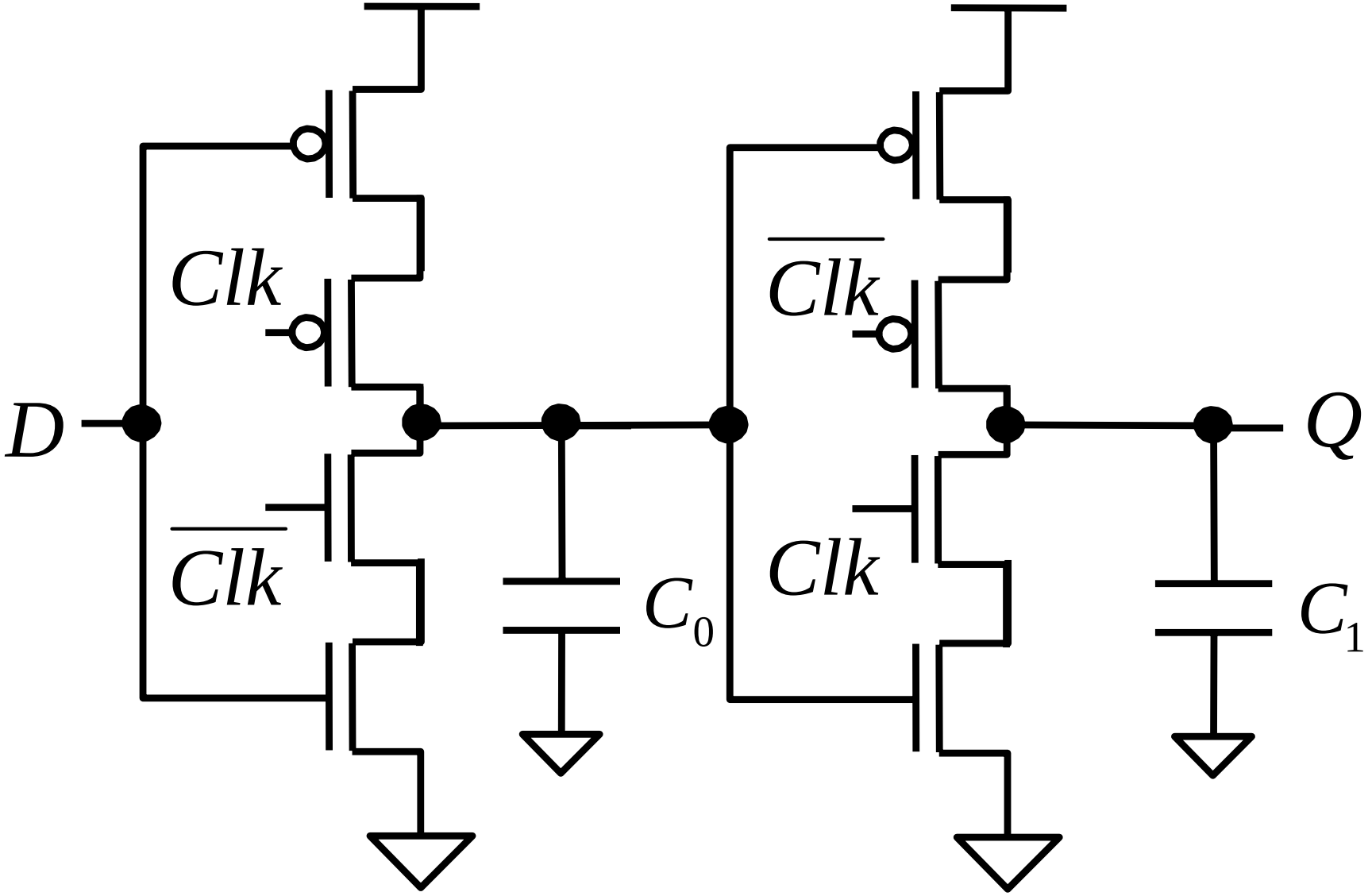
- **No feedback devices**
- **Data stored on input capacitances of inverters I0 and I1**
- **Dynamic logic issues apply: leakage, capacitive coupling, charge sharing**

Staticized Dynamic Positive Edge-Triggered FF



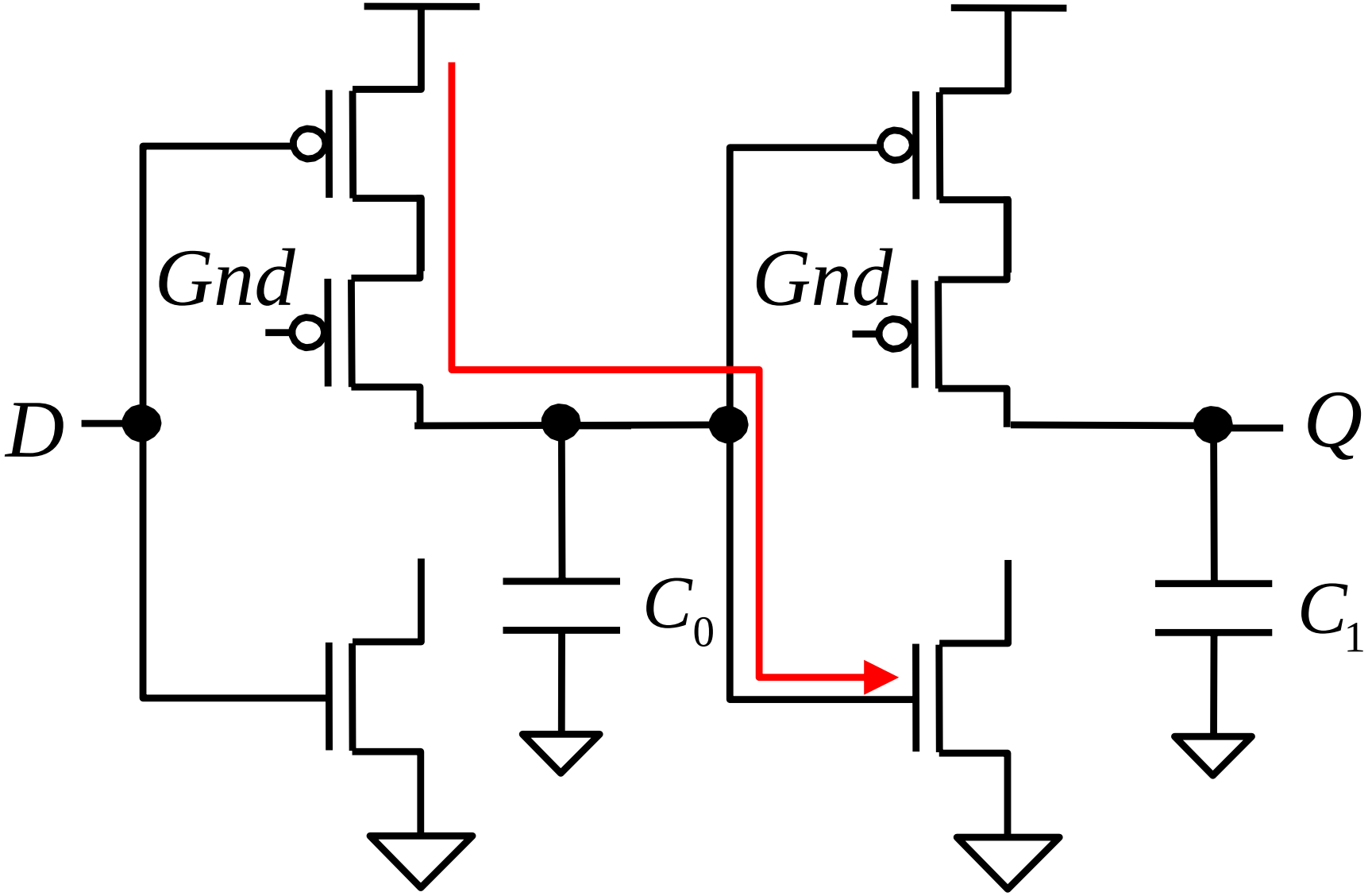
- **Use weak feedback inverters to enhance robustness**
- **Returns to reduced clock load static flip-flop with same sizing issues**

C²MOS Edge Triggered Flip-Flop



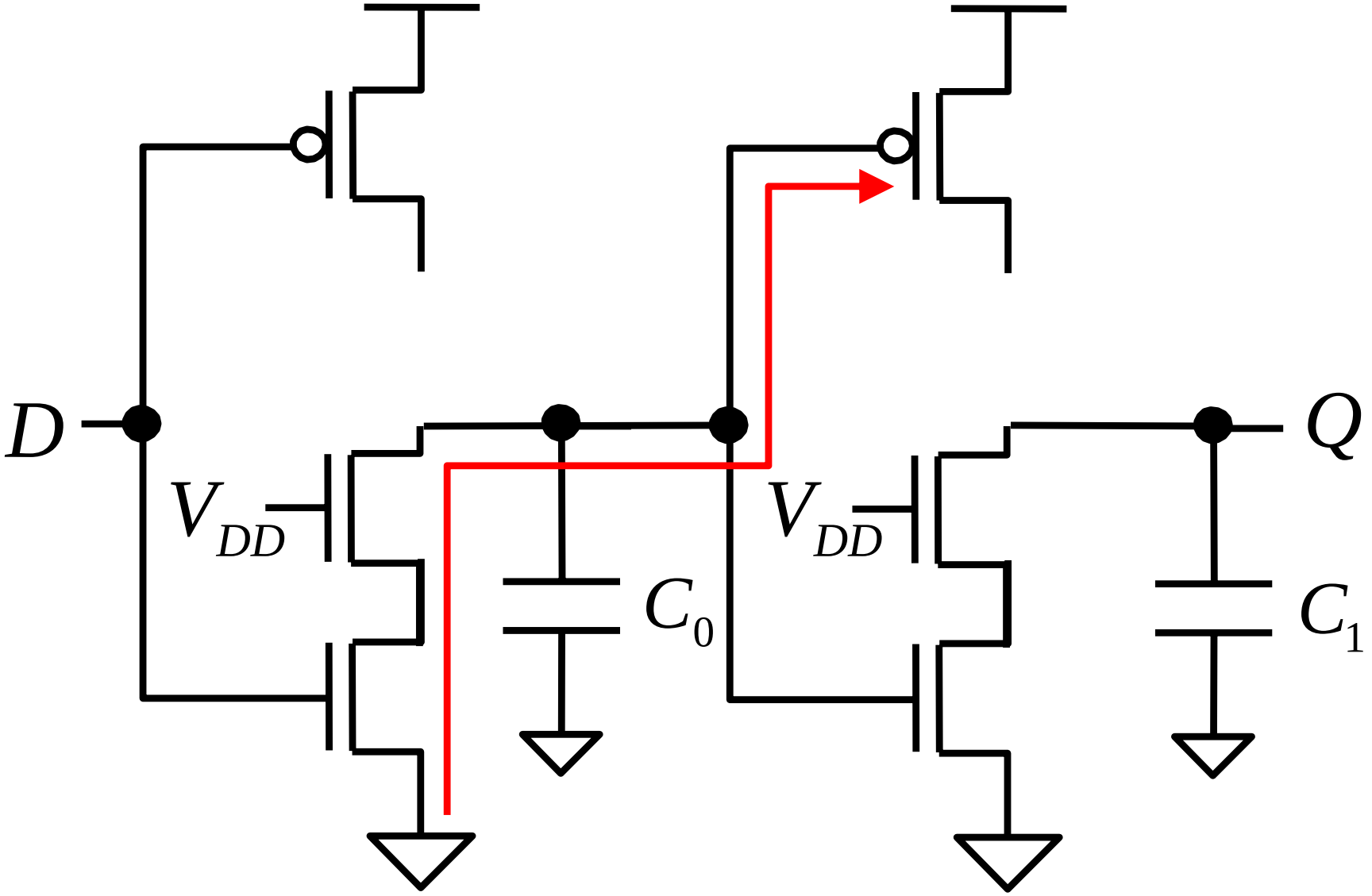
- **Eliminates clock overlap race condition**

Zero-Zero Overlap Condition



- **Both phases low simultaneously enables opposite nets**

High-High Overlap Condition

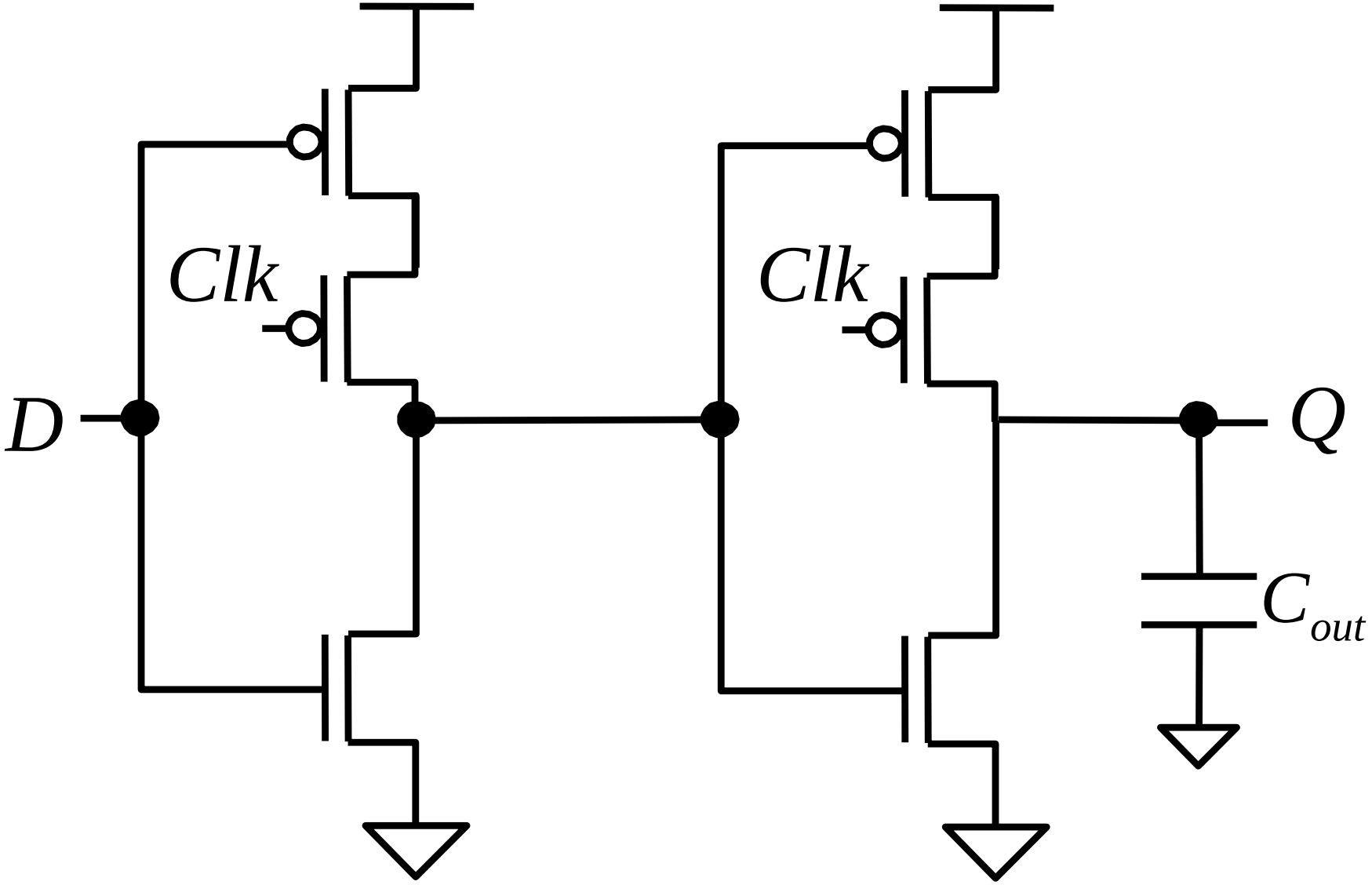


- **Both phases high simultaneously enables opposite nets**

C^2MOS Design

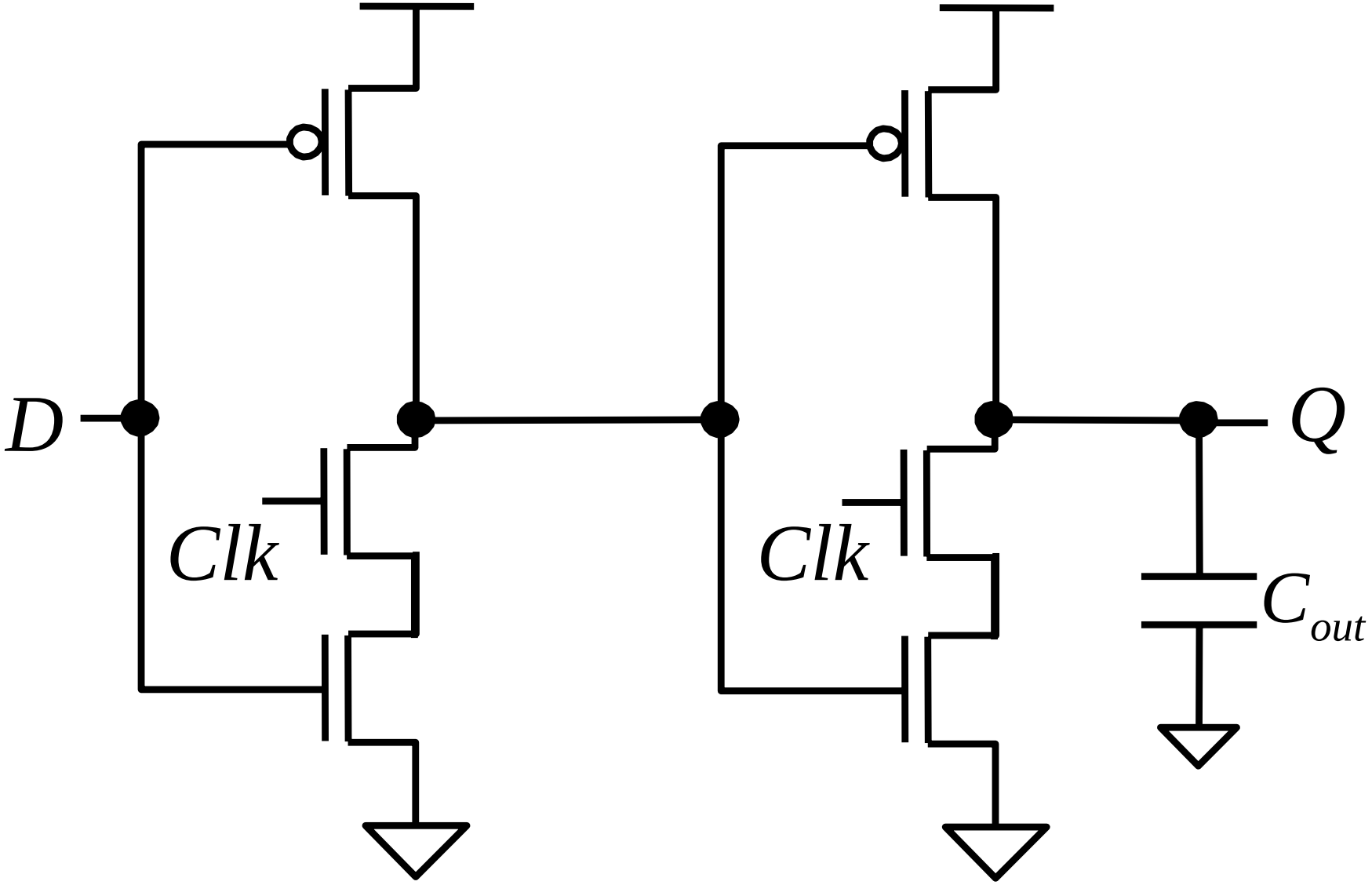
- **Clock overlap problems eliminated as long as rise and fall times remain fast**
  - Slow rise / fall times imply pullup and pulldown nets on simultaneously resulting in potential errors, static power
- **Dynamic flip-flop style leaves output high Z**
  - Must take care when using since output wire could be exposed to many more noise sources than internal nodes
- **Mix and match styles by using C^2MOS as master and other types of latch as slave**
- **Clock load small, but potentially larger than transmission gate dynamic latches due to PMOS sizing**

True Single-Phase Clock Negative Latch



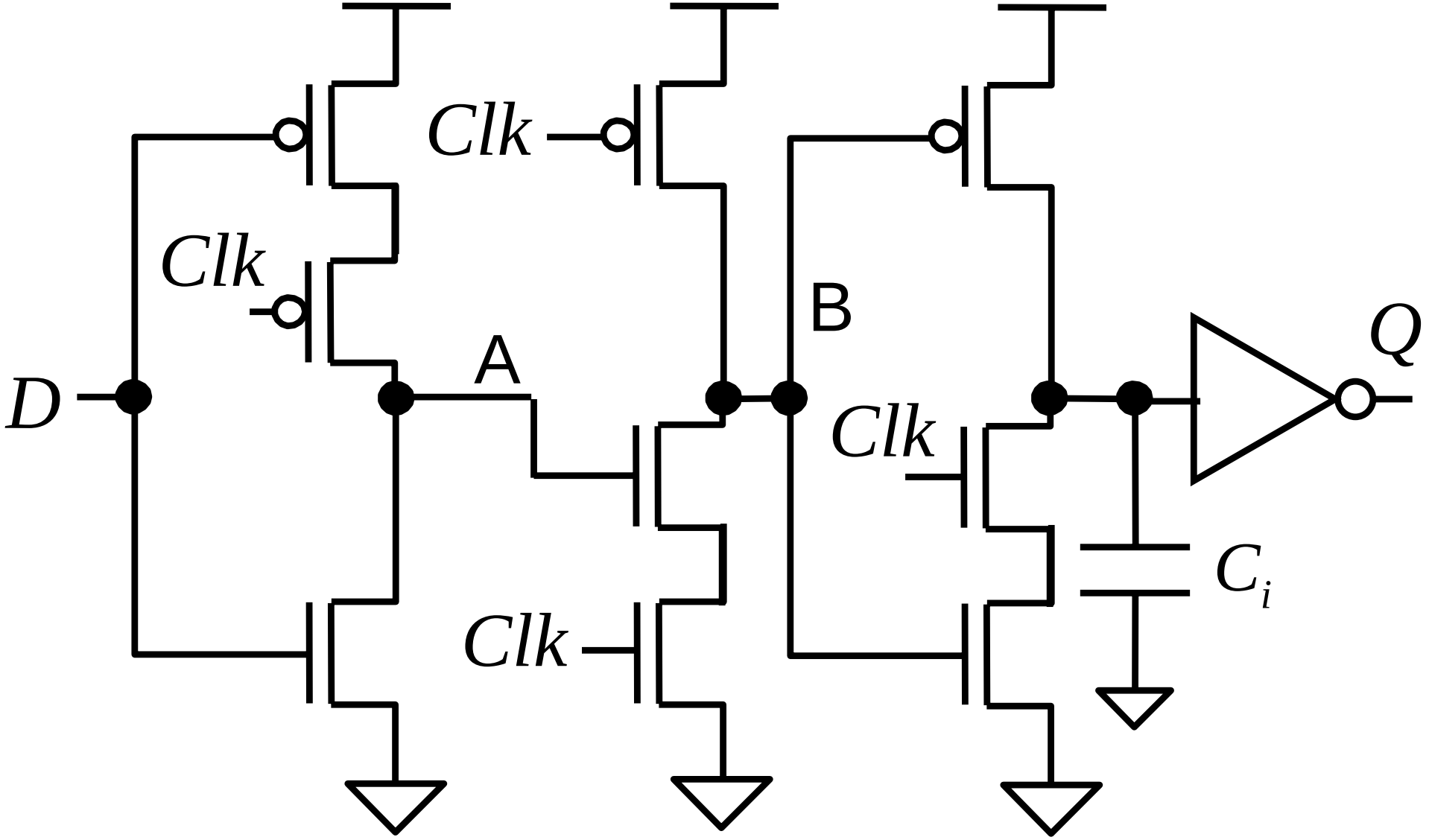
- **Idea is to eliminate one polarity of clock**

True Single-Phase Clock Positive Latch



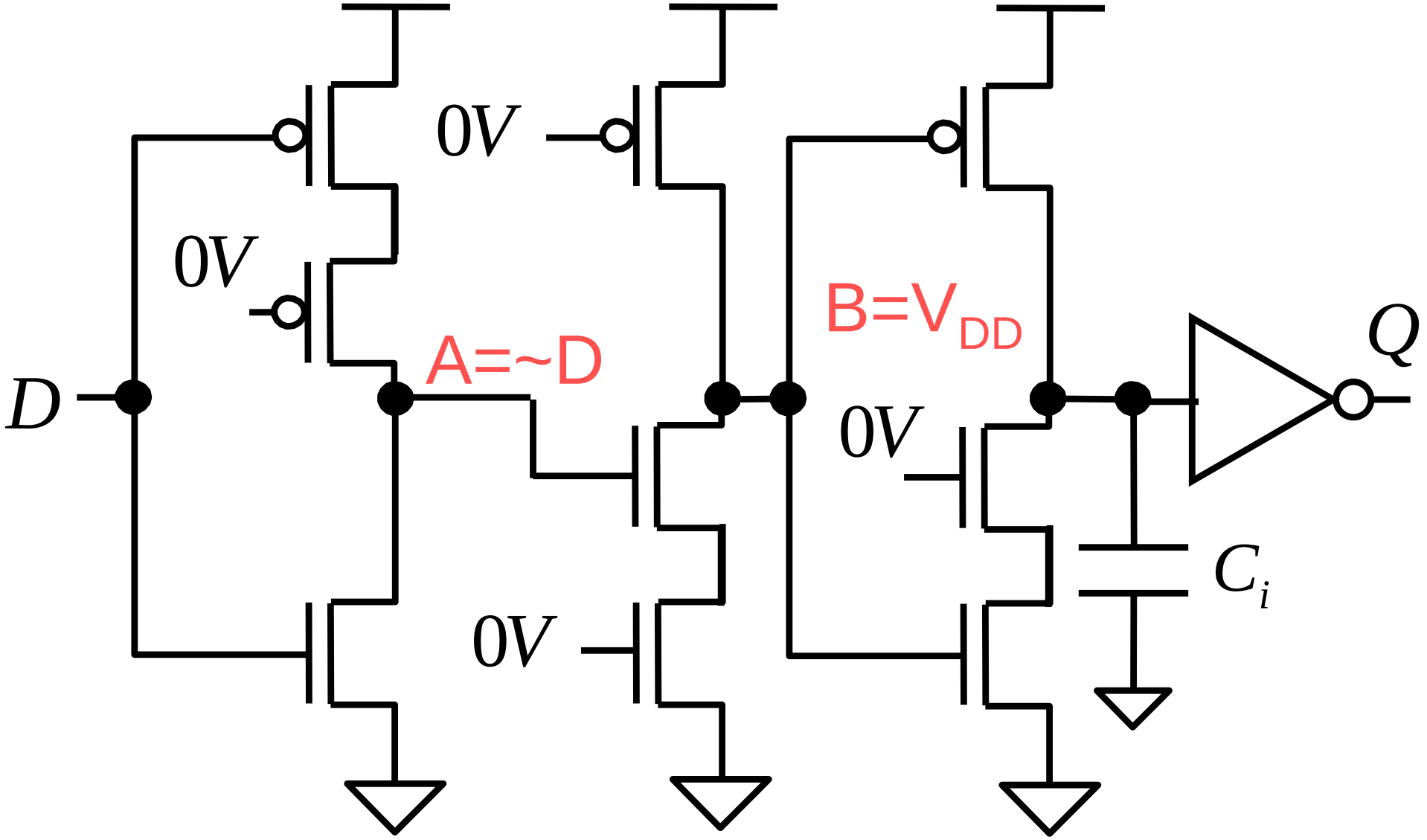
- **Complementary version**

TSPC Positive Edge Triggered Flip-Flop



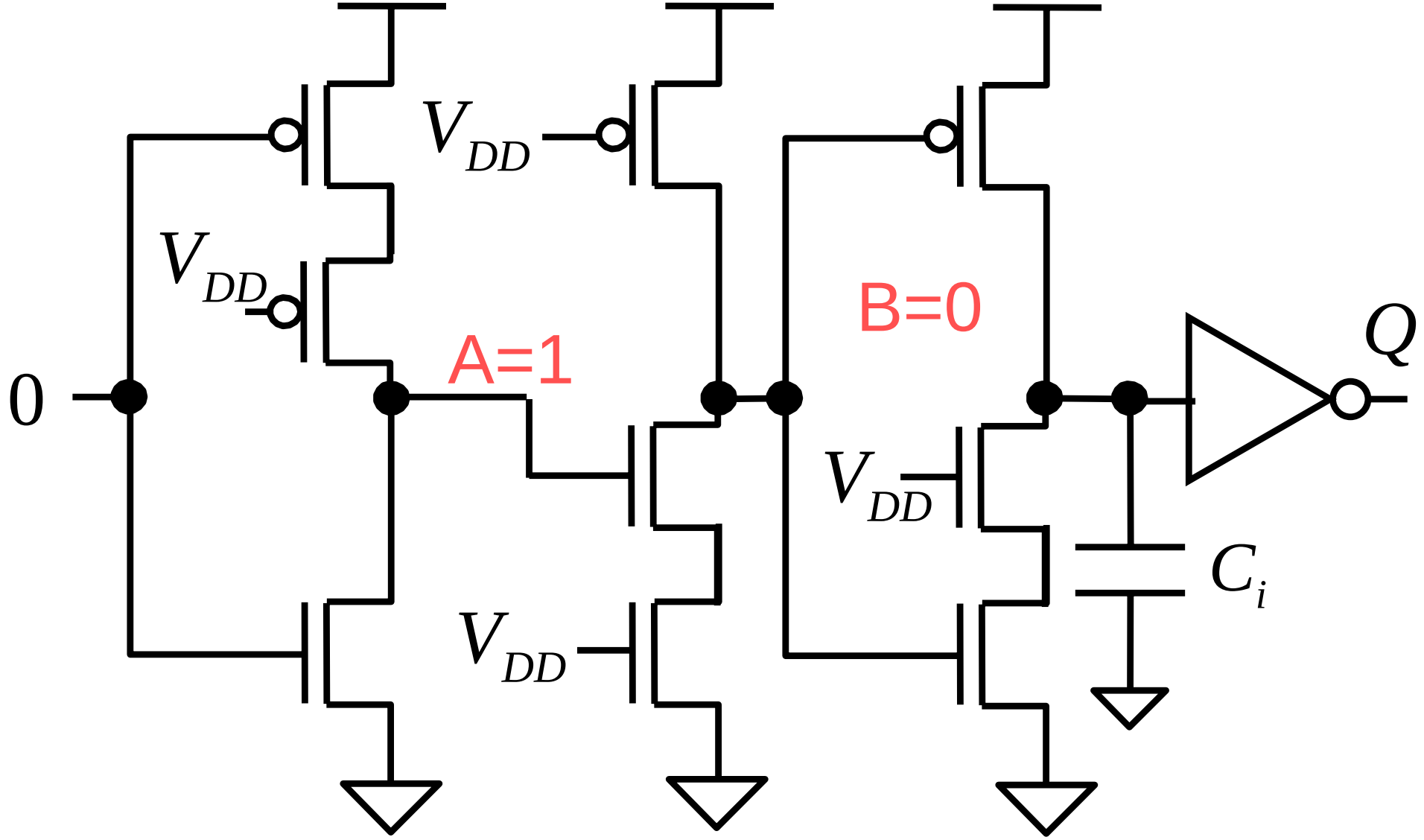
- **Combine TSPC latches and merge**

TSPC Positive Edge Triggered Flip-Flop



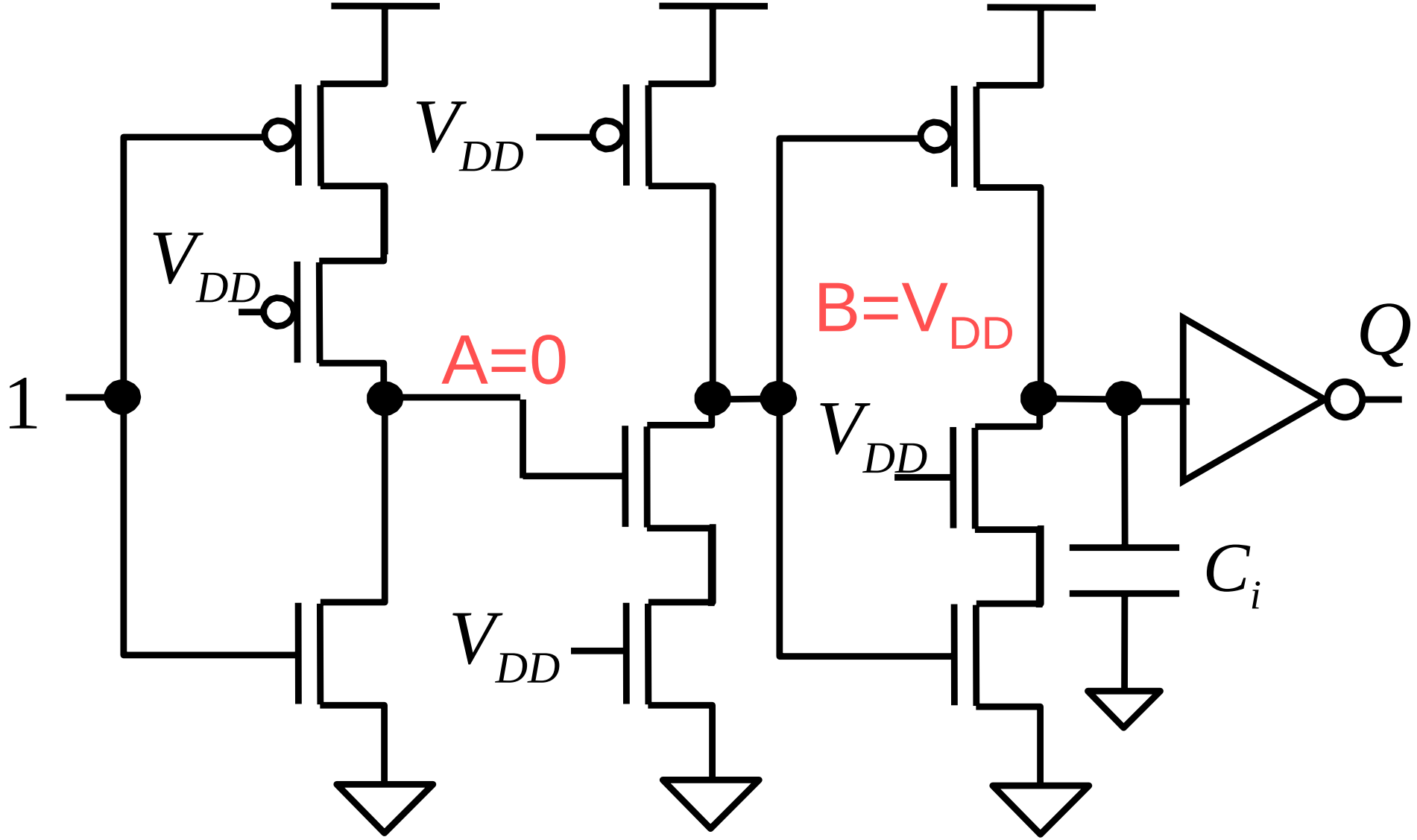
- **Clk low, A = not(D) and B precharged**

TSPC Positive Edge Triggered Flip-Flop



- **Clk high, D = 0, B discharged, C_i charges, Q goes low**

TSPC Positive Edge Triggered Flip-Flop



- **Clk high, D = 1, B stays high, C_i discharges, Q goes high**

TSPC Design

- **Clock overlap problems eliminated since only single clock required**
  - Frees routing resources compared to nonoverlapped clocks
- **Dynamic flip-flop style leaves internal nodes high Z**
  - Inherent race condition in edge-triggered flip-flop must be dealt with by careful sizing
- **Small clock load, only four transistors and no local inversion**

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- **Alternative Flip-Flop Styles**
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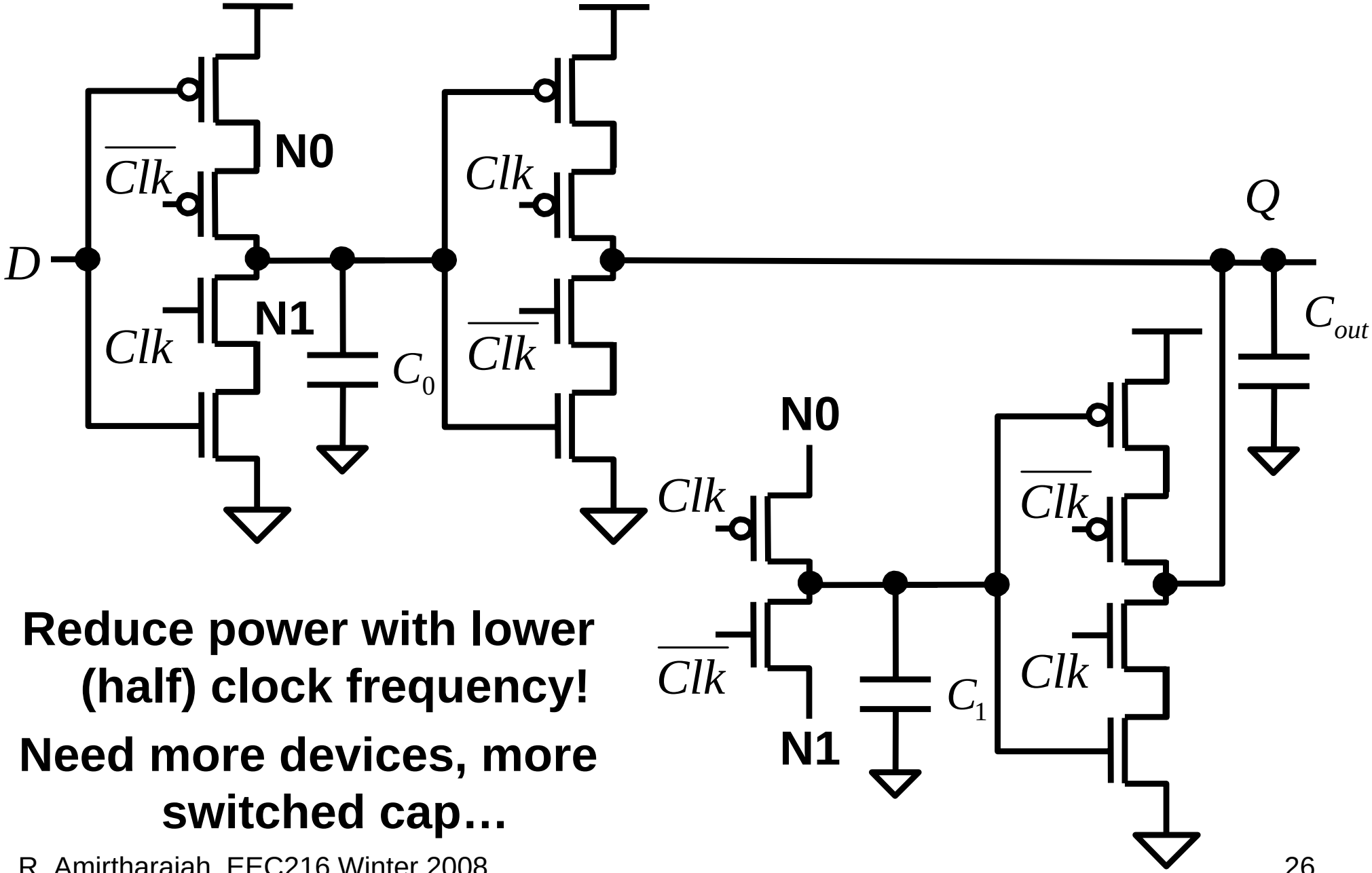
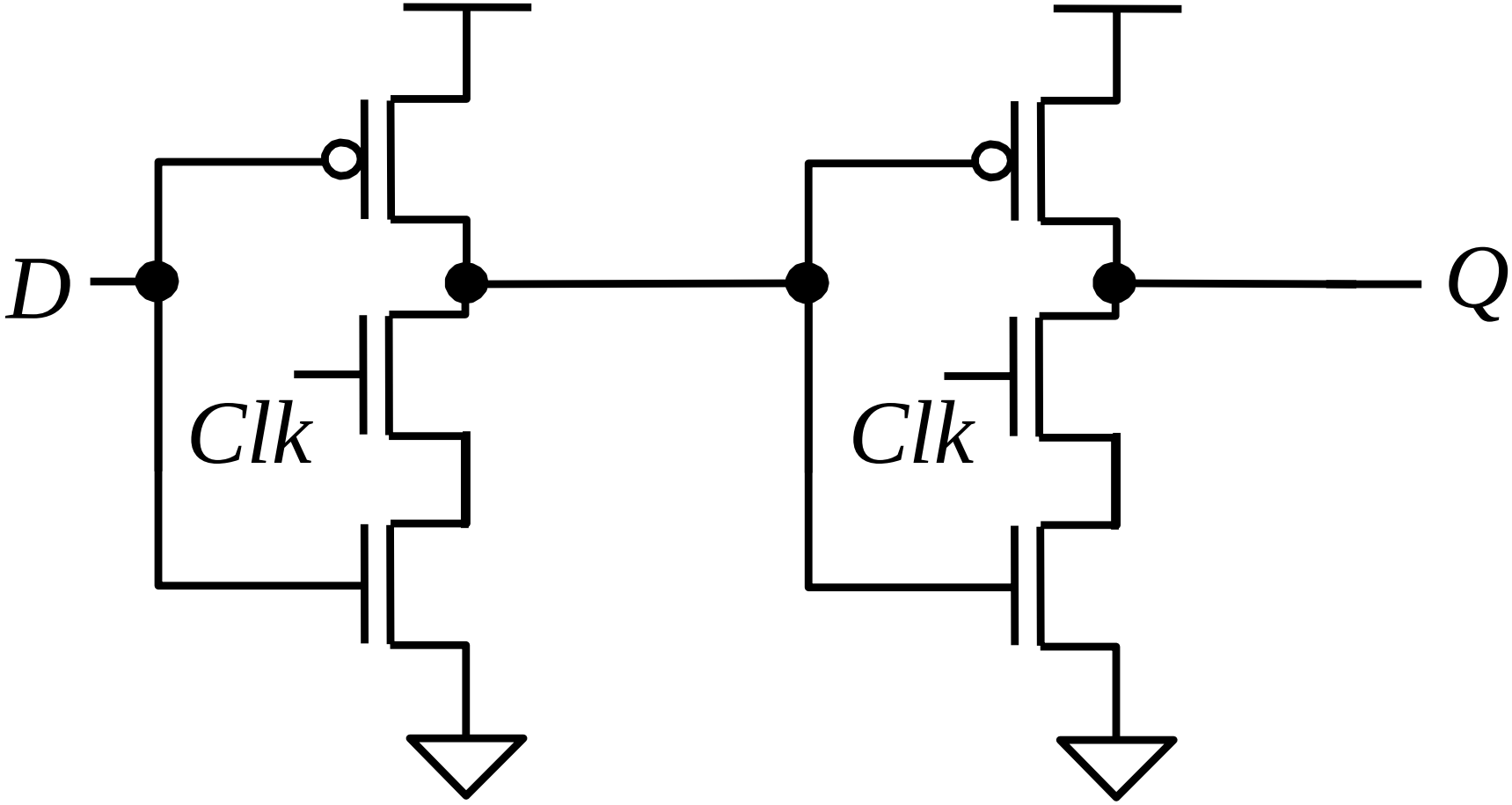
C²MOS Dual-Edge Triggered Flip-Flop

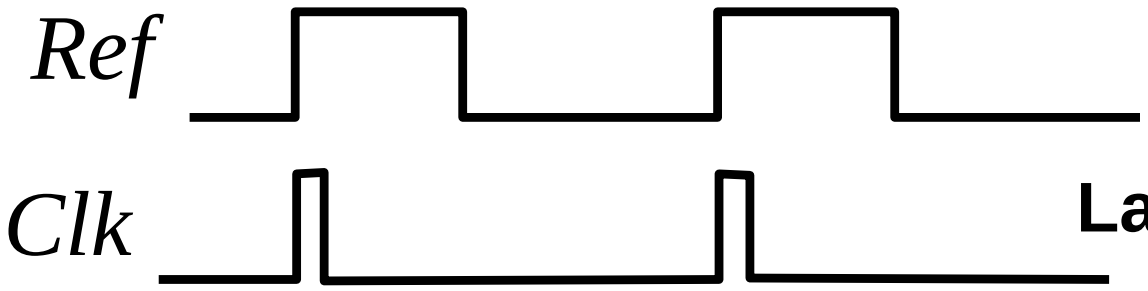


Reduce power with lower (half) clock frequency!

Need more devices, more switched cap…

TSPC Based Pulse Register



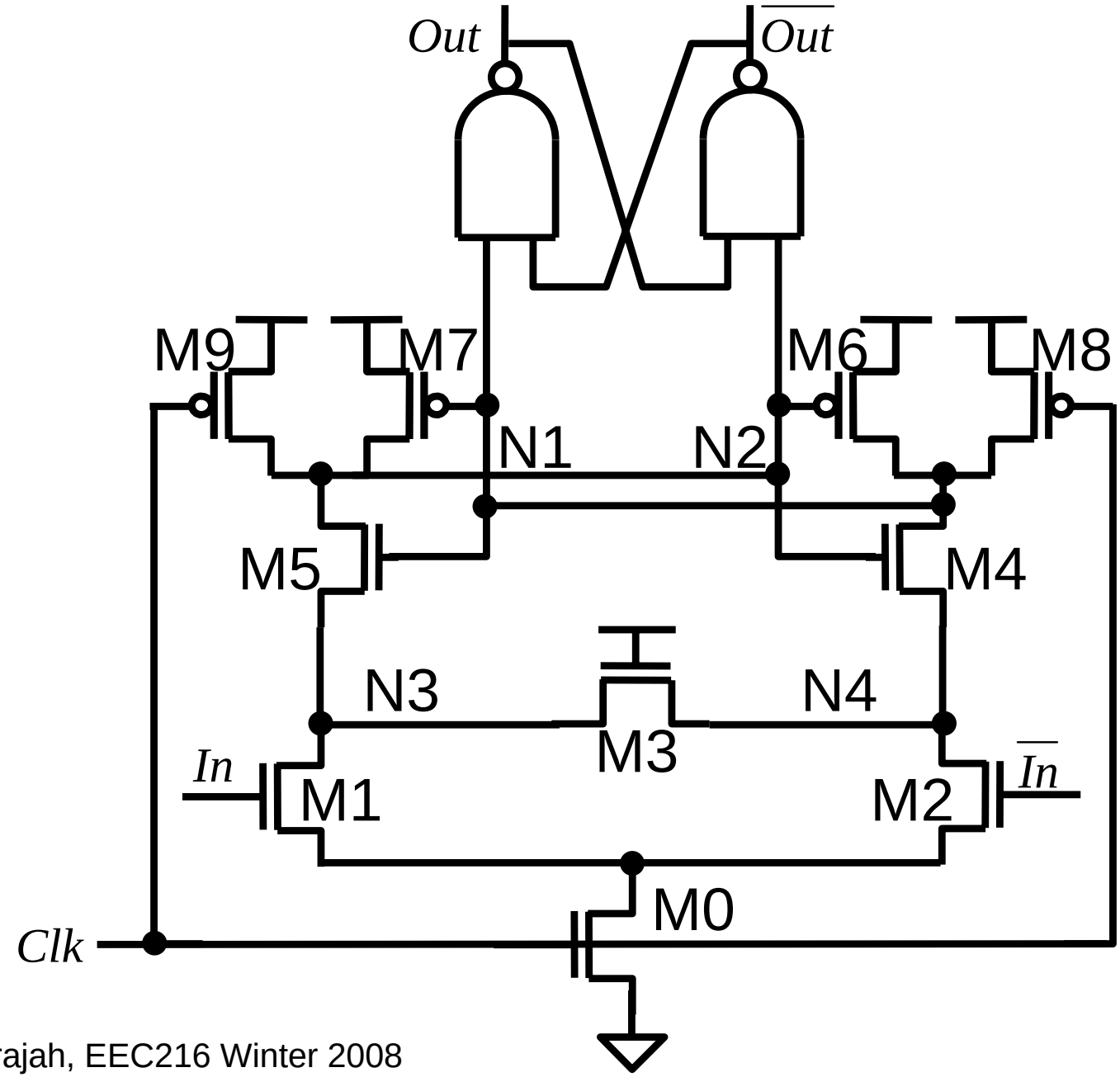


Latch briefly transparent!

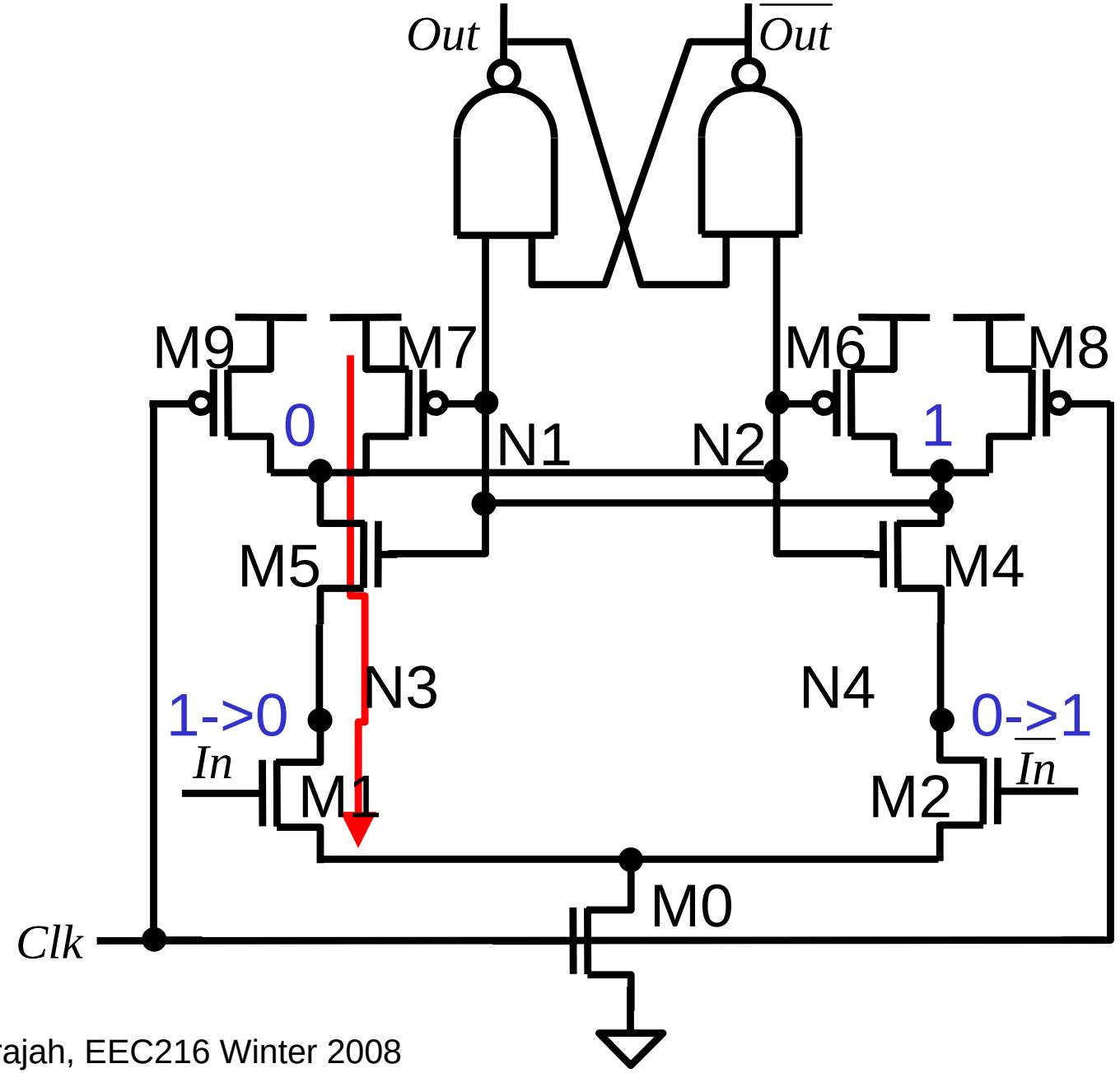
Pulse Register Design

- **Advantages in timing discipline**
  - Since edge-triggered flip-flop equivalent to transparent latch, there is essentially 0 setup time
  - Hold time is equivalent to glitch width
  - Clock-to-Q delay is only two gate delays
- **Reduced clock load and few devices, low area for lower power**
- **Can use glitch circuit (one-shot) to generate narrow pulses from regular clock**
  - Amortize over many state elements
  - High frequency signal (narrow pulse) challenging to distribute over lossy interconnect

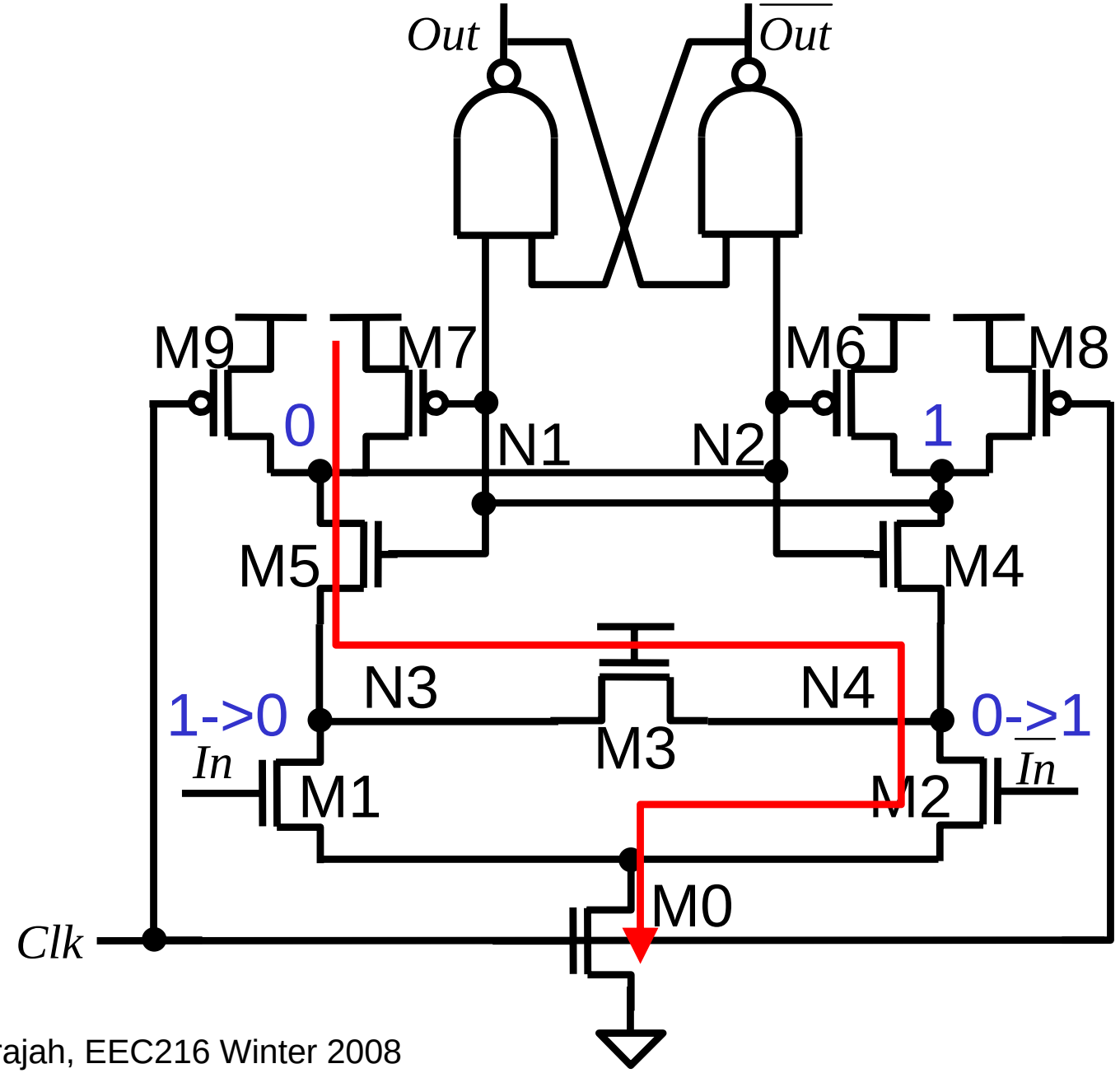
Sense Amplifier Based Edge-Triggered FF



Leakage Problem When Inputs Change



M3 Eliminates Leakage Problem



Sense Amplifier Register Design

- **Designed to detect small (below rail-to-rail) differential inputs**
  - Good for low swing large capacitances, since dynamic power drops quadratically with decreasing voltage swing
  - Potentially fast since input swings can be small, less time required to develop adequate differential voltage
- **Several analog design issues**
  - Must ensure both halves of design well matched to enable minimum input swing (reduced offset)
  - Large area consumed by single flip-flop, especially if good input transistor matching required

Flip-Flop Design Example

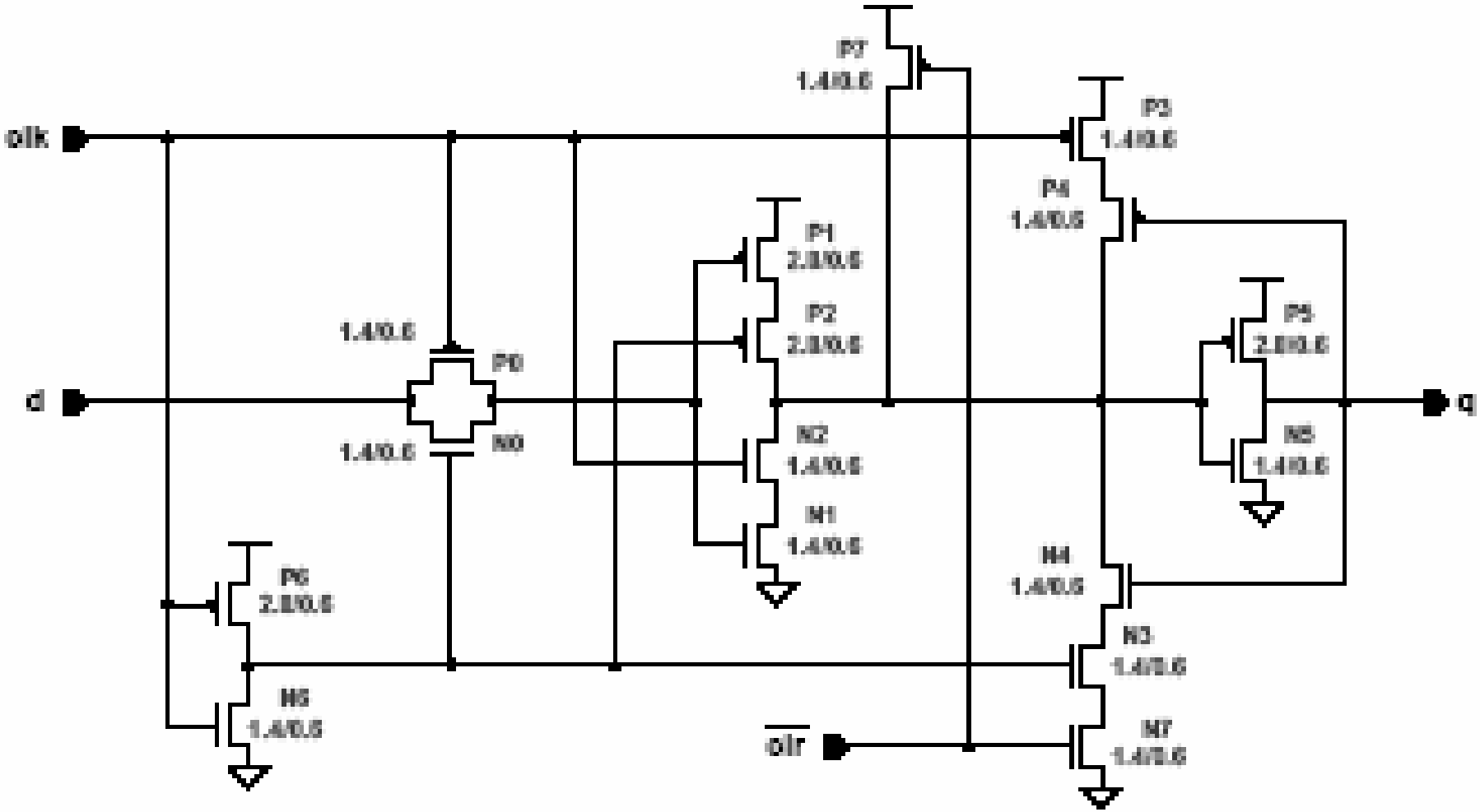


Fig. 9. Positive edge-triggered flip-flop with asynchronous clear schematic.

- **Amirtharajah PhD 99, JSSC 04**

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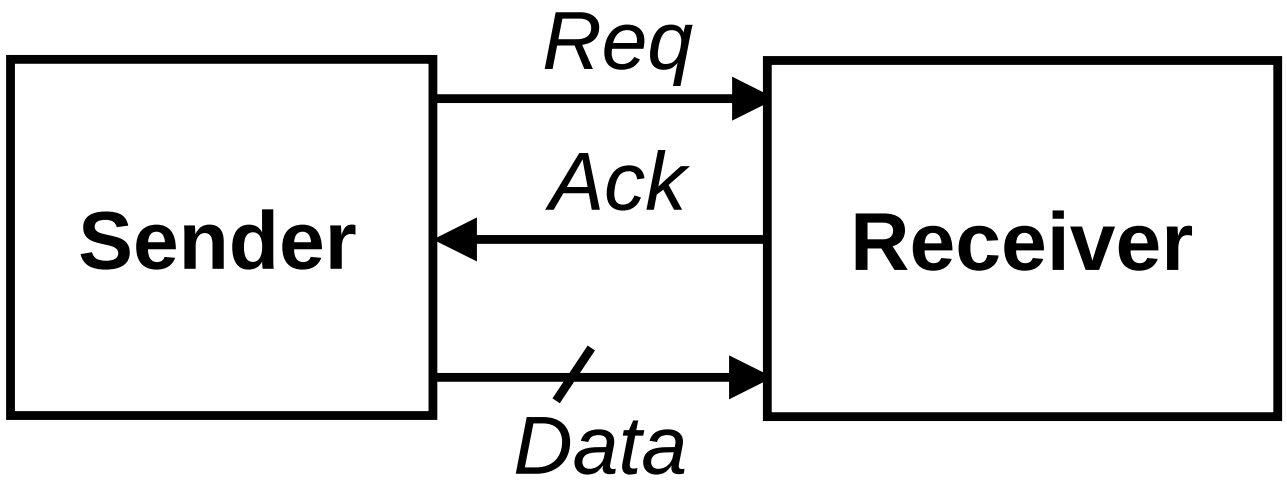
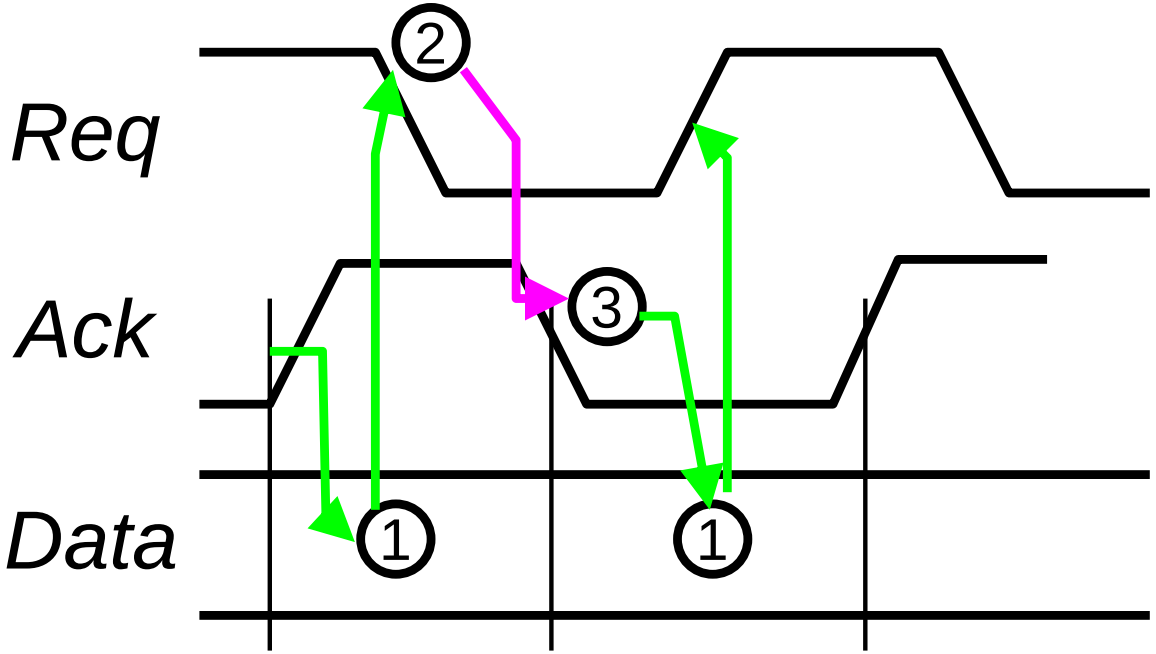
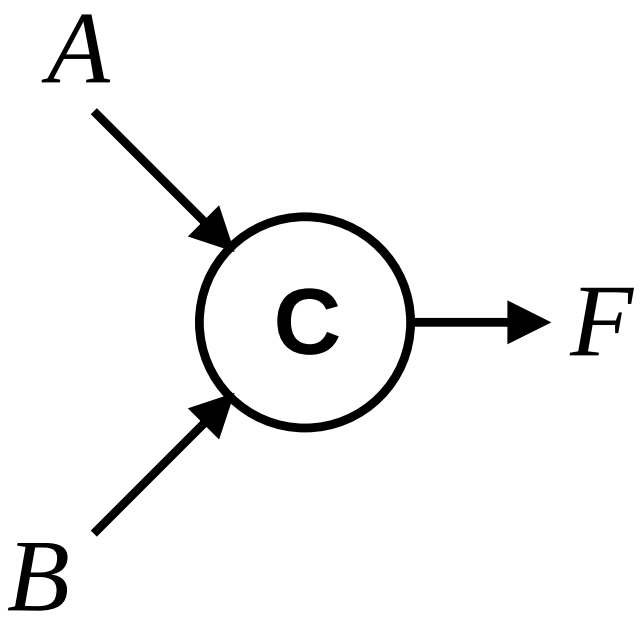
Two Phase Handshake Protocol





- **Green: sender action, Magenta: receiver action**

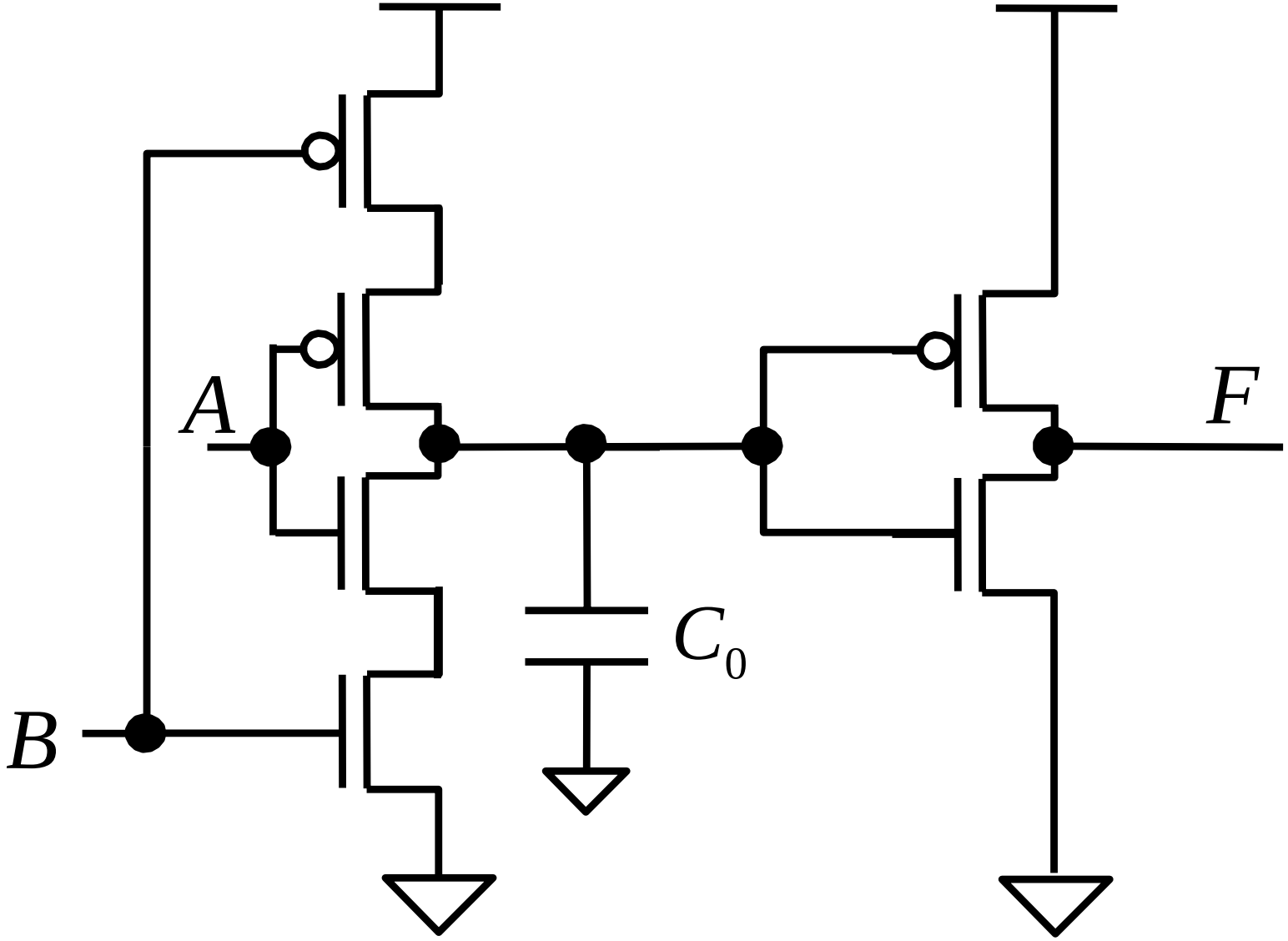
Muller C-Element



A	B	F_{n+1}
0	0	0
0	1	F_n
1	0	F_n
1	1	1

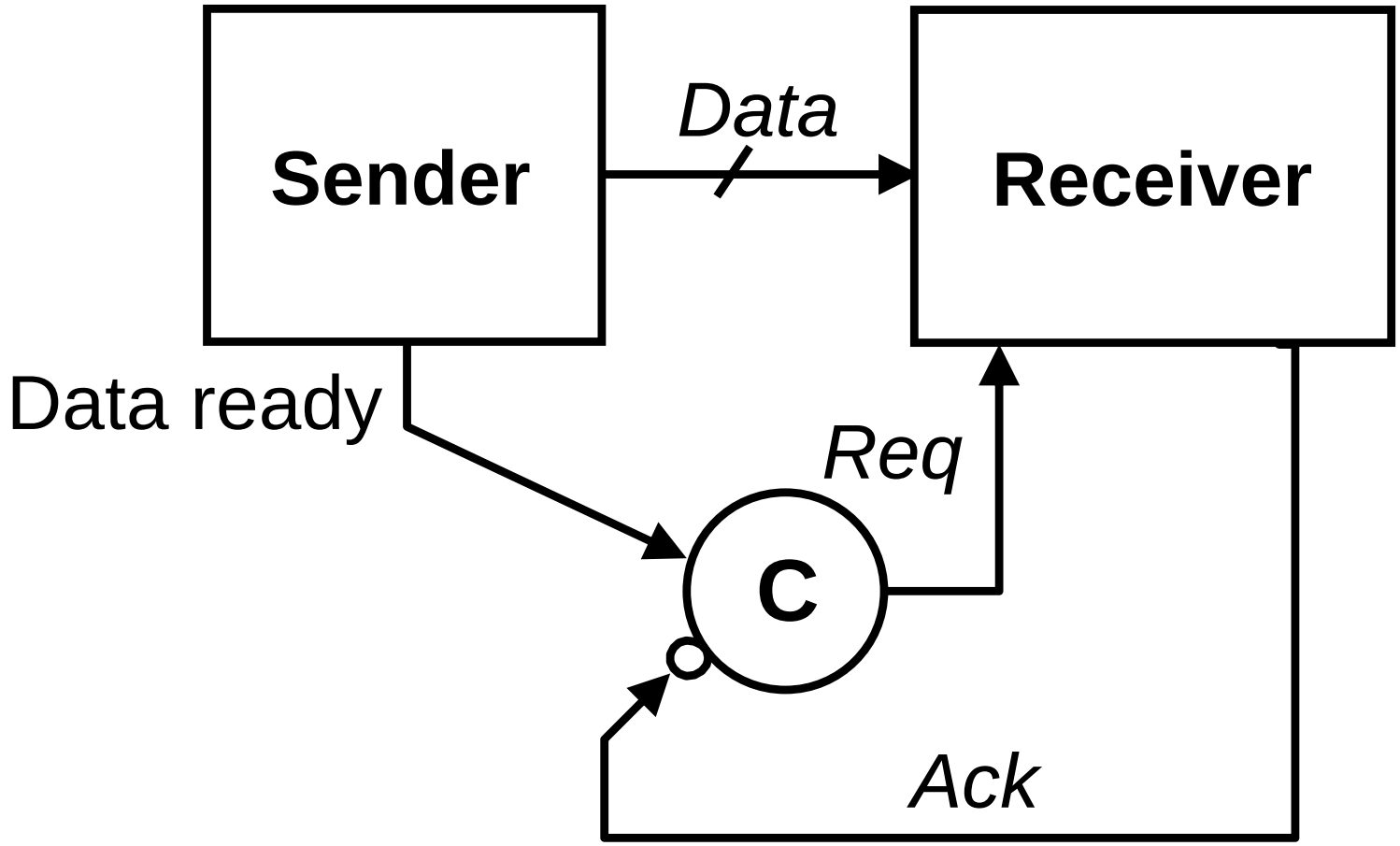
- **Signaling protocol requires strict ordering of transitions**
- **Muller C-element essential component of handshake logic**
  - Performs AND operation on events
  - Events required on both inputs before output event generated

Dynamic Muller C-Element



- **Dynamic latch on output handles memory function**

Two Phase Protocol Implementation

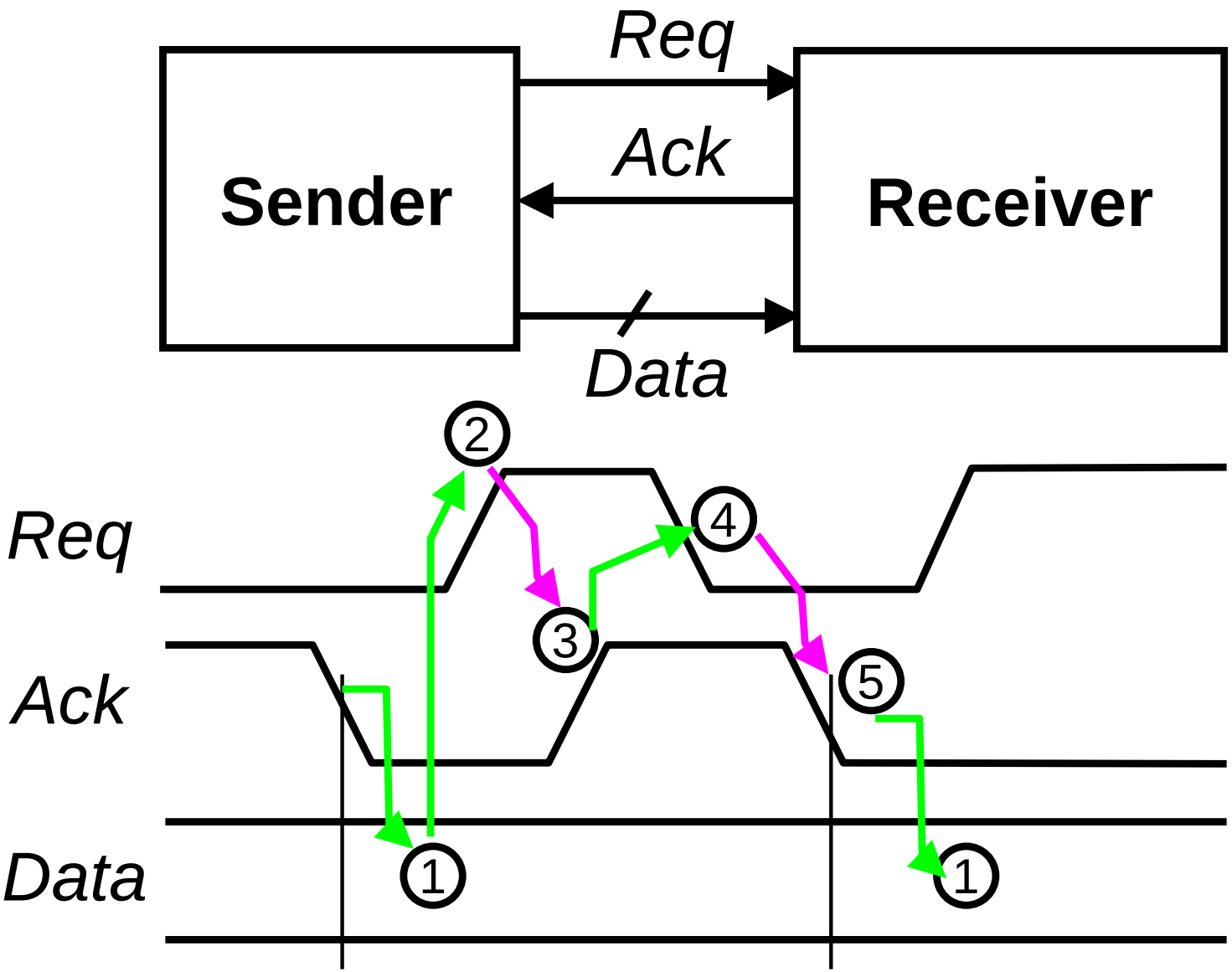


- **Two phase protocol can be implemented with single C-element and inverter**

Two Phase Protocol Issues

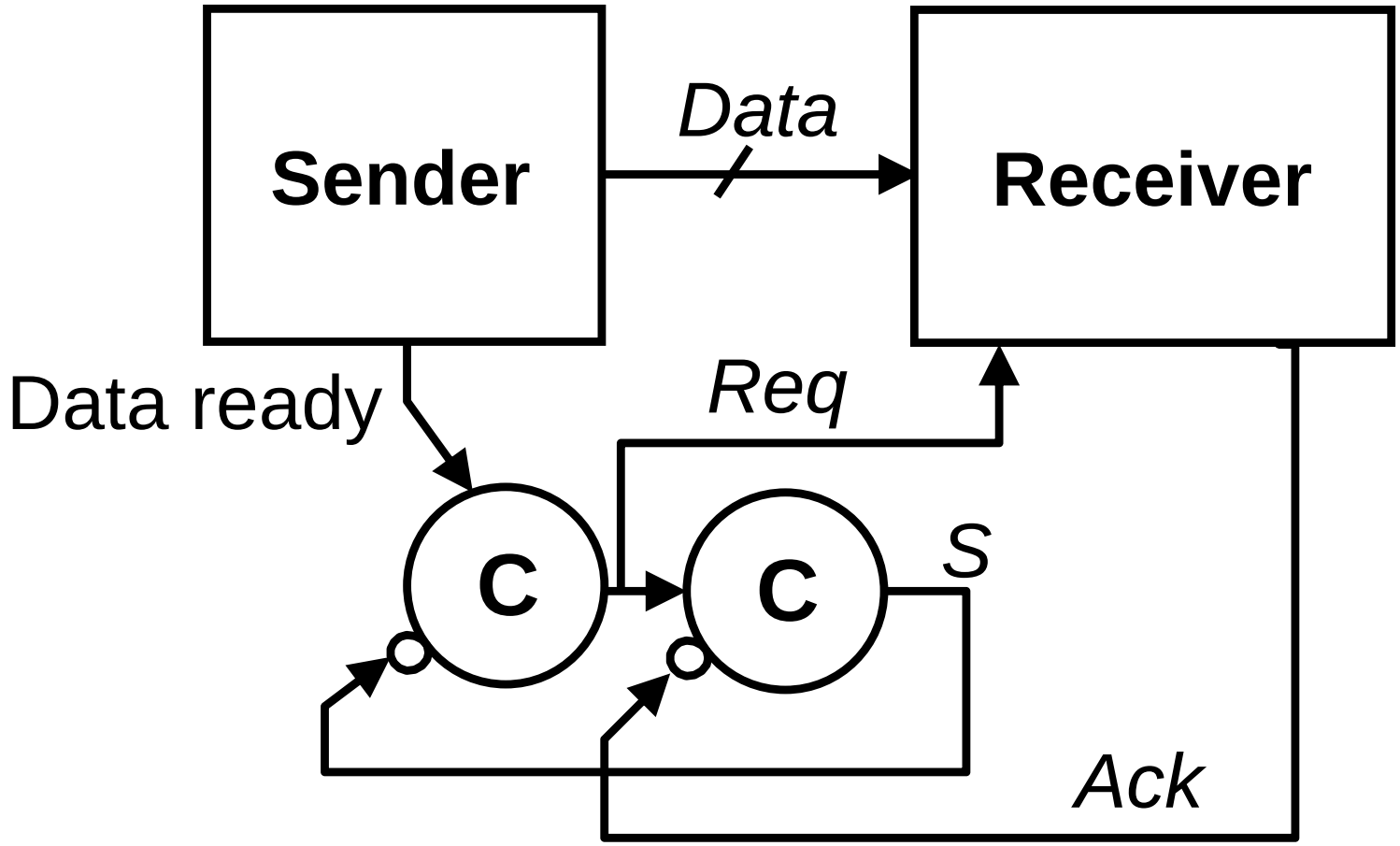
- **Simple to implement and good performance**
  - Low overhead beneficial for low power applications
- **Many logic devices level sensitive or sensitive to only one polarity of transition**
  - Event-triggered logic requires extra circuitry and state information
  - All C-elements must be initialized properly to avoid deadlock between logic stages (requires more devices, area, routing of reset signals)
- **Alternative signaling approach relies on bringing control signals back to initial state before commencing new cycle**

Four Phase (Return-to-Zero) Protocol



- **All controlling signals back to initial state each cycle**

Four Phase Protocol Implementation



- **Four phase protocol can be implemented with two C-elements and two inverters**

Four Phase Protocol Issues

- **More complex and requires more overhead than two phase**
- **More robust implementation of handshaking**
  - Logic does not deal with arbitrary transitions, only considers rising/falling edges and logic levels
  - Easy to interface with traditional circuit styles
- **Preferred implementation for self-timed pipelines**
- **Two phase used when sender and receiver far apart**
  - Long delays on request and acknowledge signals degrade performance

Synchronous vs. Asynchronous for Power

- **Asynchronous has advantage of inherent higher speed, therefore allows more voltage scaling**
  - Eliminates large global clock net
- **Asynchronous disadvantages: circuit overhead, design complexity**
  - Overhead adds capacitance, leakage current (increasingly important)
  - Difficult to design correctly
- **Synchronous, or similar styles such as replica-based ring oscillators, likely to remain dominant**