# EEC 216 Lecture #12: Power Electronics

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# Outline

#### Announcements

- Review: Energy Scavenging
- Wrap-Up: Energy Scavenging Example 3
- Variable-Voltage Design
- Basics of DC/DC Conversion
- Low Resolution Controller Design

#### Announcements

#### **Final Projects**

- 1. A. Chang, Sliding Mode Control DC/DC Conversion (Guilar '07)
- 2. X. Chen, Power Estimation of LDPC (Chen '04)
- 3. Y. Cheuk, <u>CPL-Based Dual Supply Adder</u> (Chatterjee '04)
- 4. J. Chieh, <u>Dual Edge-Triggered Level-Converting Flip-Flops</u> (Mahmoodi '04)
- 5. C. Chiem, <u>Gate-Leakage Reduction</u> (Guindi '03)
- 6. S. Hsu, <u>Subthreshold SRAM</u> (Verma '08)
- 7. N. Irizarry, Energy-Recovery Adder (Tzartzanis '95)
- 8. X. Jing, Sliding Mode Control DC/DC Conversion (Guilar '07)
- 9. S. Le, Asynchronous Adiabatic Logic (Arsalan '07)
- 10. H. Liao, Capacitively-Coupled Wire Drivers (Ho '07)
- 11. F. Maker, Mobile Phone Power Characterization (Viredaz '03)
- 12. H. Pham, Maximum Power Point Tracking (Guilar '06)
- 13. Y. Wang, Biological Computing Power Estimation ()
- 14. Y. Zhang, Dual Edge-Triggered Flip-Flops (Llopis '96)
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### **Energy Density of Nuclear Materials**

<b>ENERGY CONTENT</b>	
TECHNOLOGY	ENERGY DENSITY (MILLIWATT-HOURS/MILLIGRAM)
Lithium-ion in a chemical batter	y 0.3
Methanol in a fuel cell*	3
Tritium in a nuclear battery**	850
Polonium-210 in a nuclear batte	ry** 57 000
*Assuming 50 percent efficiency **Assuming 8 percent efficiency and 4 years (	of operation
	ah anaray danaity?

- How do you exploit this high energy density?
  - Fission, fusion not practical

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Lal, Spectrum 04

### **Nuclear Microbatteries**

#### Radioisotope thermoelectric generators (RTGs)

- Traditional approach from NASA space probes
- Rely on Seebeck effect: heating one end of metal bar causes electrons with high thermal energy to flow to other end, inducing a voltage
- Washing machine-sized generator
- Uses Plutonium-238 (high energy radiation generates enormous heat)
- Doesn't scale down well

### Photodiode based current source

- Radioactive material (Ni-63) emits beta particles (e<sup>-</sup>) which induce current in *pn* junction
- Produces 3 nW, still too low for most applications

### **Cantilever Beam Mechanical Generator**

- Radioactive piezoelectric generator
- Converts energy from beta particles to mechanical energy first
  - Higher efficiency than direct conversion through diodes
  - Compatible with MEMS technology
- Consists of 4 square mm radioactive material below free end of cantilever Si beam
  - Piezoelectric material bonded to beam
  - Radiated beta particles (electrons) embed in Si beam, charging it negatively and causing it to bend
  - As beam deforms, piezo material deforms and generates a voltage
  - Beam touches radioactive material and shorts charge, causing cantilever to oscillate and inducing AC voltage

### **Radioactive Piezoelectric Generator 1**



# Energy stored in deformed silicon beam (like stretching a spring) Lal, Spectrum 04

#### **Radioactive Piezoelectric Generator 2**



When the cantilever bends to the point where the copper sheet touches the radioactive source, the electrons flow back to it, and the attractive force ceases. The cantilever then oscillates, and the mechanical stress in the piezoelectric plate creates an imbalance in its charge distribution, resulting in an electric current.

Lal, Spectrum 04

- Peak power pulses of 100 mW for one cantilever
- Integrate several for other applications

### **Sources of Ambient Energy**

#### Solar Power

- Photovoltaics convert light to electricity
- Very well established (calculators, watches, etc.)
- Electromagnetic Fields
  - Usually inductively coupled, sometimes uses antenna
  - Used in smart cards, pacemaker charging, RFID tags

#### • Thermal Gradients

- Woven into clothing, power off skin-air temperature gradient (ISSCC 03)
- Fluid Flow
- Mechanical Vibration

### **Energy Scavenging Output Power Examples**

Energy Source	Transducer	Output Power
Walking	Piezoelectric	5 W [15]
(Direct Conversion)		
Thermal	Thermoelectric	30 mW [36]
Solar	Photovoltaic Cell	20 mW [35]
Magnetic Field	Coil	1.5 mW [13]
Walking	Discrete	$400 \mu W$
(Vibration)	Moving Coil	
High Frequency	MEMS	100 µW [11]
Vibration	Moving Coil	
Small Fluid Flow	Turbine	50 µW
RF Field	Antenna	5 μW [12]

#### • From Amirtharajah, PhD 99

### **Vibration Based Energy Harvesting**

- Embedded sensor applications
  - Monitoring of vibrating machinery: turbines, internal combustion engines, machine tools
  - Monitoring of vehicles: ships, submarines, aircraft
  - Monitoring of structures: load-bearing walls, staircases, buildings, bridges
  - Applications demand long lifetime in environments without continuous exposure to incident light
- Wearable devices
  - Wrist worn biomedical monitor
  - Computers embedded in clothing, smart textiles

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## Variable Supply Voltage Intuition

- Seen in past lectures that voltage scaling is key to reducing power consumption
- If circuits can operate faster than required throughput, two alternatives for power reduction:
  - Run at full speed until computation is complete and then gate clock for remaining time
  - Reduce voltage and slow down circuit until computation consumes all available time

#### • Voltage reduction results in better energy savings

- So far have seen systems which fix voltage at design time
- If throughput requirement varies at runtime, would like to vary voltage as well to minimize power

#### **Expected Power Reduction: DSP Example**

$$E(r) = CV_0^2 T_s f_r r \left[ \frac{V_T}{V_0} + \frac{r}{2} + \sqrt{r \frac{V_T}{V_0} + (r/2)^2} \right]^2$$

E(r) is energy versus normalized sample processing rate

- C : average switched capacitance
- $T_s$  : sample period
- $f_r$  : clock frequency at maximum supply voltage  $V_{\it ref}$
- r : normalized processing rate, i.e. clock speed normalized to  $f_r$

$$V_0 = \frac{\left(V_{ref} - V_T\right)^2}{V_{ref}}$$

### **Energy Reduction With Variable Supplies**



# **Power Scaling With Variable Supplies**

- Fixed voltage (chosen to meet delay constraints in maximum throughput situation):
  - Power decreases linearly due to clock gating as throughput requirement decreases
- Arbitrary voltage levels:
  - Choose arbitrary voltage to minimize power at throughput
  - Minimal power implementation
- Discrete voltage levels
  - Fixed over a range of throughputs, scales linearly over range through clock gating
- Dithered discrete levels
  - Generate intermediate point by switching between levels
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### DC / DC (Switching) Converter Fundamentals



#### **Example Current and Voltage Waveforms**



# **Switching Converter Tradeoffs**

#### • Passive lowpass filter reduces output ripple

- Larger L and C, lower cutoff frequency, lower switching frequency, less dynamic power dissipation in FET gates
- Larger volume and higher cost for inductor and cap

### • FET switch sizing tradeoff

- Wider devices result in less resistive power loss...
- ...but wider gates increase dynamic power dissipation
- Duty cycle waveform generation
  - Analog circuitry allows finest granularity control...
  - ...but dissipates static power, consumes area (matching, reduce short channel effects)
  - All digital implementation preferred

### Need low power control loop implementation

# **Duty Cycle PWM Generation Alternatives**

- Traditional approach uses linear voltage ramp and comparator
  - Two threshold crossings generate leading and trailing edges of duty cycle waveform
  - Varying thresholds modulates duty cycle
  - Requires analog implementation to create voltage ramp, set comparator thresholds
- Use counter with fast clock to create "digital" linear ramp
  - Logic generates leading and trailing edges when count reaches thresholds
  - Easy to implement, but granularity limited to counter width
  - Dynamic power dissipation due to high frequency clock

# **Digital Duty Cycle Waveform Generation**

- Use delay line and selector to steer edges for creating D(t) leading and trailing edges
  - Less dynamic power than fast clocked counter approach
  - Glitches potentially an issue if clocking an RS flip-flop as an edge-to-pulse converter
- Digital generation techniques (counter or delay line) can be integrated with digital PID controller
  - Maximum flexibility for setting closed-loop dynamics
  - Eliminates static power associated with analog circuits like opamps
  - Use microcontroller to implement more complex control loops, e.g. adaptive

### **Digital PWM Generation Circuits**



Fig. 10. PWM generator architectures. (a) Fast-clocked counter approach. (b) Pure delay-line approach.

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#### • From Goodman, JSSC 98 <sub>24</sub>

### **PID Controller Transfer Function**



Fig. 6. Control-loop frequency-domain model.

• From Wei, JSSC 99

#### **Fast-Clocked Counter PID Controller**



Fig. 7. Digital-loop architecture.

From Wei, JSSC 99

#### **Fast-Clocked Counter PID Controller Power**



Fig. 9. Fixed-frequency controller power breakdown.

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#### • From Wei, JSSC 99

#### **Delay Line PWM Using DLL Example**



Fig. 11. (a) PWM generator block diagram. (b) PWM generator delay line.

• From Goodman, JSSC 98 <sub>28</sub>

## **DLL PWM Waveform Generation**

#### • DLL fixes switching frequency of converter

- Can adjust to set output ripple requirement (higher frequency, lower ripple)
- Requires analog circuit implementation
  - Static power dissipation for charge-pump current sources
  - If current-starved delay elements with analog control voltages used, they also dissipate static power
  - Voltage headroom required to bias current sources appropriately, increased dynamic power for other nodes
- Look for simpler implementation for energy scavenging applications for less controller overhead

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### **Coil Example Using Performance Feedback**



### Performance Feedback Design

- Earlier approaches targeted specific output voltages
  - Requires analog circuits or A/D conversion in feedback loop, implying higher power
  - Maps indirectly to desired optimization: minimal supply voltage for required performance or throughput
- Performance feedback closes loop directly around optimization criteria
  - Compensates for input voltage, temperature, silicon process variations simultaneously
  - Also cope with changes in desired performance (variable supply voltage design)
  - Can implement with all digital control using replica critical path ring oscillators

## Low Resolution Digital Control

- Continuous time analog control loops easy to analyze using linear systems theory
  - Analog circuits or A/D converters for mixed-signal controller consume power, require matched components, sensitive to noise generated by integrated digital systems
- Prefer to implement all digital controller with minimum bits of resolution to save power
  - Discrete time system with quantized error and control variables
  - Finite resolution creates nonlinear dynamics
  - Sample rate for error signal and update rate for controller output affect dynamics also (think of it as variable "gain" when integrated using something like a counter)

### **Digital Controller Block Diagram**



- All digital feedback loop uses frequency comparator to generate error and Up/Down counter as integrator
  - T<sub>s</sub> counter used to determine error sample rate
  - Sample rate chosen ad hoc depending on configuration

#### **Frequency Comparator**



### **Digital PWM Controller Architecture**



# • Free running oscillator must be guaranteed to run sufficiently fast compared to LC cutoff frequency

 Eliminates overhead of DLL in exchange for real-time variable switching frequency, output voltage ripple

### **Bootstrap Circuit**



- Boot circuit switches between backup supply and regulator output for controller circuits
  - Enable derived from frequency comparator error signal

### Low Resolution Regulator Step Response



#### Limit cycle caused by low resolution error feedback

### **Bootstrapping Operation**



#### Switches controller from backup voltage V<sub>bk</sub> to V<sub>out</sub>

## **Voltage Regulation in Operation**



### DC / DC Converter Test Chip



#### • Integrates regulator, power FETs, test load DSP circuit

### **DC / DC Converter Test Chip Specifications**

Area	2609 μm x 2609 μm
Transistor Count	5 K
Process	0.8 µm CMOS
NMOS Threshold Voltage	$V_{tN} = 0.70 \text{ V}$
PMOS Threshold Voltage	$V_{tP} = -0.87  V$
Controller Power	5.71 $\mu$ W ( $f_{ref} = 500$ kHz, $V_{dd} = 1$ V)
Subband Filter Power	4.75 $\mu$ W ( $f_{ref} = 500$ kHz, $V_{out} = 1$ V)
Switch Drive Power	$7.50 \mu W  (V_{in} = 1.07 V)$
1 Generator Excitation	23 ms of valid DSP operation
	11,700 cycles
	2,340 operations

 Operates for 23 ms with single moving-coil generator excitation

• Power consumption much less than 400  $\mu\text{W}$  average expected output for vibration due to walking