EEC 216 Winter 2008 Design Project #2

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Issued: February 15, 2008
Due: February 29, 2008, at 5 PM in 3173 Kemper.

Reading: Wang and Chandrakasan, "A 180-mV Subthreshold FFT Processor Using a Minimum Energy Design Methodology", 2005. A recent work on low power subthreshold circuit design [1]. Available on the course web page.

1 Subthreshold Minimum Energy 32 Bit Adder

Part 1.1 Specification: The goal for this design project is to apply the circuit techniques, architectures, and clocking methodologies discussed in class to a specific application. Your assignment is to implement a 32 bit adder for a signal processing datapath. The performance constraint is fixed at 100 MHz, i.e. new inputs must be accepted every 10 ns and a new sum must be produced every 10 ns. You may pipeline the system if you wish. Choose an architecture, logic style, clocking scheme (if you wish) and power supply voltage to minimize the power consumption while meeting the performance constraint. Your supply voltage will likely be somewhere between 200 mV and 400 mV, well into the subthreshold regime of operation for our example CMOS process. Use the 45 nm model file and the file `macros.sp` to specify the transistors for the simulation. The design must meet the following specifications:

- Implement the adder design in a separate Hspice file which includes the adder as its own subcircuit and the voltage source implementing the power supply at the voltage for your design. The idea is to make sure the adder can be incorporated into a separate test bench spice file to verify operation.
- The adder will have two summand inputs labeled A and B and a single carry input labeled Cin. Use the convention A32 A31 ... A0 to label each input port. You must also include a clock input labeled Clk, whether you use a clocked design or not. The sum output will be labeled S and follow the same convention as the inputs for naming the individual bits. There will also be a single carry out output Cout. Use the following spice file template as a guide:

```
Vvdd vdd gnd dc=1.0

.subckt add32 A31 A30 A29 A28 A27 A26 A25 A24
+             A23 A22 A21 A20 A19 A18 A17 A16
+             A15 A14 A13 A12 A11 A10 A09 A08
+             A07 A06 A05 A04 A03 A02 A01 A00
+             B31 B30 B29 B28 B27 B26 B25 B24
+             B23 B22 B21 B20 B19 B18 B17 B16
+             B15 B14 B13 B12 B11 B10 B09 B08
+             B07 B06 B05 B04 B03 B02 B01 B00
+             Cin Cout    Clk
+             S31 S30 S29 S28 S27 S26 S25 S24
+             S23 S22 S21 S20 S19 S18 S17 S16
+             S15 S14 S13 S12 S11 S10 S09 S08
+             S07 S06 S05 S04 S03 S02 S01 S00
.ends
```

- The adder must produce valid logic levels at its outputs of $V_{OH} \geq 0.9V_{DD}$ and $V_{OL} \leq 0.1V_{DD}$, under worst case I_{ON}/I_{OFF} conditions.
- Simulate and plot the minimum average energy point of your design as V_{DD} and clock frequency are scaled. Evaluate the energy at the maximum frequency for each voltage between 100 mV and 1.0 V at 100 mV increments. Your plot should look like Figure 4 in [1].

Part 1.2 Report: Turn in a report describing your design. Explain your design choices in the context of the adder specification. In particular, be sure to justify the logic style, architecture, and clocking/pipelining scheme if used. Discuss your approach to minimizing the power consumption. The report must include the following:

- A block diagram showing the adder architecture.
- Circuit schematics for each of the key elements showing the logic style and device sizes.
- A description of the inputs which exercise the critical path of the adder and a simulation output showing that the performance constraint is met under the critical path input condition. Be sure to justify the choice of input vectors.
- If your architecture requires potentially long wires, discuss how their resistance and capacitance will impact the critical path. If your architecture does not require them, be sure to justify why it is not necessary to include wire parasitics in the critical path analysis.
- The average power of the adder along with a description of the simulation methodology used to arrive at the measurement (what inputs were used, how long the simulation was run, etc.)

- An estimate of the average power-delay product (PDP) and average energy-delay product (EDP) for your adder.
- A plot of the energy vs. voltage performance and minimum energy point for your adder.
- A list of references for any circuits or architectures not covered in class (unless you invent a new one)!

References

[1] A. Wang and A. Chandrakasan, "A 180-mV subthreshold FFT processor using a minimum energy design methodology," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 310–9, January 2005.

EEC 216 Winter 2006 Design Project #2 Summary

Name:

Grading:

Part	Maximum	Score
Following Directions	15	
Meeting Requirements	35	
Minimizing Power	25	
Report	25	
Total	100	

Summary:

Parameter	**Design (Simulated Results)**
Critical Path Delay	
Power (Average)	
PDP (Average)	
EDP (Average)	