EEC 216 Winter 2008 Design Project #1

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Instructions: This first design project is a simple one designed to familiarize you with basic CMOS logic design styles and the use of HSPICE.

1. Your project will be evaluated in part by electronically processing your final file. You should email your file to **ramirtha@ece.ucdavis.edu** and the email subject should be "216 project 1". It is your responsibility to make sure that your file is compatible with HSPICE. An edited version of your final file will be resimulated using HSPICE.
2. Turn in a writeup answering the questions listed below.
3. Fill in the summary table and turn in the summary page as the cover sheet for your project writeup.

Reading: Two papers on the basics of Differential Cascode Voltage-Switch Logic, including the introductory paper from IBM [1] and a comparison with conventional CMOS by Chu and Pulfrey [2].

Simulation: This problem requires extensive use of HSPICE. For information on running HSPICE on the UCD ECE department network, follow this URL:

`http://www.ece.ucdavis.edu/cad/hspice/index.html.`

If you want to use another version of Spice (e.g. PSpice, Berkeley Spice, Spectre), you must get permission from the instructor first.

Device Models: This problem relies on freeware models from the Predictive Technology Model Group [3, 4]. Download the model file `45nm_MGHiK.sp` from the course web site and include it in your Spice deck. You should already have the models from completing Problem Set 1.

1 Low Power Logic Design

Part 1.1 (5 points) **Complex Gate Design.** Design a static CMOS logic gate to implement the following logic function:

$$F = \overline{E \bullet (A + BC) + D}. \tag{1}$$

Part 1.2 (10 points) **Static CMOS: Sizing.** Size the devices in the pullup network of the gate you designed in Problem 1.1 to equalize the worst case 10% to 90% rise and fall times of the gate. Use minimum size NMOS devices in the pulldown network and use the smallest total PMOS width in the pullup network to equalize the transition times.

Download and modify the HSPICE deck `dp1.sp` from the course web page. A template for the complex gate is already in the deck. You will also need the `macros.sp` file.

Part 1.3 (5 points) **Static CMOS: Minimum V_{DD}.** Find the minimum power supply voltage of the gate you designed in Problem 1.1 which satisfies a 2 GHz clock frequency. Use an FO4 load and inverters to drive the input signals. Use stimulus inverters which are connected to the same power supply as the complex gate.

Part 1.4 (15 points) **Static CMOS: Average Power Over Input Cases**. One approach to characterizing power for a complex logic gate is to simulate it over all possible combinations of inputs and measure the average power. In the gate you designed in Problem 1.1, there are 5 inputs for 32 possible input bit patterns. Simulate all 32 patterns applied to the gate's inputs at a 2 GHz clock frequency and report the average power at the supply voltage you found in Problem 1.3. Use an FO4 load and inverters to drive the input signals. Be sure to connect the power supplies of the load inverters to a different supply than the one you measure average power through so their dissipation does not contaminate the result. However, input loading is a concern so be sure to use stimulus inverters which are connected to the same power supply as the complex gate. Turn in your HSPICE deck along with the reported average power. Note that although the sequence in which the inputs are applied will affect the power, you may use any sequence you find convenient for this problem, but be sure to apply enough vectors to get what you believe to be an accurate power estimate. Justify your choice of vectors and the number applied.

Part 1.5 (10 points) **Internal Node Capacitances**. Determine the worst case sequence of input patterns which results in charging the largest amount of internal node capacitance in the pullup and pulldown networks of the gate. Draw a timing diagram for this input pattern. Simulate this worst case pattern and compare the power dissipation due to charging the worst case internal node capacitance to the average power measured above. How pessimistic is it to assume the worst case? Turn in your HSPICE deck.

Part 1.6 (10 points) **Pseudo NMOS: Sizing**. Implement the logic function in a pseudo NMOS logic style. Size the PMOS load device such that its width is equivalent to the worst case resistance of the pullup network you sized in Problem 1.2. Size the NMOS devices in the pulldown network such that $V_{OL} \leq 0.1V_{DD}$ under any input combination which pulls the output low. Turn in an HSPICE simulation plot confirming your choice of sizing.

Part 1.7 (5 points) **Pseudo NMOS: Minimum V_{DD}.** Find the minimum power supply voltage of the gate you designed in Problem 1.6 which satisfies a 2 GHz clock frequency. Use an FO4 load and inverters to drive the input signals. Use stimulus inverters which are connected to the same power supply as the complex gate.

Part 1.8 (10 points)**Pseudo NMOS: Average Power Over Input Cases**. Repeat the average power measurement from Problem 1.4 for the pseudo NMOS gate at the supply voltage you found in Problem 1.7. Turn in your HSPICE deck along with the reported average power. How does the average power for this style compare to the static CMOS design? Under these test conditions, what does the average power tell you about the tradeoff between dynamic power and static power for pseudo NMOS logic?

Part 1.9 (10 points) **Dynamic Logic: Sizing**. Implement the logic function in a dynamic N-block logic style with minimum-sized NMOS devices. Use a minimum-sized NMOS device as the evaluation transistor. Size the PMOS precharge device such that the precharge rise time equals the worst case evaluation fall time. Turn in your HSPICE deck and a plot showing the precharge and evaluate phases verifying logic gate operation.

Part 1.10 (5 points) **Dynamic Logic: Minimum V_{DD}.** Find the minimum power supply voltage of the gate you designed in Problem 1.9 which satisfies a 2 GHz clock frequency. Use an FO4 load and inverters to drive the input signals. Use stimulus inverters which are connected to the same power supply as the complex gate.

Part 1.11 (10 points) **Dynamic Logic: Average Power Over Input Cases**. Repeat the average power measurement from Problem 1.4 for the dynamic gate at the supply voltage you found in Problem 1.10. Be sure to incorporate the power of the inverters driving the precharge and evaluate devices as well. Turn in your HSPICE deck along with the reported average power. How does the average power for this style compare to the static CMOS design?

Part 1.12 (10 points) **Differential Cascode Voltage-Switched Logic (DCVSL): Sizing**. Implement the logic function in a DCVSL logic style. Size the PMOS and NMOS devices in the pullup and pulldown networks such that the rise and fall times are equal and less than 300 ps. You may assume the true and complement versions of the input signals are available. Turn in an HSPICE simulation plot confirming your choice of sizing.

Part 1.13 (5 points) **DCVSL: Minimum V_{DD}.** Find the minimum power supply voltage of the gate you designed in Problem 1.12 which satisfies a 2 GHz clock frequency. Use an FO4 load and inverters to drive the input signals. Use stimulus inverters which are connected to the same power supply as the complex gate.

Part 1.14 (10 points)**DCVSL: Average Power Over Input Cases**. Repeat the average power measurement from Problem 1.4 for the DCVSL gate at the supply voltage you found in Problem 1.13. Turn in your HSPICE deck along with the reported average power. How does the average power for this style compare to the static CMOS design?

Part 1.15 (10 points) **Design Discussion: Mixed-Signal System-On-Chip**. Your company is shipping a highly integrated chip for cellular phone applications. The chip incorporates a very noise-sensitive RF signal processing analog path with substantial DC current biasing and a large high performance DSP. Low power consumption is a high priority because this is a portable application. Your manager wants you to inform her of all the issues regarding the choice of logic style for the digital modules on-chip and make a recommendation of which circuit technique to use. Discuss the pros and cons of using each of the logic styles analyzed in the preceding parts in the context of the design problem. What are the tradeoffs between static power dissipation, dynamic dissipation, speed, and noise generated by the logic? Fill in the summary table by ranking each style from 1 to 4 in each category, with 1 being the best for that category, and make your design recommendation.

EEC 216 Winter 2008 Design Project #1 Summary

Name:

Grading:

Part	Maximum	Score
1.1 Complex Gate Design	5	
1.2 Static CMOS: Sizing	10	
1.3 Static CMOS: V_{DD}	5	
1.4 Static CMOS: Avg. Power	15	
1.5 Internal Node Capacitance	10	
1.6 Pseudo NMOS: Sizing	10	
1.7 Pseudo NMOS: V_{DD}	5	
1.8 Pseudo NMOS: Avg. Power	10	
1.9 Dynamic: Sizing	10	
1.10 Dynamic: V_{DD}	5	
1.11 Dynamic: Avg. Power	10	
1.12 DCVSL: Sizing	10	
1.13 DCVSL: V_{DD}	5	
1.14 DCVSL: Avg. Power	10	
1.15 Discussion	10	
Total	130	

Logic Style Summary:

Style	Static Power	Dynamic Power	Speed	Noise Generation	Design Risk
Static CMOS					
Pseudo NMOS					
Dynamic					
DCVSL					
Recommendation					

References

[1] L. G. Heller, W. R. Griffin, J. W. Davis, and N. H. Thoma, "Cascode voltage switch logic: A differential CMOS logic family," in *ISSCC 1984 Digest of Technical Papers*, February 1984, pp. 16–7.

[2] K. M. Chu and D. L. Pulfrey, "A comparison of CMOS circuit techniques: Differential cascode voltage switch logic versus conventional logic," *IEEE Journal of Solid-State Circuits*, vol. SC-22, no. 4, pp. 528–32, August 1987.

[3] Nanoscale Integration and Modeling (NIMO) Group, Arizona State University. (2006, December) Predictive technology model (ptm). latest.html. [Online]. Available: http://www.eas.asu.edu/~ptm/

[4] W. Zhao and Y. Cao, "New generation of predictive technology model for sub-45 nm early design exploration," *IEEE Trans. Electron Devices*, vol. 53, no. 11, pp. 2816–23, November 2006.