EEC 210 Fall 2008 Midterm

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Name:

Instructions: This test consists of 4 problems and 14 pages, including the cover sheet. Please make sure that you have all of them. This is an open-book, open-notes test. State any assumptions you make and show complete work to receive credit. The time limit is 80 minutes. The problems are weighted as shown below:

Grading:

Problem	Maximum	Score
1	13	
2	13	
3	12	
4	12	
Total	50	

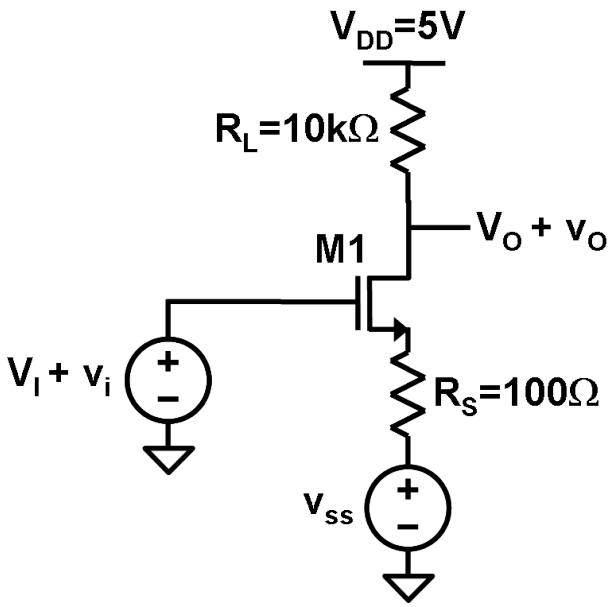

Figure 1: Resistive load amplifier.

1 Resistive Load Amplifier

Figure 1 shows a resistively loaded amplifier. Source v_{ss} is a small-signal source only. For this problem, use the transistor parameters in Table 1.

Parameter	NMOS
V_t	1 V
L_d	0
X_d	0
k'	300 μA/V^2
γ	0
W/L	16/3
λ	1/100 V^{-1}

Table 1: Problem 1 Transistor Parameters.

Problem 1.1 (**4 points**) Find the large-signal input voltage V_I such that the large-signal output voltage $V_O = 3$V. You may ignore channel length modulation for this part.

Problem 1.1 (cont.)

Problem 1.2 (**4 points**) Find the small-signal voltage gain $a_{v1} = \frac{v_o}{v_i}$.

Problem 1.3 (**4 points**) Find the small-signal voltage gain $a_{v2} = \frac{v_o}{v_{ss}}$.

Problem 1.4 (**1 point**) Find the power supply rejection ratio $\left|\frac{a_{v1}}{a_{v2}}\right|$.

2 Differential Amplifier

Figure 2 shows the circuit schematic for a differential amplifier. For this problem, use the transistor parameters in Table 2. Assume that all transistors are biased in saturation and the following circuit parameters: $I_{TAIL} = 400\mu$A, $R_{TAIL} = 500$ kΩ, $R_S = 50\Omega$, $(W/L)_1 = (W/L)_2 = 10, (W/L)_3 = (W/L)_4 = 8$.

Parameter	NMOS	PMOS
V_t	1 V	-1 V
L_d	0	0
X_d	0	0
k'	400 μA/V^2	100 μA/V^2
χ	0.25	0.25
λ	0.01 V^{-1}	0.01 V^{-1}

Table 2: Problem 2 Transistor Parameters.

Problem 2.1 (**4 points**) Draw and label the small-signal differential-mode half circuit, and find the differential-mode gain, $\frac{v_{od}}{v_{id}}$, where $v_{id} = v_{i1} - v_{i2}$ and $v_{od} = v_{o1} - v_{o2}$.

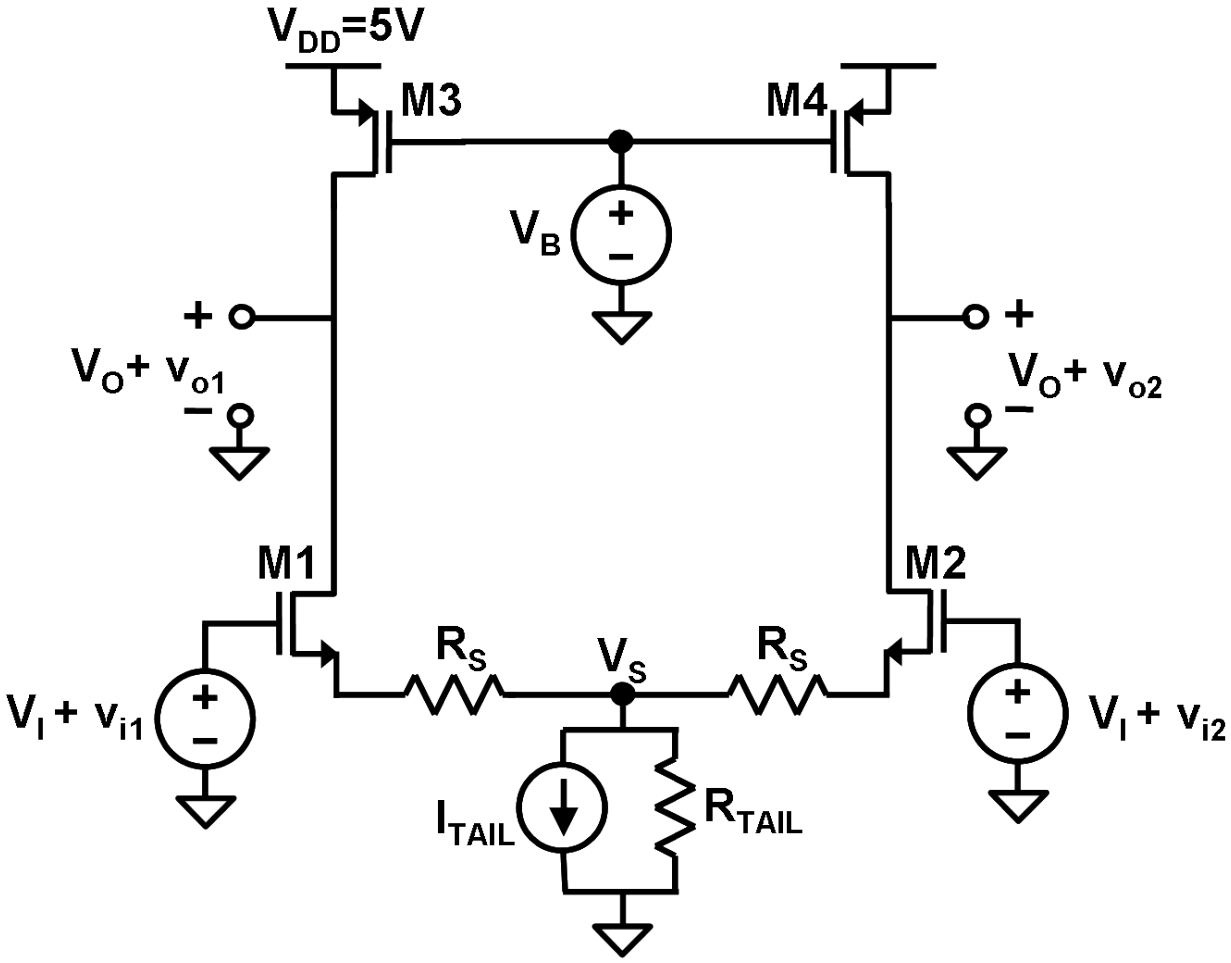

Figure 2: Differential amplifier.

Problem 2.2 (**4 points**) Draw and label the small-signal common-mode half circuit, and find the common-mode gain, $\frac{v_{oc}}{v_{ic}}$, where $v_{ic} = 0.5(v_{i1} + v_{i2})$ and $v_{oc} = 0.5(v_{o1} + v_{o2})$.

Problem 2.3 (**2 points**) Find the common-mode rejection ratio (CMRR).

Problem 2.4 (**3 points**) Find the large-signal common-mode input voltage V_I assuming $V_{DS1} = V_{DS2} = 1.5\text{V}$ and the current through R_{TAIL} is $2\mu\text{A}$.

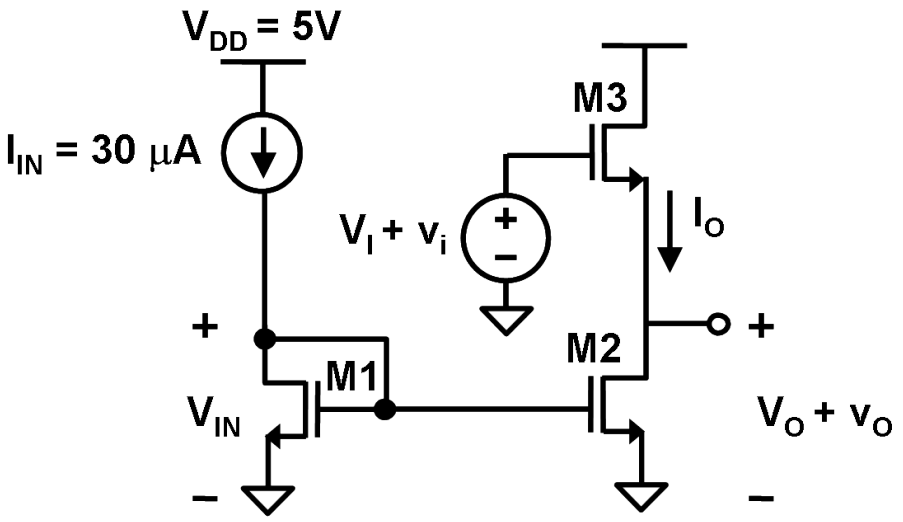

Figure 3: Active load amplifier.

3 Active Load Amplifier

Figure 3 shows an actively loaded amplifier circuit. For this problem, use the transistor parameters in Table 3. For the circuit in Figure 3, assume the following circuit parameters: $(W/L)_1 = 2$, $(W/L)_2 = 20$, and $(W/L)_3 = 30$.

Parameter	NMOS	PMOS
V_t	1 V	-1 V
L_d	0	0
X_d	0	0
k'	300 μA/V^2	100 μA/V^2
χ	0.2	0
λ	0.02 V^{-1}	0.02 V^{-1}

Table 3: Problem 3 Transistor Parameters.

Problem 3.1 (**4 points**) Find the large-signal input voltage V_I required to make the systematic current gain error 0. You can ignore λ when calculating the large-signal current.

Problem 3.1 (cont.)

Problem 3.2 (**3 points**) Find the minimum large-signal input voltage $V_I(MIN)$.

Problem 3.3 (**2 points**) Find the output resistance R_o.

Problem 3.4 (**3 points**) Find the small-signal voltage gain $a_v = \frac{v_o}{v_i}$.

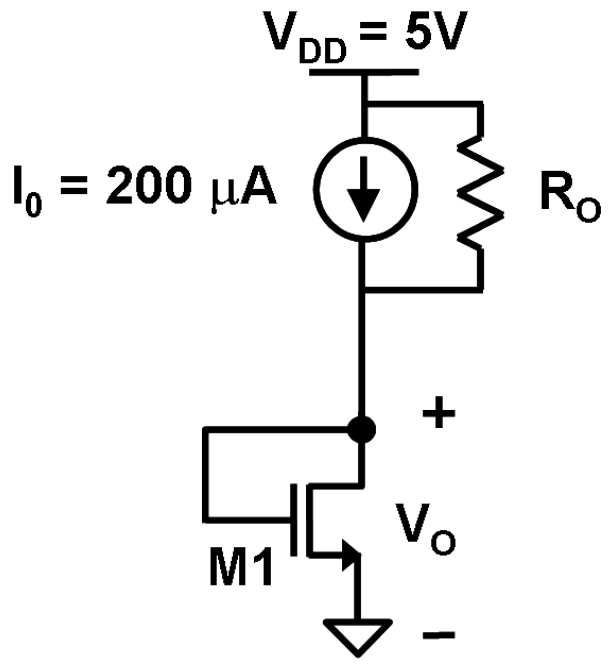

Figure 4: Voltage reference.

4 Voltage Reference

Figure 4 shows a proposed temperature and supply voltage-independent voltage reference circuit. For this problem, use the transistor parameters in Table 4. Note the temperature dependence of V_t and k'.

Parameter	NMOS	PMOS
V_t	1 V	-1 V
$\frac{dV_t}{dT}$	-2.3 mV/K	-3 mV/K
L_d	0	0
X_d	0	0
k'	100 μA/V^2 $\left(\frac{T}{300K}\right)^{-1.5}$	50 μA/V^2
γ	0	0
λ	0	0

Table 4: Problem 4 Transistor Parameters.

Problem 4.1 (**5 points**) Find W/L such that $\frac{dV_O}{dT} = 0$ at $T = 300\text{K}$ in the limit as $R_O \to \infty$.

Problem 4.2 (**3 points**) Find the target output voltage V_O at the operating point found in Problem 4.1.

Problem 4.3 (**4 points**) Suppose $R_O = 100\text{k}\Omega$. Find the approximate power supply gain $\frac{\Delta V_O}{\Delta V_{DD}}$ assuming $V_{DD} \gg V_O$. Hint: $(1+x)^{\frac{1}{2}} \approx 1 + \frac{x}{2}$ for small x.