EEC 210 Fall 2008 Design Project

Rajeevan Amirtharajah
Dept. of Electrical and Computer Engineering
University of California, Davis

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1 Self-Biased Op Amp with External Compensation

Send your HSPICE file to **ramirtha@ece.ucdavis.edu** before Friday, December 5, 2008 at 5:00 PM. Your report is due in my office that afternoon. Slide it under the door if I am unavailable.

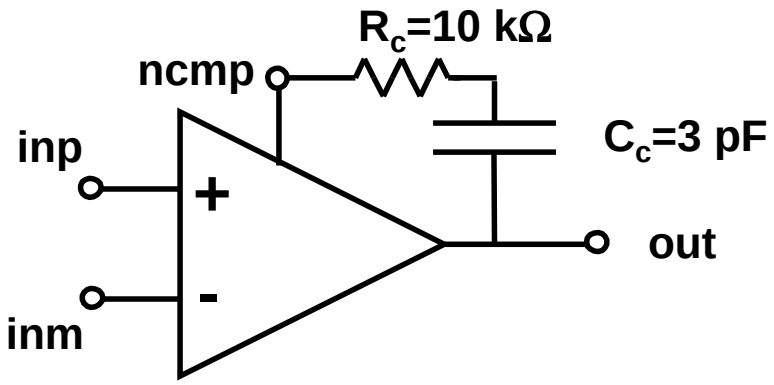

Figure 1: Op amp with external *RC* network compensation.

Specification: The goal for this design project is to apply the circuit techniques and design insight discussed in class to a develop an operational amplifier. The amplifier is compensated with a fixed external *RC* network as shown in Figure 1. The design must meet the following specifications:

1. The only elements you may use in your amplifier circuit are resistors, NMOS transistors, and PMOS transistors.

2. The topology shown in Figure 2 may be used as a starting point. Note that the differential pair is self-biased (no current source reference) and that you must use this circuit as the first stage.

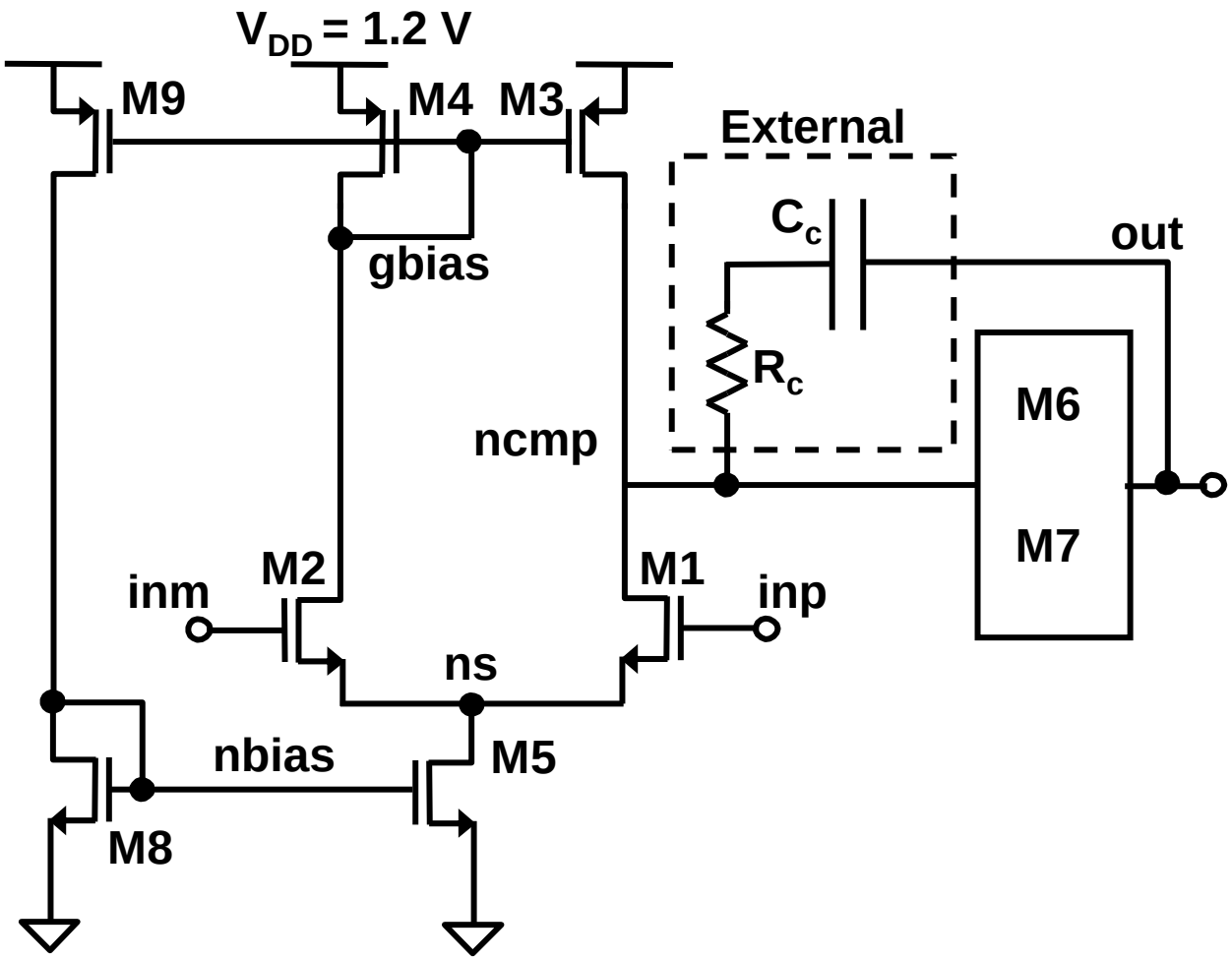

Figure 2: Two stage CMOS op amp with a self-biased differential stage and external compensation.

3. It is suggested that the second stage be a two transistor single-ended amplifier whose topology you may choose. However, it cannot be biased using ideal current sources (you may only use transistors and resistors). For a two transistor circuit, label the pullup device M6 and the pulldown device M7.

4. Download an HSPICE template file and the transistor model file for the project from the course web page. The template file includes some useful transistor macros and a subcircuit specification for the opamp, as well as an instantiation of the amplifier with the external compensation. You may add analysis and measurement commands as necessary, but do **not** change the amplifier subcircuit interface as your circuit will be resimulated using a testbench to verify its performance.

5. Assume an nwell-only CMOS process, therefore you may bias the PMOS bulk terminal if you desire using a practical bias network (no ideal voltage sources). The HSPICE three terminal FET macros automatically compute source/drain areas and perimeters

for you, so if you choose not to use them you must compute these parameters yourself.

6. We will assume scalable CMOS design rules, which requires dimensions to be specified in terms of a minimal length, λ, equal to $\frac{1}{2}$ times the minimum gate length for the process (130 nm for this project). The minimum device width is $5\lambda = 0.325$ μm to eliminate effects due to creating core device widths narrower than a single contact dimension.

7. The drawn channel length must be no less than $2\lambda = 0.13$ μm and no more than $20\lambda = 1.3$ μm. A length of $4\lambda = 0.26\mu$m helps reduce short channel effects.

8. The maximum ratio of matched devices is 20 (e.g., for scaling up bias currents). All matched devices should use unit devices. You may assume that there is no mismatch.

9. Your amplifier must operate with one power supply of value V_{DD} between nodes V_{DD} and ground. A requirement of this project is that the amplifier must meet all specifications with $V_{DD} = 1.2$ V.

10. Assume that the amplifier operates at room temperature, 27 °C.

11. The amplifier must satisfy several performance requirements, including gain, output swing, offset, and phase margin for stability.

    (a) The voltage gain at DC ($|v_o/v_{id}|$) must be > 8000. Measure the gain assuming an input common-mode voltage of $V_{DD}/2$.

    (b) The output-referred offset (V_{os}(OUT)) must be < 10 mV. The ideal output voltage is $V_{DD}/2$ for zero differential input voltage and an input common-mode voltage of $V_{DD}/2$.

    (c) The input-referred offset (V_{os}(IN)) must be < 1.25 μV.

    (d) The output swing must be > 0.75 V.

    (e) The input common-mode range (CMR) must be > 0.7 V.

    (f) The unity gain frequency (including the external compensation network) should be > 10 MHz.

    (g) The phase margin (including the external compensation network) should be $> 45°$.

    (h) The low frequency common-mode rejection ratio (CMRR) should be > 250.

    (i) The low frequency power-supply rejection ratio (PSRR^+) should be > 250.

    (j) The power supply rejection ratio (PSRR^+) at 25 kHz should be > 25.

    (k) The total power consumption should be < 10 μW.

    (l) The circuit area is defined for this project as the sum of the drawn gate areas of all MOS transistors plus the total resistor area. Assume the resistors are built using 1.3 μm width polysilicon with a sheet resistance of 100 Ω/sq. (the polysilicon sheet resistance is the resistance of a square region of polysilicon, i.e. a region for which the length is equal to the width). The transistor area should be < 70 μm^2 and the resistor area must be less than < 2000 μm^2.

Optimization: You should design your op amp to maximize the low frequency (DC) gain while satisfying all other project requirements.

Report: Turn in a report describing your design. Explain your design choices in the context of the amplifier specification. The report must include the following:

1. A circuit schematic showing both amplifier stages and any associated biasing. Label your circuit diagram to show all node and element names and provide a copy of the corresponding HSPICE input listing.

2. Address the following issues in a brief summary (no more than two pages).

   (a) Describe your choice and rationale for the second amplifier stage, including its biasing.

   (b) Describe your approach to sizing of devices in the first and second gain stages, including which devices are intended to be matched and why. Specify which regime of operation the devices are biased in.

   (c) Describe the operation of the self-biasing network M8-M9 and explain your approach to sizing the devices, including which devices are intended to be matched and why. Specify which regime of operation the devices are biased in.

3. Your project will be evaluated in part by electronically processing your final file. You should email your file to **ramirtha@ece.ucdavis.edu** and the email subject should be "210 project". It is your responsibility to make sure that your file is compatible with HSPICE. An edited version of your final file will be resimulated using HSPICE. Because your files will be resimulated, it is not necessary to include any HSPICE outputs in your report.

4. Fill in the following tables on performance and dimensions (with the labeled units) and turn in the next page as the cover sheet for your report. If you modified the circuit schematic from the nine transistors, zero resistors shown in Figure 2, please leave the last table blank and create a similar table for your circuit.

EEC 210 Fall 2008 Design Project Summary

Name:

Grading:

Criterion	Maximum	Score
Following Directions	20	
Meeting Requirements	40	
Maximizing DC Gain	20	
Report	20	
Total	100	

Performance		
Parameter	Specification	Design (Actual)
DC Gain (A_v(DC))	> 8000	
V_{os}(OUT)	< 10 mV	
V_{os}(IN)	$< 1.25\mu$V	
Output Swing	> 0.75 V	
Common-Mode Range (CMR)	> 0.7 V	
Unity Gain Frequency	> 10 MHz	
Phase Margin	$> 45^\circ$	
Common-Mode Rejection Ratio (CMRR) @ DC	> 250	
Power Supply Rejection Ratio (PSRR$^+$) @ DC	> 250	
Power Supply Rejection Ratio (PSRR$^+$) @ 25 kHz	> 25	
Power Consumption	< 10 μW	
Transistor Area	< 70 μm^2	
Resistor Area	< 2000 μm^2	

Dimensions						
Transistor	Length (λ)	Length (μm)	Width (λ)	Width (μm)	# Unit Devices	Area (μm^2)
M1						
M2						
M3						
M4						
M5						
M6						
M7						
M8						
M9						
Total	X	X	X	X	X	