# EEC 210 Fall 2005 Midterm

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#### Name:

**Instructions:** This test consists of 4 problems and 13 pages, including the cover sheet. Please make sure that you have all of them. This is an open-book, open-notes test. State any assumptions you make and show complete work to receive credit. The time limit is 80 minutes. The problems are weighted as shown below

#### Grading:

Problem	Maximum	Score
1	12	
2	16	
3	10	
4	12	
Total	50	

### 1 CMOS Inverter Amplifier

Figure 1 shows a CMOS inverter biased as a linear amplifier. For this problem, use the transistor parameters in Table 1.

Parameter	NMOS	PMOS
$V_t$	1 V	-1 V
$L_d$	0	0
$X_d$ k'	0	0
k'	$300 \ \mu A/V^2$	$100 \ \mu A/V^2$
$\gamma$	0	0
W/L	2	6
$\lambda$	$0.1 \ V^{-1}$	$0.1 \ V^{-1}$

Table 1: Problem 1 Transistor Parameters.

**Problem 1.1** (3 points) Assume  $V_I = 1.5$  V. For what range of  $V_O$  will the circuit best act as an amplifier? What is the output voltage swing?

**Problem 1.2** (2 points) Find the power dissipation assuming the bias conditions in Problem 1.1.

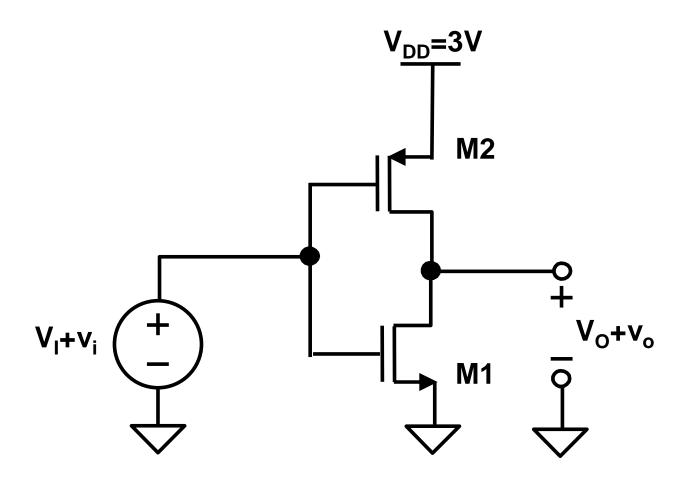


Figure 1: CMOS inverter as linear amplifier.

**Problem 1.3** (2 points) Find the small-signal output resistance  $R_o$  assuming the bias conditions in Problem 1.1.

**Problem 1.4** (**3 points**) Find the small-signal gain assuming the bias conditions in Problem 1.1.

**Problem 1.5** (2 points) Suppose that  $\gamma$  is nonzero and that through source-well biasing,  $V_{tn} = 1.25$  V and  $V_{tp} = -1.25$  V. How does this affect the small-signal gain (assume the bias conditions in Problem 1.1)?

### 2 Differential Amplifier

Figure 2 shows the circuit schematic for a differential amplifier. For this problem, use the transistor parameters in Table 2. Assume the following circuit parameters:  $I_{TAIL} = 590 \mu \text{A}$ ,  $R_{TAIL} = 30 \text{ k}\Omega$ ,  $R1 = 3 \text{ k}\Omega$ ,  $R2 = 6 \text{ k}\Omega$ ,  $(W/L)_1 = (W/L)_2 = 8$ .

Parameter	NMOS	PMOS
$V_t$	1 V	-1 V
$L_d$	0	0
$X_d \\ k'$	0	0
k'	$300 \ \mu A/V^2$	$100~\mu {\rm A/V^2}$
$\gamma$	0	0
$\lambda$	0	0

Table 2: Problem 2 Transistor Parameters.

**Problem 2.1** (3 points) Find  $V_I$  such that  $V_s = 300$  mV.

**Problem 2.2** (3 points) Find  $(W/L)_3 = (W/L)_4$  such that  $V_O = 1.5$  V, assuming the bias conditions you found in Problem 2.1.

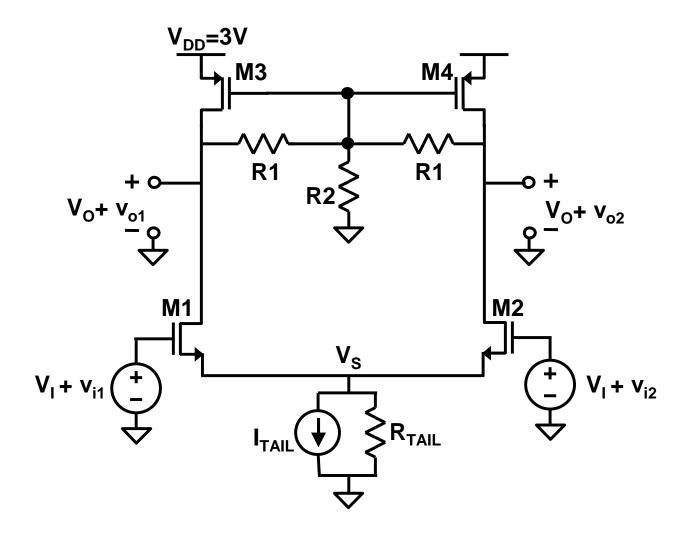


Figure 2: Differential amplifier.

**Problem 2.3** (4 points) Draw and label the small-signal differential-mode half circuit, and find the differential-mode gain,  $\frac{v_{od}}{v_{id}}$ , where  $v_{id} = v_{i1} - v_{i2}$  and  $v_{od} = v_{o1} - v_{o2}$ .

**Problem 2.4** (6 points) Draw and label the small-signal common-mode half circuit, and find the common-mode gain,  $\frac{v_{oc}}{v_{ic}}$ , where  $v_{ic} = 0.5(v_{i1} + v_{i2})$  and  $v_{oc} = 0.5(v_{o1} + v_{o2})$ .

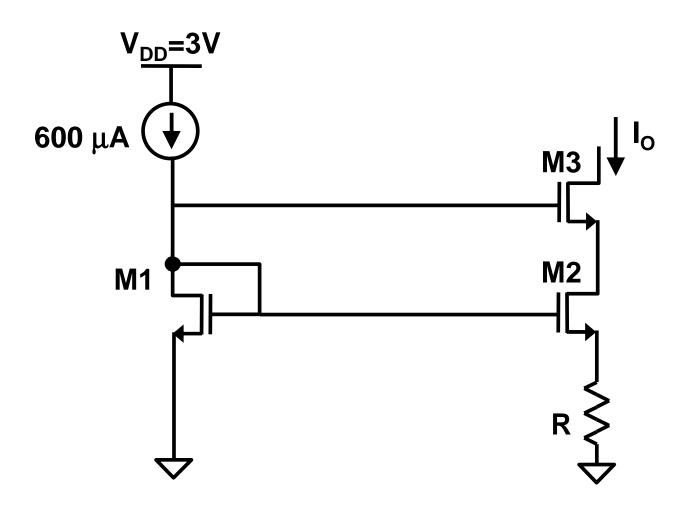


Figure 3: Current source.

# 3 Current Source

Figure 3 shows a current source circuit. For this problem, use the transistor parameters in Table 3. For the circuit in Figure 3, assume the following circuit parameters:  $R = 10 \text{ k}\Omega$ ,  $(W/L)_1 = (W/L)_3 = 2$ ,  $(W/L)_2 = 20$ .

Problem 3.1 (2 points) Find the output current  $I_O$ .

Parameter	NMOS	PMOS
$V_t$	1 V	-1 V
$L_d$	0	0
$X_d \\ k'$	0	0
k'	$300 \ \mu A/V^2$	$100 \ \mu A/V^2$
$\gamma$	0	0
$\lambda$	$0.1 \ V^{-1}$	$0.1 \ V^{-1}$

Table 3: Problem 3 Transistor Parameters.

**Problem 3.2** (3 points) Find the minimum output voltage  $V_{OUT}(MIN)$ .

**Problem 3.3** (3 points) Find the output resistance  $R_o$ .

**Problem 3.4** (2 points) Resistor R can be used to model the parasitic resistance associated with routing current sources for long distances on an IC. Find the largest value for R such that  $I_O$  is within 1% of the current reference value in Figure 3. Assume  $(W/L)_1 = (W/L)_3 = (W/L)_2 = 2$ .

## 4 Current Source Reference

Figure 4 shows a current reference circuit. For this problem, use the transistor parameters in Table 4. For the circuit in Figure 4, assume the following circuit parameters:  $R = 10 \text{ k}\Omega$ ,  $(W/L)_1 = (W/L)_2$ ,  $(W/L)_3 = 2$ , and  $(W/L)_4 = (W/L)_5 = (W/L)_6 = 6$ .

Parameter	NMOS	PMOS
$V_t$	1 V	-1 V
$L_d$	0	0
$egin{array}{c} X_d \ k' \end{array}$	0	0
k'	$300 \ \mu A/V^2$	$100~\mu {\rm A/V^2}$
$\gamma$	0	0
$\lambda$	0	0

Table 4: Problem 4 Transistor Parameters.

**Problem 4.1** (6 points) Find  $(W/L)_1 = (W/L)_2$  and  $(W/L)_7$  such that  $I_O$  is dependent on process parameters only (i.e., independent of bias point to first order).

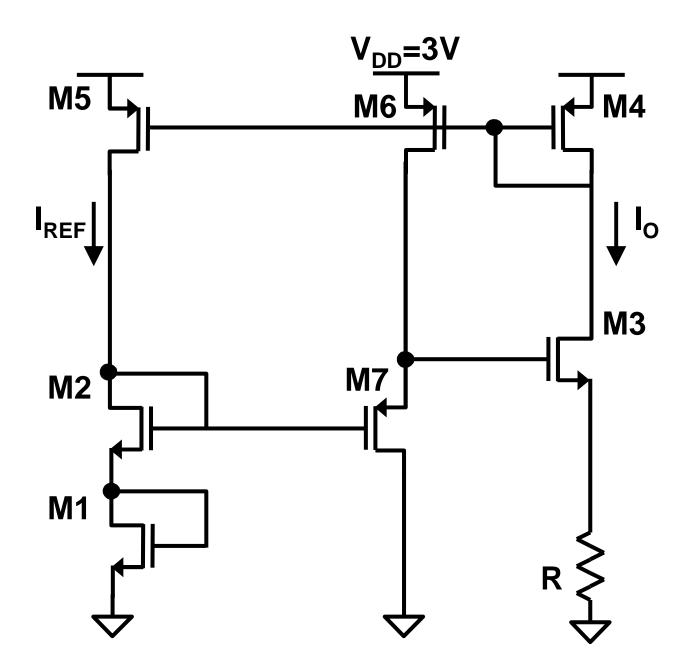


Figure 4: Current source reference.

**Problem 4.2** (6 points) One can model the thermal noise of resistor R as a small-signal current source  $i_n$  in parallel with R. Quantify the impact of the noise current source on the total output current  $I_O + i_o$ , assuming the bias point you found in Problem 4.1 and  $|i_n| = 1\mu A$ .