Problem 1 (5 points) Design a four-input static CMOS logic gate which implements the boolean expression \( f = \overline{ABC} + \overline{B} \) using minimum-sized transistors. Select the transistors such that the worst case rise and fall times of the output are equal to a minimum-sized inverter.

Problem 2 (5 points) A step input is applied at time \( t = 0 \) to the loaded inverter with after the step is applied.

Dimensions and initial conditions as shown below. What is the current immediately after the step is applied?

Problem 3 (5 points) A step input is applied at time \( t = 0 \) to the loaded inverter with after the step is applied.

\[
\begin{align*}
\text{Problem 1 (5 points) Design a four-input static CMOS logic gate which implements the boolean expression } f &= \overline{ABC} + \overline{B} \\
\text{using minimum-sized transistors. Select the transistors such that the worst case rise and fall times of the output are equal to a minimum-sized inverter.}
\end{align*}
\]