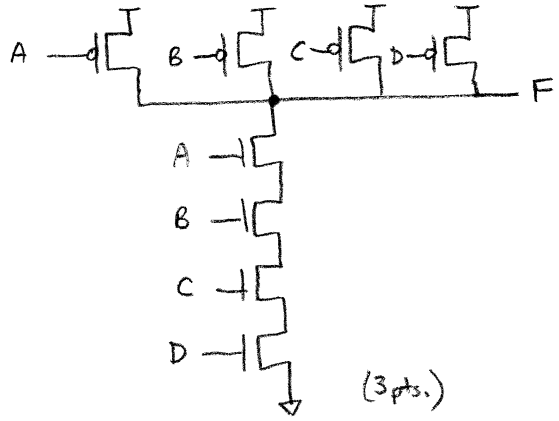
Quiz #2 **EEC118** **Spring 2011**

Name: Solutions Lab Section:_____

For all transistors: $L_{min} = 1\ \mu m$, $W_{min} = 1\ \mu m$, $V_{T,p} = -1\ V$, $\mu_p C_{ox} = (1/7) \times 10^{-3}\ A/V^2$, $\lambda_p = 0.0V^{-1}$, $V_{T,n} = 1\ V$, $\mu_n C_{ox} = (1/2) \times 10^{-3}\ A/V^2$, $\lambda_n = 0.0V^{-1}$.

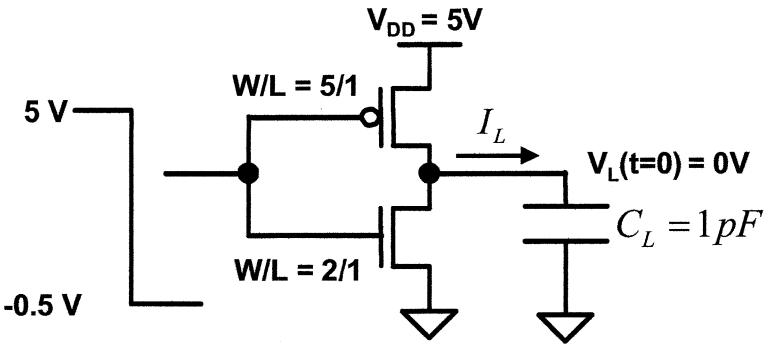
Problem 1 (5 points) Design a four-input static CMOS logic gate which implements the Boolean expression $F = \overline{A \bullet B \bullet C \bullet D}$. Clearly label all inputs, outputs, and power supply connections. Pick sizes for the transistors such that the worst case rise and fall times of the output are equal to a minimum-sized inverter.



$W_p = \frac{7}{2}\mu m$, $L_p = 1\mu m$ (1pt.)

$W_n = 4\mu m$, $L_n = 1\mu m$ (1pt.)

Problem 2 (5 points) A step input is applied at time t=0 to the loaded inverter with dimensions and initial conditions as shown below. What is the current I_L immediately after the step is applied?



$V_{GS,n} = -0.5V < V_{T,n} = 1V$ cutoff (1pt.)

$V_{GS,p} = -5.5V < V_{T,p} = -1V$

$V_{DS,p} = -5V < V_{GS,p} - V_{T,p} = -4.5V$ sat (1pt)

$I_L = I_{DS,p}$

$= \frac{\mu_p C_{ox}}{2}(V_{GS,p} - V_{T,p})^2 \left(\frac{W}{L}\right)$ (2pts.)

$= \frac{1}{2}\left(\frac{1}{7}\frac{mA}{V^2}\right)\left(\frac{5}{1}\right)(-5.5V - -1V)^2$

$= \boxed{7.23\ mA}$ (1pt.)