This examination is closed book and closed notes. Some formulas which you may find useful are listed in the back of the exam. Calculators are allowed, however using the calculator’s function memory to store course related material is NOT allowed and constitutes cheating on this exam.
For all problems, state any assumptions you make, show all work, and clearly mark your answers. Correct but unclear or ambiguous answers will not receive full credit.
Excerpts from the UC Davis Code of Academic Conduct state:

1. Each student should act with personal honesty at all times.

2. Each student should act with fairness to others in the class. This means, for example, that when taking an examination, students should not seek an unfair advantage over other classmates through cheating or other dishonest behavior.

3. Students should take group as well as individual responsibility for honorable behavior. This includes notifying the instructor or TA if you observe cheating.

I understand the honor code and agree to be bound by it.
Signature:
Name (printed): Solutions
Lab Section:

Grading:

<table>
<thead>
<tr>
<th>Problem</th>
<th>Maximum</th>
<th>Score</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td>55</td>
<td></td>
</tr>
</tbody>
</table>
1 Transistor Biasing

![FET biasing circuit](image)

Figure 1: FET biasing circuit.

**Problem 1.1** (8 points) Consider the NMOS bias circuit shown in Figure 1. Suppose we know that for the NMOS under bias, $V_{T0} = 1V$, $W/L = 4/1$, $\gamma = 0.35V^{1/2}$, $\lambda = 0 V^{-1}$, $\mu C_{ox} = 350 \mu A/V^{2}$, and $-2\Phi_F = 0.6$ V. Given that $V0 = 3V$ and $V1 = -2V$, find the following:

- $V_{Th} = \frac{1.293 V}{1.69 mA}$
- $I0 = \frac{1.69 mA}{1.69 mA}$

$$V_{Th} = V_{T0} + \sqrt{(2\Phi_F + V_{SB}) - \sqrt{(2\Phi_F})} \quad V_{SB} = -V1 - 2V \quad (\pm \phi^+.)$$

$$= 1V + 0.35 V^{1/2} (\sqrt{0.6V + 2V} - \sqrt{0.6 V}) \quad (\pm \phi^+)$$

$$= 1.293 V \quad (1 \phi^+)$$

$V_{DS} = V_{DD} = 1V$  
$V_{GS} - V_{Th} = V\phi - V_{Th} = 3V - 1.293V = 1.707 V > V_{DS}$

$\Rightarrow \text{linear} \quad (1 \phi^+.)$

$$I\phi = \frac{\mu C_{ox}}{2} \left( \frac{W}{L} \right) [2(V_{GS} - V_{Th})V_{DS} - V_{DS}^2] \quad (1 \phi^+.)$$

$$= \frac{\mu C_{ox}}{2} \left( \frac{W}{L} \right) [2(V\phi - V_{Th})V_{DD} - V_{DD}^2] = \frac{350 \mu A/\Omega^2}{2} \left( \frac{4}{1} \right) \left[ 2(1.707 V) 1V - 1V^2 \right] \quad (1 \phi^+)$$

$$= 1.69 mA$$
Problem 1.1 (cont.)
2 Inverter

Assume all transistor $W/L$ ratios are as shown in Figure 2 and the following transistor and supply voltage characteristics:

\[
\begin{align*}
V_{DD} &= 5 \text{ V} \\
V_{T0,n} &= 0.9 \text{ V} \\
\gamma_n &= 0.3 \text{ V}^{1/2} \\
\mu_n C_{ox} &= 250 \times 10^{-6} \text{ A/V}^2 \\
\lambda &= 0.02 \text{ V}^{-1} \\
V_{T0,p} &= -0.9 \text{ V} \\
\gamma_p &= 0.3 \text{ V}^{1/2} \\
\mu_p C_{ox} &= 100 \times 10^{-6} \text{ A/V}^2
\end{align*}
\]

![CMOS inverter diagram](image)

Figure 2: CMOS inverter.

**Problem 2.1 (2 points)** What is $V_{OL}$ (approximately) for the inverter circuit in Figure 2? Justify your answer.

Need $V_{GS} = V_{OUT} \geq V_{T,n}$ to be out of cutoff, so (1 pt.)

\[
V_{OL} \approx V_{T0,n} = 0.9 \text{ V}
\] (1 pt.)

**Problem 2.2 (8 points)** Find $W/L$ for the PMOS in Figure 2 such that $V_{OH} = 4.5 \text{ V}$.

$V_{OH} = 4.5 \text{ V} \geq V_{OUT}$ when $V_{IN} = 0 \text{ V}$

\[
\begin{align*}
\text{NMOS} & \quad V_{GS,n} = 4.5 \text{ V}, \quad V_{TH,n} = 3.6 \text{ V} \quad \therefore V_{DS,n} = 4.5 \text{ V} \quad (1 \text{ pt.}) \\
\text{PMOS} & \quad V_{GS,p} = -5 \text{ V}, \quad V_{TH,p} = -4.1 \text{ V} \quad \therefore V_{DS,p} = -0.5 \text{ V} \quad (1 \text{ pt.})
\end{align*}
\]
Problem 2.2 (cont.)

\[ I_{D_{S,N}} = I_{D_{S,P}} \quad (1 \text{ pt}) \]

\[ \frac{M_nC_{ox}}{2} \left( \frac{W}{L} \right)_n (V_{G_{S,n}} - V_{T,n}) \left( 1 + \lambda V_{D_{S,n}} \right) = \frac{M_pC_{ox}}{2} \left( \frac{W}{L} \right)_p \left[ 2 (V_{G_{S,p}} - V_{T,p}) V_{D_{S,p}} - V_{D_{S,p}}^2 \right] \quad (2 \text{ pts}) \]

\[
\frac{250 \mu A/V^2}{2} \left( \frac{3}{1} \right) (4.5V - 0.9V)^2 (1 + 0.02V^{-1})(4.5V) = \frac{100 \mu A/V^2}{2} \left( \frac{W}{L} \right)_p \left[ 2 (-5V - 0.9V)(-0.5V) - (-0.5V)^2 \right] \quad (2 \text{ pts})
\]

\[
\left( \frac{W}{L} \right)_p = 27.52/1 \quad (1 \text{ pt})
\]

Alternative: assume \( V_{\text{in}} = V_{\text{OL}} = 0.9 \text{ V} \), PMOS still \( \text{lin} \)

\[ I_{D_{S,P}} = \frac{100 \mu A/V^2}{2} \left( \frac{W}{L} \right)_p \left[ 2 (-4.1V - 0.9V)(-0.5V) - (-0.5V)^2 \right] \]

\[ \Rightarrow \left( \frac{W}{L} \right)_P = 35.91/1 \]
**Problem 2.3 (2 points)** Suppose that the only capacitances in the circuit of Figure 2 are the parasitic capacitances of the NMOS transistor. If the NMOS width \( W \) is doubled such that \( W/L = 6/1 \), what happens to the inverter fall time \( t_f \) (circle one)? Justify your answer.

- \( t_f \) almost doubles
- \( t_f \) is almost cut in half
- \( t_f \) stays about the same

\[
C_{\text{out}} = C_{gs,n} + C_{db,n} \quad (C_{gd,n} \text{ shorted out})
\]
\[
= C_{ox}WL \left( \frac{2}{3} \right) + C_jWL_D + C_{jm}(W+2L_D) \quad L_D \equiv \text{diffusion length}
\]
\[
\sim 2X \quad \text{if } W = 6
\]
\[
I_{0S,n} \propto \left( \frac{W}{L} \right) \sim 2X \quad \text{if } W = 6
\]
\[
\Delta t = \frac{C_{\text{out}} \Delta V}{I_{0S,n}} \sim \text{same}
\]

**Problem 2.4 (2 points)** Under the same assumptions as Problem 2.3, if the NMOS width \( W \) is doubled such that \( W/L = 6/1 \), what happens to the inverter rise time \( t_r \) (circle one)? Justify your answer.

- \( t_r \) almost doubles
- \( t_r \) is almost cut in half
- \( t_r \) stays about the same

\[
C_{\text{out}} \text{ almost doubles, but } I_{0S,p} \text{ stays same or net current to } C_{\text{out}} \text{ decreases since } I_{0S,n} \text{ increases,}
\]
\[
\text{Either way, } t_r \text{ must increase.}
\]

**Problem 2.5 (2 points)** Under the same assumptions as Problem 2.3, if the NMOS \( W/L \) is doubled to 6/1, what happens to \( V_{OH} \) as you designed in Problem 2.2 (circle one)? Justify your answer.

- \( V_{OH} \) increases
- \( V_{OH} \) decreases
- \( V_{OH} \) stays the same

\[
I_{0S,n} \text{ for any } V_{out} > V_{T,n} \text{ increases, so } I_{0S,p} \text{ must increase implying higher } V_{DS,p}.
\]
<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 1: Truth table for function $F$.

3 Static CMOS Logic Design

Problem 3.1 (2 points) Consider the function $F$ represented by truth Table 1. Write a Boolean expression for the logic function $F$.

$$ F = \overline{A \cdot (B+C)} $$

Problem 3.2 (6 points) Design a single multiple input CMOS logic gate which implements $F$. You may assume that both true and complement versions of the input signals are available (i.e., $A, \overline{A}, B, \overline{B}, C, \overline{C}$)

[Diagram of CMOS logic gate]
Problem 3.3 (6 points) Assume a minimum-sized inverter has PMOS ratio $W_P/L = 4/1$ and NMOS ratio $W_N/L = 2/1$. Choose appropriate $W/L$ ratios for the transistors in your circuit of Problem 3.2 such that the worst case rise and fall times are the same as a minimum-sized inverter. Indicate the sizes in your schematic above. Be sure to minimize the total area of the transistors.

Problem 3.4 (1 point) How many other implementations of logic function $F$ can you think of which use the same number of transistors as your design?

2. (swap $B+C$ PMOS in pullup, swap top & bottom in pulldown)
4 Static CMOS Logic Analysis

For this problem, assume the transistor characteristics as shown in Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{TO}$</td>
<td>1.0 V</td>
<td>-0.9 V</td>
</tr>
<tr>
<td>$\mu C_{ox}$</td>
<td>300 $\mu$A/V$^2$</td>
<td>100 $\mu$A/V$^2$</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>0.0 V$^{-1}$</td>
<td>0.0 V$^{-1}$</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>3.3 V</td>
<td></td>
</tr>
</tbody>
</table>

Table 2: Problem 4 Transistor Parameters.

Figure 3: CMOS logic gate. All dimensions in microns.

**Problem 4.1 (1 point)** Write a Boolean algebra expression for the function $F$ computed by the static CMOS logic gate shown in Figure 3.

$$ F = \overline{A \cdot B} = \overline{A} + \overline{B} \text{ (other more complex expressions possible...)} $$
Problem 4.2 (2 points) For the circuit shown in Figure 3 and assuming the only relevant capacitance is at output $F$, what set of input values gives the worst case rise time? Justify your answer.

\[ A = \Phi \text{ or } B = \Phi , \text{ output pulled up through two series PMOS} \]

\[ (1 \text{ pt.)} \]

\[ (1 \text{ pt.)} \]

Problem 4.3 (2 points) What set of input values gives the worst case fall time? Justify your answer.

\[ A = B = 1 , \text{ only combination which pulls output low} \]

\[ (1 \text{ pt.)} \]

\[ (1 \text{ pt.)} \]

Problem 4.4 (7 points) Assume the capacitance at output $F$ is 100 fF. Find the worst case fall time $t_f$ using the switch $RC$ model. Compute an average "ON" resistance using two resistance values, one at the beginning of the output falling transition and one at the end of the output falling transition, as specified in the definition of $t_f$.

\[ \text{NMOS equivalent } (W/L) = 2/1 \]

\[ (1 \text{ pt.)} \]

\[ I_{ds,n} (V_{out} = 0.9V_{DD}) \text{ NMOS } \text{ sat} \]

\[ V_{GS} = 3.3V , V_{DS} = 0.9 (3.3V) = 2.97V \]

\[ V_{GS} - V_{th,n} = 2.3 V \]

\[ (1 \text{ pt.)} \]

\[ I_{ds,n} = \frac{\mu n C_{ox}}{2} \frac{(W/L)}{(V_{GS} - V_{th,n})^2} = \frac{300 \mu A V^2}{2} \frac{(2)}{2} (3.3V - 1V)^2 = 1.587 mA \]

\[ (1 \text{ pt.)} \]

\[ R_1 = \frac{V_{OS,n}}{I_{ds,n}} = \frac{2.97V}{1.587 mA} = 1.871 \text{ k}\Omega \]

\[ (1 \text{ pt.)} \]

\[ I_{ds,n} (V_{out} = 0.1V_{DD}) \text{ NMOS } \text{ lin} \]

\[ V_{GS} = 3.3V , V_{DS} = 0.33V \leq 2.3 V = V_{GS} - V_{th,n} \]

\[ (1 \text{ pt.)} \]

\[ I_{ds,n} = \frac{\mu n C_{ox}}{2} \frac{(W/L)}{2 (V_{GS} - V_{th,n}) V_{DS} - V_{DS}^2} = \frac{300 \mu A V^2}{2} \frac{(2)}{2} (3.3V - 1.0V)^2 (0.33V) - (0.33V)^2 \]

\[ (1 \text{ pt.)} \]

\[ = 4.227 \mu A \]

\[ R_2 = \frac{V_{OS,n}}{I_{ds,n}} = \frac{0.33V}{4.227 \mu A} = 780.6 \Omega \]

\[ R_n = \frac{R_1 + R_2}{2} = 1.326 \text{ k}\Omega \]

\[ (1 \text{ pt.)} \]

\[ t_f = 2.2 \times 10^{-12} \text{ s} \times C_{out} = 2.2 (1.326 \text{ k}\Omega) (100 \text{ fF}) = 292 \text{ ps} \]

\[ (1 \text{ pt.)} \]
Problem 4.5 (4 points) Draw the schematic for a static CMOS logic gate which computes the same function as the circuit in Figure 4.1 but uses only four transistors. You do not need to find \( W/L \) for the transistors in your circuit.

\[\text{or equivalent...}\]

3 pts FETs + inputs
1 pt. \( V_{DD}, V_{SS}, \text{and} \)
Miscellaneous Formulas

MOSFET Threshold Voltage

\[ V_T = V_{T0} + \gamma \cdot \left( \sqrt{2 \phi_F + V_{SB}} - \sqrt{2 \phi_F} \right) \]

\[ \gamma = \frac{\sqrt{2q \cdot N_A \cdot \epsilon_{Si}}}{C_{ox}} \]

CMOS Inverter Switching Threshold

\[ V_{TH} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_r}} \cdot (V_{DD} - |V_{T0,p}|)}{1 + \sqrt{\frac{1}{k_r}}} \]

CMOS Inverter Propagation Delay Times

\[ \tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T,n})} \left[ \frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln \left( \frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1 \right) \right] \]

\[ \tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T,p}|)} \left[ \frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln \left( \frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1 \right) \right] \]

Switch Model Propagation Delay Times

\[ t_{PHL} = 0.69R_nC_L \]

\[ t_{PLH} = 0.69R_pC_L \]

\[ t_f = 2.2R_nC_L \]

\[ t_r = 2.2R_pC_L \]

Junction Capacitances

\[ C_{j0} = \sqrt{\frac{\epsilon_{Si} \cdot q}{2 \cdot \left( \frac{N_A N_D}{N_A + N_D} \right) \phi_0}} \]

\[ C_j(V) = \frac{AC_{j0}}{(1 - \frac{V}{\phi_0})^m} \]

\[ C_{eq} = AC_{j0}K_{eq} \]