EEC 118 Lecture #3: Inverters

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Announcements

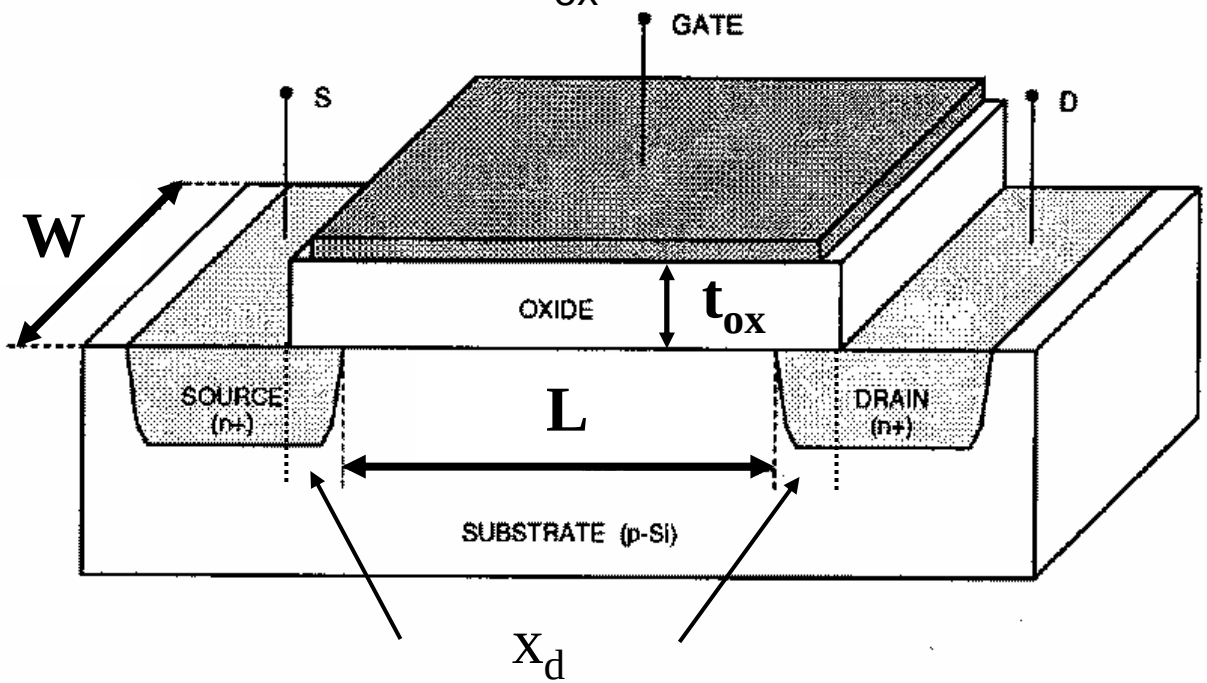
- **Lab 1 report due this week**
- **HW 2 due this Friday at 4 PM in box, Kemper 2131**

Outline

- **Review: MOSFET Regimes of Operation**
- **Lecture 2: Scaling, Parasitic Capacitances**
- **Inverter Operation: Rabaey 1.3.2, 5 (Kang & Leblebici, 5.1-5.3 and 6.1-6.2)**

Review: MOS Transistor Structure

- **Important transistor physical characteristics**
  - Channel length $L = L_D - 2x_d$ (K&L $L = Lgate - 2L_D$)
  - Channel width W
  - Thickness of oxide t_{ox}



MOSFET Drain Current Overview

Saturation: $$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2\left(1 + \lambda V_{DS}\right)$$

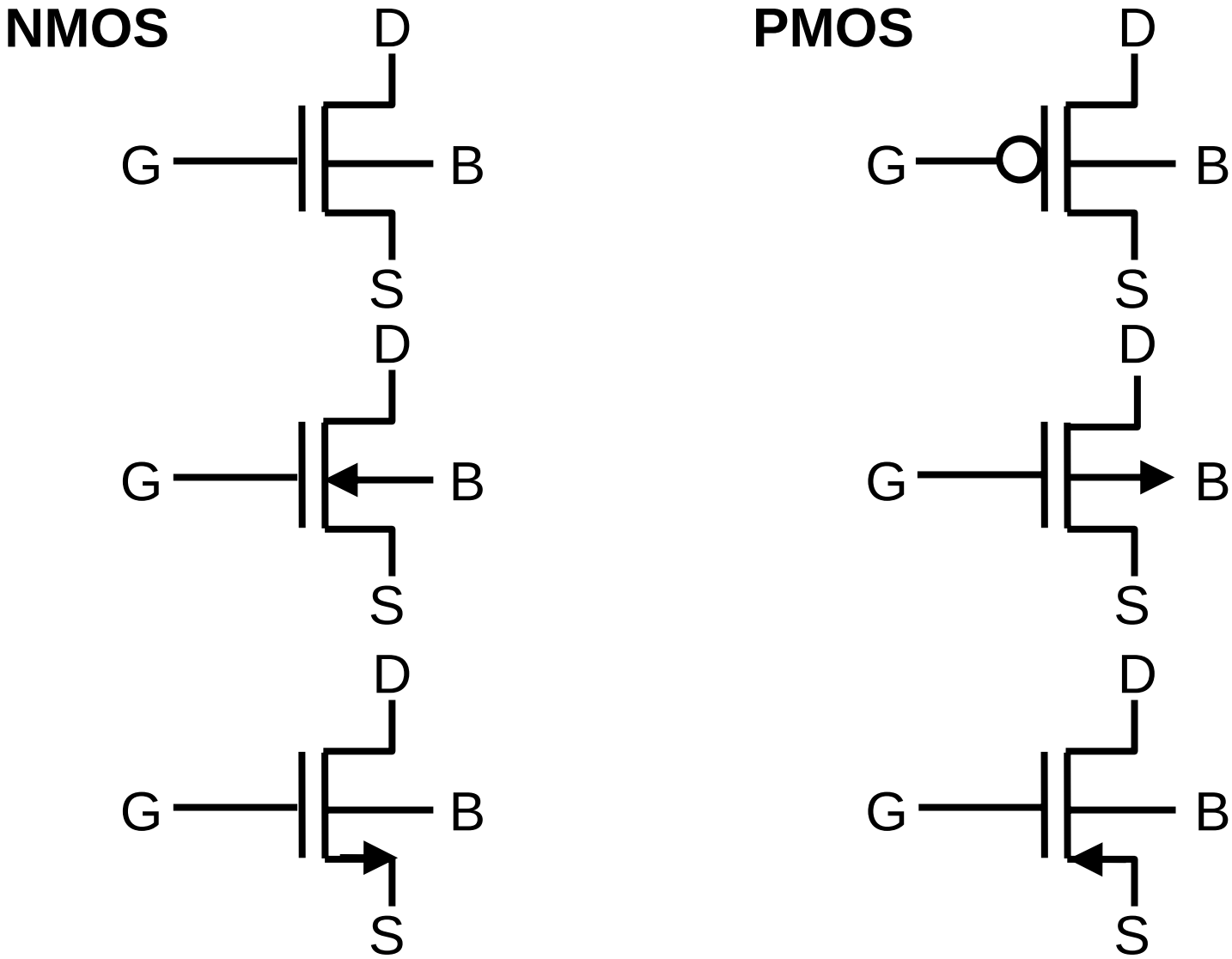
Linear (Triode, Ohmic):

$$I_D = \mu C_{ox}\frac{W}{L}\left(\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

Cutoff: $$I_D \approx 0$$

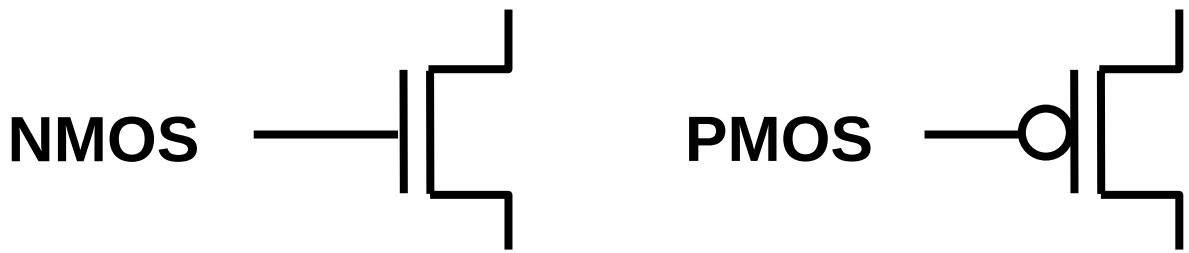
"Classical" MOSFET model, will discuss deep submicron modifications as necessary (Rabaey, Eqs. 3.25, 3.29)

MOS Transistor Symbols



Note on MOS Transistor Symbols

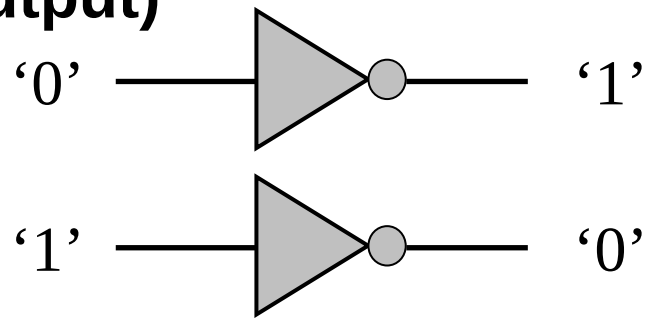
- **All symbols appear in literature**
  - Symbols with arrows are conventional in analog papers
  - PMOS with a bubble on the gate is conventional in digital circuits papers
- **Sometimes bulk terminal is ignored – implicitly connected to source or appropriate supply rail:**



- **Unlike physical bipolar devices, source and drain are usually symmetric**

Inverter Operation

- **Inverter is simplest digital logic gate (1 input, 1 output)**

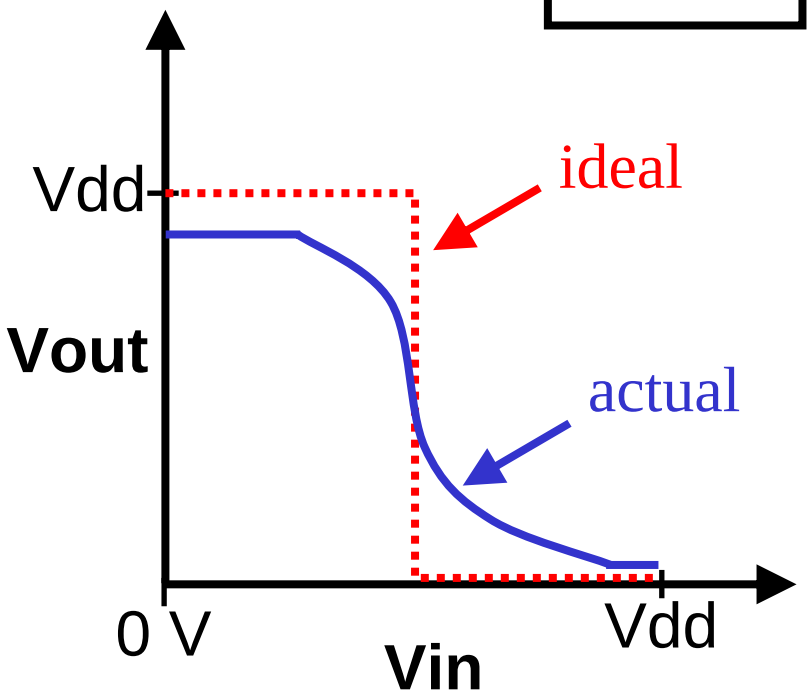


In	Out
0	1
1	0

- **Many different circuit styles possible**
  - Resistive-load
  - NMOS and Pseudo-NMOS
  - CMOS
- **Important static and dynamic characteristics**
  - Speed (delay through the gate)
  - Power consumption
  - Robustness (tolerance to noise)
  - Area and process cost

Inverter Model: Voltage Transfer Curve

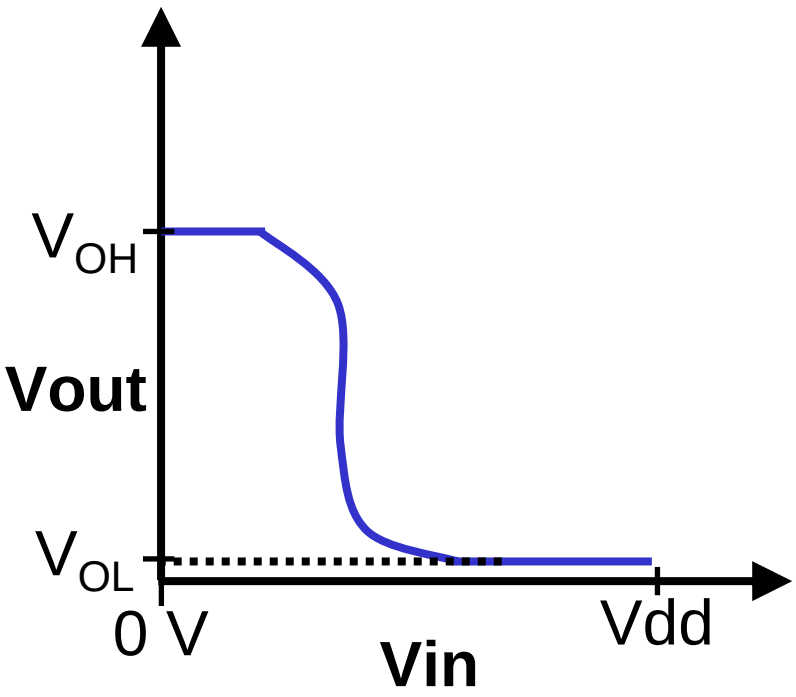
Voltage transfer curve (VTC): plot of output voltage Vout vs. input voltage Vin



Ideal digital inverter:

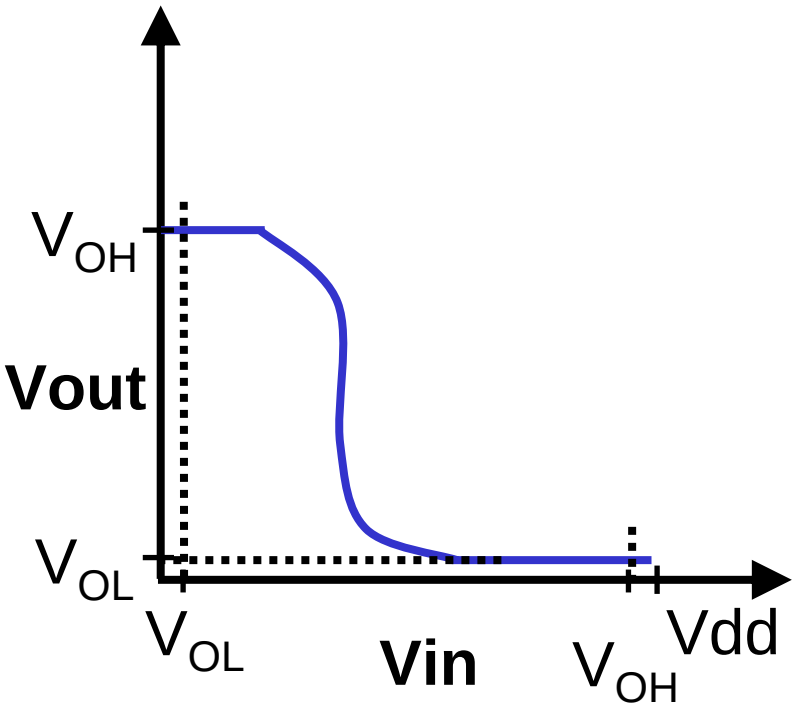
- When Vin=0, Vout=Vdd
- When Vin=Vdd, Vout=0
- Infinitely sharp transition region at inverter switching threshold

Actual Inverter: V_{OH} and V_{OL}



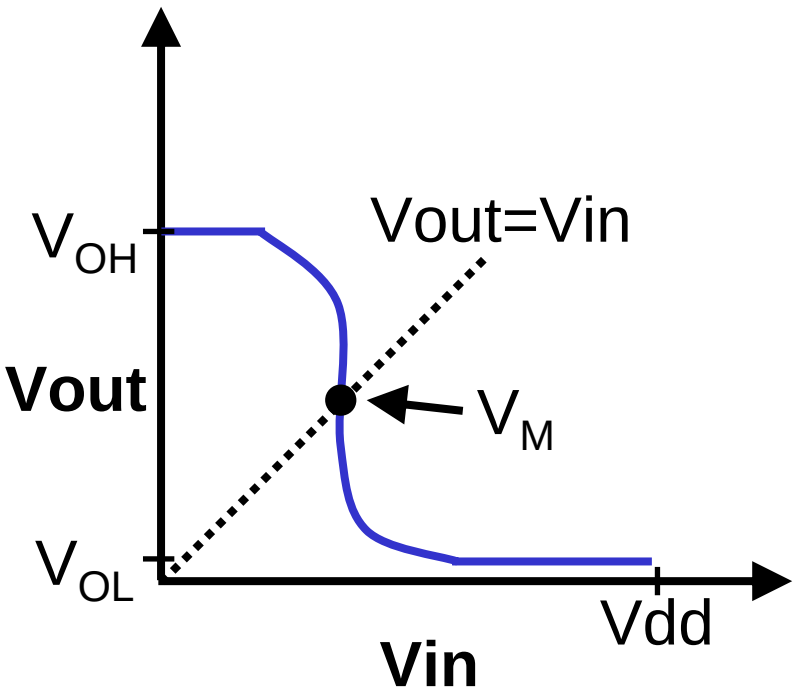
- **V_{OH} and V_{OL} represent the "high" and "low" output voltages of the inverter**
- **V_{OH} = output voltage when Vin = '0' (V Output High)**
- **V_{OL} = output voltage when Vin = '1' (V Output Low)**
- **Ideally,**
  - V_{OH} = Vdd
  - V_{OL} = 0 V

VOL and VOH



- **In transfer function terms:**
  - $V_{OL} = f(V_{OH})$
  - $V_{OH} = f(V_{OL})$
  - f = inverter transfer function
- **Difference (V_{OH}-V_{OL}) is the *voltage swing* of the gate**
  - *Full-swing logic* swings from ground to Vdd
  - Other families with smaller swings

Inverter Switching Threshold

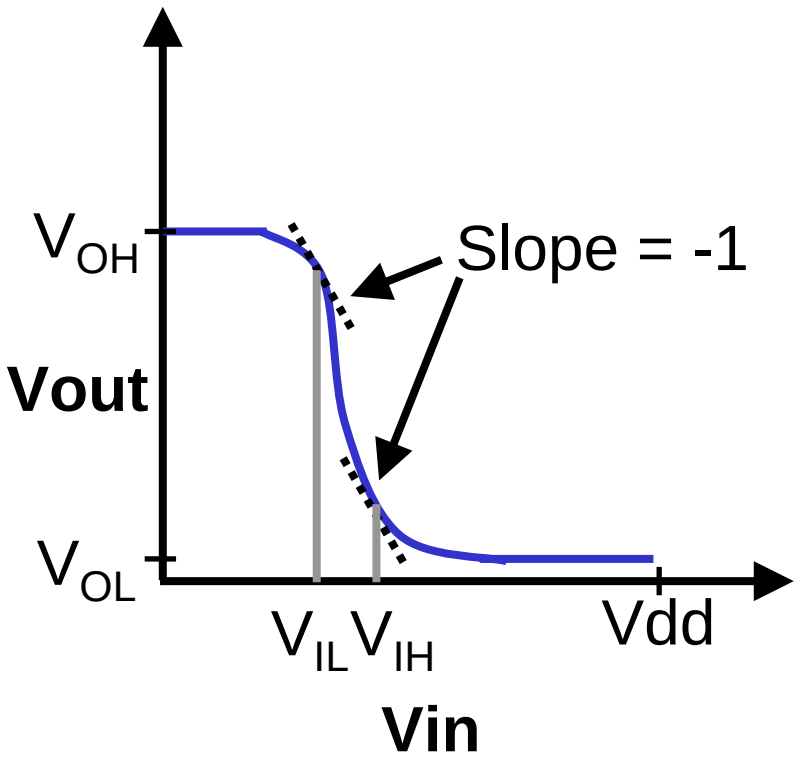


Inverter switching threshold:

- Point where voltage transfer curve intersects line Vout=Vin
- Represents the point at which the inverter switches state
- Normally, $V_M \approx Vdd/2$
- Sometimes other thresholds desirable

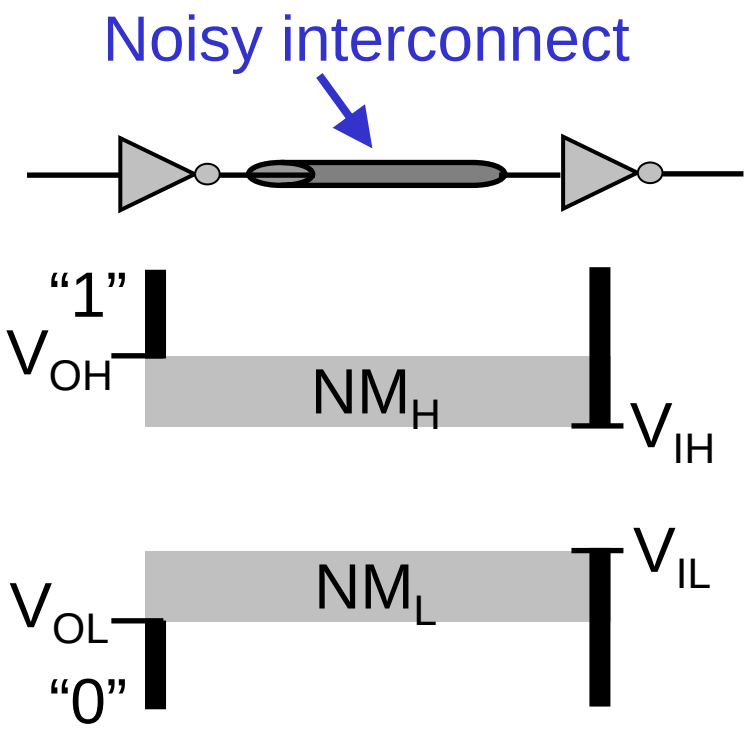
(K&L $V_{TH} = V_M$)

Noise Margins



- **V_{IL} and V_{IH} measure effect of input voltage on inverter output**
- **V_{IL} = largest input voltage recognized as logic ‘0’**
- **V_{IH} = smallest input voltage recognized as logic ‘1’**
- **Defined as point on VTC where slope = -1**

Noise Margins and Robustness



Ideally, noise margin should be as large as possible

- **Noise margin is a measure of the *robustness* of an inverter**
  - $N_{ML} = V_{IL} - V_{OL}$
  - $N_{MH} = V_{OH} - V_{IH}$
- **Models a chain of inverters. Example:**
  - First inverter output is V_{OH}
  - Second inverter recognizes input $> V_{IH}$ as logic '1'
  - Difference V_{OH}-V_{IH} is "safety zone" for noise

Noise Margin Motivation

- **Why are V_{IL}, V_{IH} defined as unity-gain point on VTC curve?**
  - Assume there is noise on input voltage V_{in}

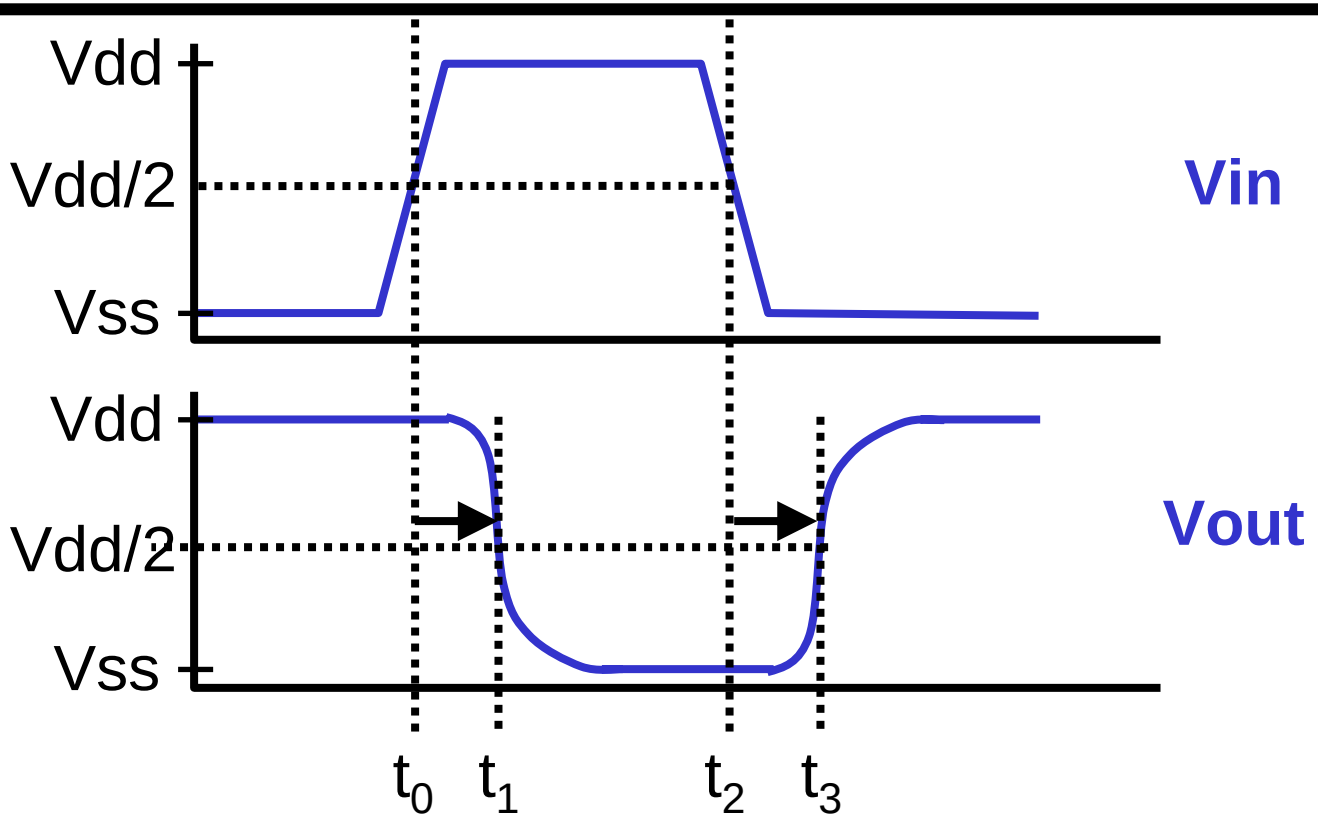
$$V_{out} = f\left(V_{in} + V_{noise}\right)$$

  - First-order Taylor series approximation:

$$V_{out} = f\left(V_{in}\right) + \frac{dV_{out}}{dV_{in}} V_{noise}$$

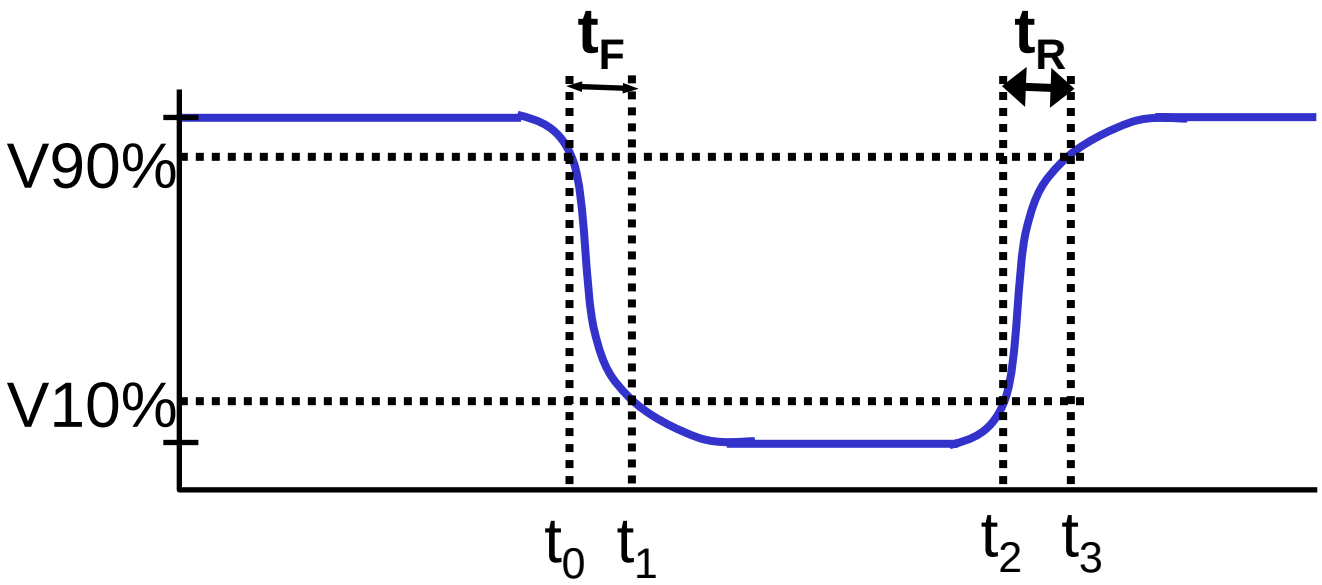
  - If gain (dV_{out}/dV_{in}) > 1, noise will be amplified.
  - If gain < 1, noise is filtered. Therefore V_{IL}, V_{IH} define regions where gain < 1

Inverter Time Response



- **Propagation delay measured from 50% point of Vin to 50% point of Vout**
- **$t_{phl} = t_1 - t_0$, $t_{plh} = t_3 - t_2$, $t_p = \frac{1}{2}(t_{phl}+t_{plh})$**

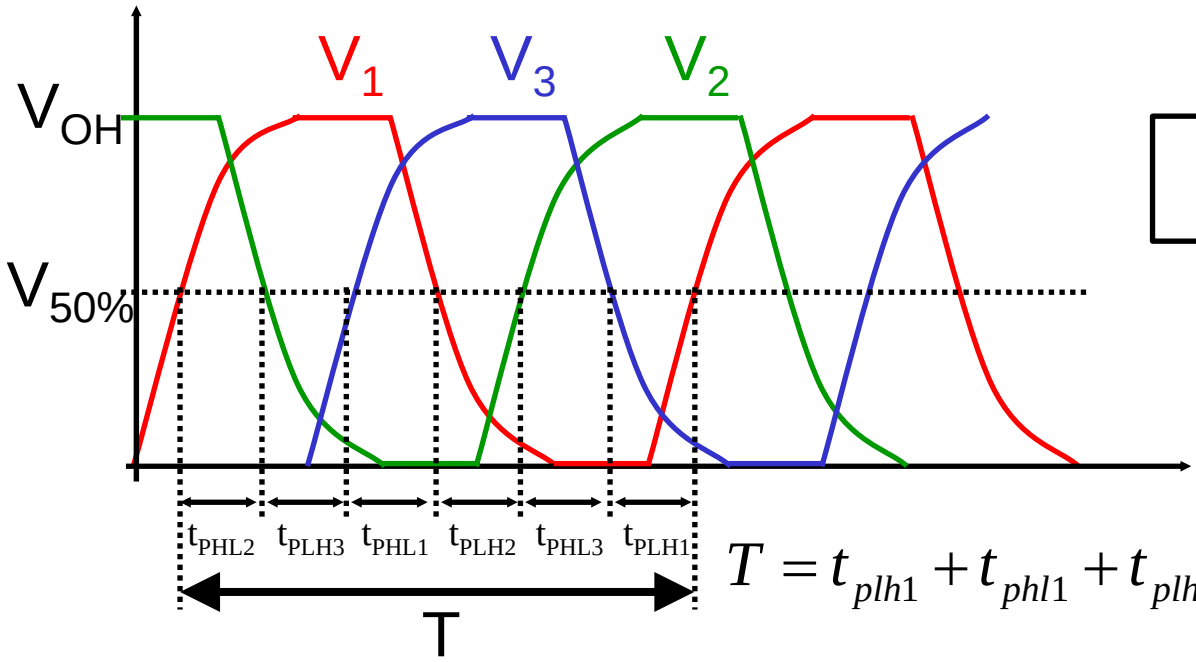
Rise and Fall Time

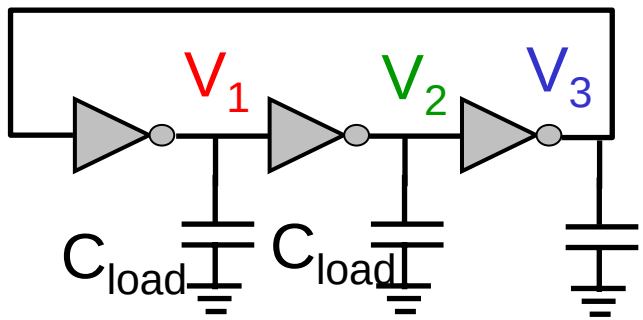


- **Fall time: measured from 90% point to 10% point**
  - $t_F = t_1 - t_0$
- **Rise time: measured from 10% point to 90% point**
  - $t_R = t_3 - t_2$
- **Alternately, can define 20%-80% rise/fall time**

Ring Oscillator

- ***Ring oscillator circuit*: standard method of comparing delay from one process to another**
- **Odd-number n of inverters connected in chain: oscillates with period T (usually n >> 5)**

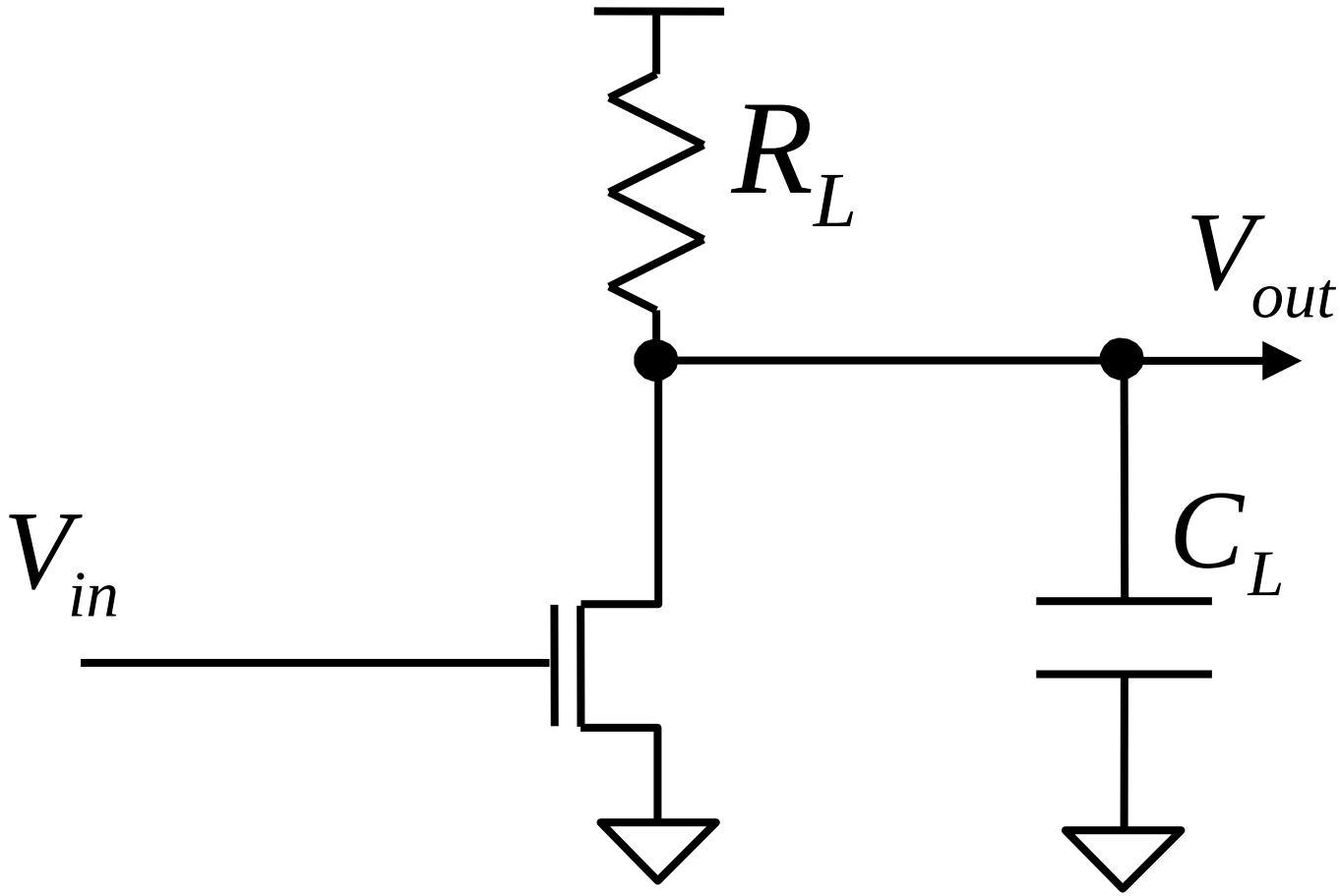




$$T = t_{plh1} + t_{phl1} + t_{plh2} + t_{phl2} + t_{plh3} + t_{phl3} + \cdots$$

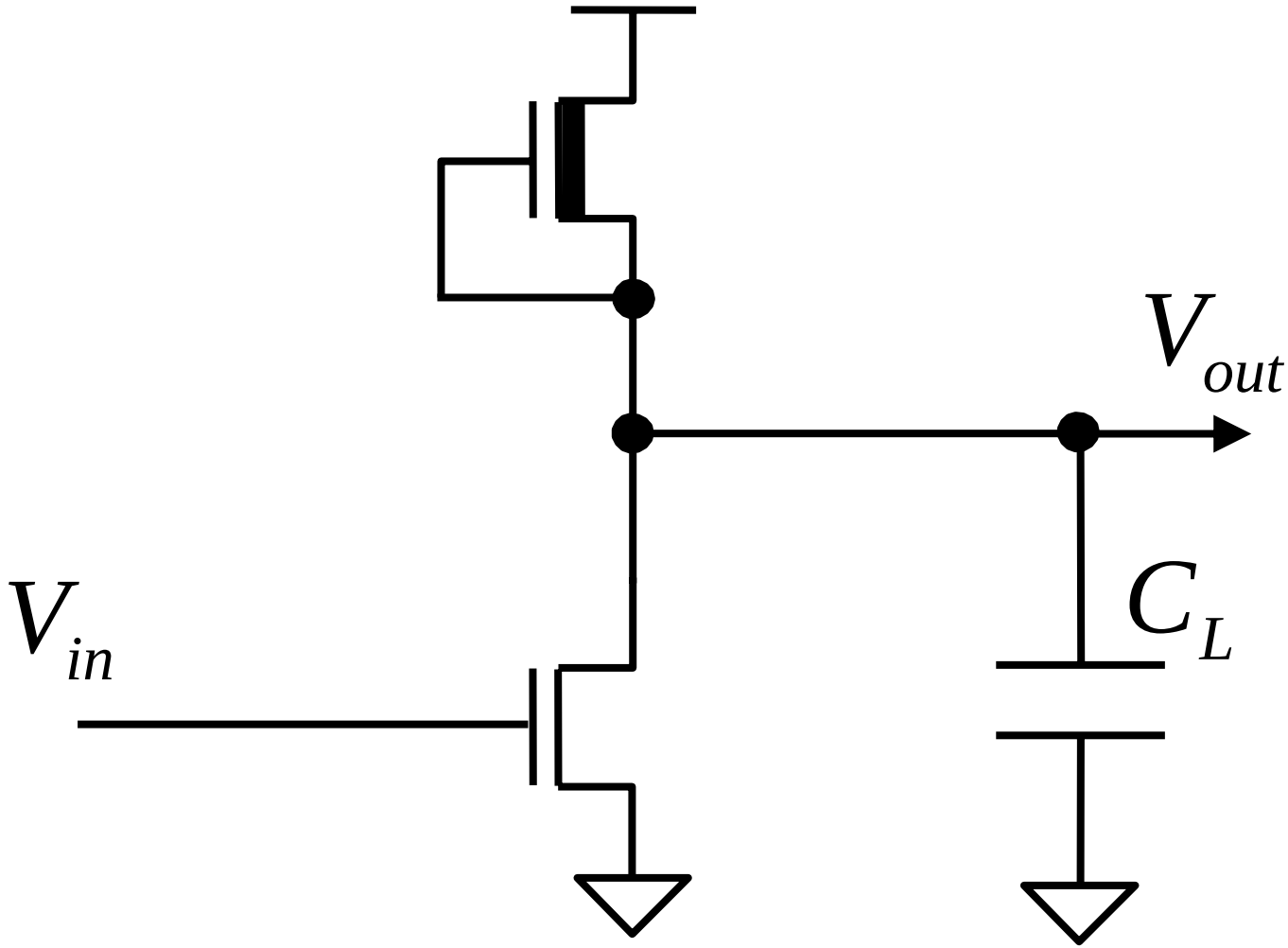
$$T = 2nt_p, \qquad f = \frac{1}{T} = \frac{1}{2nt_p}, \qquad t_p = \frac{1}{2nf}$$

Resistive Load Inverter



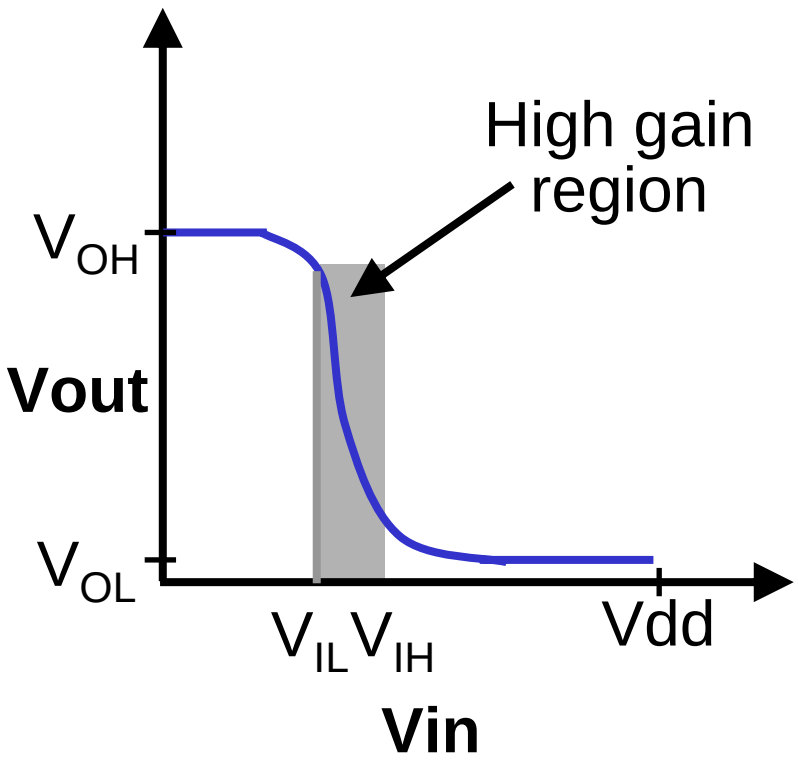
- **Resistor pulls up to Vdd (V_{OH}), NMOS pulls down (V_{OL})**

NMOS Inverter



- **Depletion NMOS always on, sourcing static current**

Inverter as Amplifier



- **For V_{in} between V_{IL} and V_{IH}, inverter gain > 1**
- **Acts as a linear amplifier (often very high gain)**
- **Logic levels ‘0’ and ‘1’ correspond to saturating amplifier output (output is pegged to high or low supply)**
- **Resistive load inverter same circuit as common source amplifier**

Next Topic: CMOS Inverters

- **CMOS Inverters**
  - DC Characteristics: Sizing
  - AC Characteristics: Designing for speed