EEC 118 Lecture #17: Future Directions
Alternatives to CMOS
Final Review

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Announcements

• Lab 6 final report due Thursday, June 2, 5 PM in homework box

• Final Exam: Monday, June 6, 8-10 AM

• Regular Office Hours: Wednesday 2-3 PM

• TA Office Hours Final Review: TBD
Digital Circuits Beyond CMOS

• Past digital technologies
  – Electromagnetic Relay: mechanical switch controlled by a current; ideal switch but high power and slow
  – Vacuum Tube: three (usually) terminal device, similar to a MOSFET but very high power
  – Bipolar Transistor: high transconductance, but high power, finite input impedance limits fanout

• State-of-the-art digital technology is bulk silicon CMOS
  – Low power, little static power (compared to other technologies)
  – Infinite input impedance allows large fanouts
  – Vast development investment has led to extremely high reliability, high yields, and high performance
Digital Circuits Beyond CMOS

• Modifications on CMOS can extend Moore’s Law
  – Strained silicon: mechanical stress on bulk crystal improves mobility
  – Silicon-on-Insulator: insulating bulk decreases parasitic capacitors, allows tighter integration
  – New materials: low-k interconnect dielectrics, high-k gate dielectrics, metal gates
  – New structures: 3D gates (finFET)

• But what happens when scaling stops?
  – International Technology Roadmap for Semiconductors extends to about 20 nm gate lengths in 2015-2020 time frame
  – Research devices demonstrated down to 5 nm gate lengths
Nanometer Gate Length Bulk FETs

• Still more room at the bottom!

• In 10 nm CMOS, Intel 386 occupies 25 μm x 25 μm

• Fabricated using a combination of lithography and epitaxial growth to define feature sizes

Doyle, Intel 2002

Amirtharajah, EEC 118 Spring 2011
Three Dimensional Transistors: FinFETs

- Channel forms in thin silicon fin
- Gate wraps around fin to control channel formation
- Allows very small channel lengths

Hisamoto, JSSC 2000
Digital Circuits Beyond CMOS

- New devices based on new materials or quantum effects
  - Gallium Arsenide (GaAs) MESFET: high electron mobility but no complementary device and poor oxide isolation
  - Josephson Junctions: superconducting logic and interconnect promises very high speed (THz), but only two terminals inconvenient for circuit design
  - Carbon Nanotube Transistors: carbon nanotube devices demonstrate high carrier mobilities and promise high speed
  - Molecular Electronics: single organic molecules shown to switch states in the lab, but also only two terminals
  - Organic Electronics: semiconducting plastic substrate, enables flexible displays and low cost but offers poor performance
Alternatives to Electronics

• A number of completely different digital technologies
  – Optical Computing: use photons to carry information instead of charge carriers, but no good three terminal nonlinear optical element and difficult integration
  – Quantum Computing: using various atomic-scale structures to store multiple bits simultaneously and operating on them using laws of quantum mechanics allows massive parallelism, but very sensitive to noise
  – Biological Computing: use DNA gene coding and promoter and repressor sites to control synthesis of proteins, which form the digital “signals”

• But can anything replace CMOS?
  – Maybe, but not for a long time
  – Some parts of a system (memory) before others (logic)
Final Exam Review List

Closed Book, Closed Notes, 1 8.5 in. x 11 in. Formula Sheet allowed, both sides, (You may bring a calculator)

• MOS Fabrication (very basics)
• MOS Structure
• Inverter Operation
• CMOS Inverter (Static Characteristics, e.g. VTC)
• CMOS Inverter (Dynamic Characteristics, e.g tpd, etc.)
• Complex Gates, Pseudo NMOS
  – DC and Transient characteristics
• Sequential Logic
• Logical Effort
Final Exam Review List

• Pass Transistor Logic, Pseudo NMOS
• Dynamic Logic
• Memory (DRAM, SRAM, Flash, ROM)
• Low Power Circuits
• Arithmetic Circuits
• Interconnect
• Study all homework and lecture materials
• Study labs
Key Learnings

• Should know what region of operation the transistor is in given the bias voltages at its terminals

• Should know what the PMOS and NMOS Id vs Vds curves look like

• Be able to identify major points of the VTC for a CMOS Device [Voh, Vol, Vih, Vil, Vth]

• Need to know how to calculate the total capacitance at the output node (including Miller effect)

• Know the relevant capacitances of a transistor used in transient analysis (i.e. Cgs, Cgd, …).
Key Learnings

• Know how to calculate propagation delay using Req and capacitance load. Be able to derive Req and Cload.
• Know Pseudo NMOS and Pass Transistor Logic pros and cons
• Know Different Adders and Multipliers
  – Know concepts of how they speed up these arithmetic units
• Dynamic Logic concepts
  – Pros and cons, techniques used to cascade, avoid noise, etc.
• Memory (different types, SRAM operation)
• Low Power Design techniques (voltage scaling, pipelining, etc.)
• Interconnect basics (resistance, capacitance)
Key Learnings

• Know how to find the Boolean function from a schematic

• Know how to properly size transistors to get the equivalent resistance of a basic inverter

• Know how to size devices and choose logic depth based on logical effort

These are here to help focus your study but is not an exhaustive list of what you are responsible for