EEC 118 Lecture #15: Interconnect

Rajeevan Amirtharajah
University of California, Davis

Outline

- Review and Finish: Low Power Design
- Interconnect Effects: Rabaey Ch. 4 and Ch. 9 (Kang & Leblebici, 6.5-6.6)

Interconnect Modeling

- **Early days of CMOS, wires could be treated as ideal for most digital applications, not so anymore!**
- **On-chip wires have resistance, capacitance, and inductance**
  - Similar to MOSFET charging, energy depends solely on capacitance
  - Resistance might impact low power adiabatic charging, static current dissipation, speed
  - Ignore inductance for all but highest speed designs
- **Interconnect modeling is whole field of research itself!**

Interconnect Models: Regions of Applicability

- **For highest speed applications, wire must be treated as a transmission line**
  - Includes distributed series resistance, inductance, capacitance, and shunt conductance (*RLGC*)
- **Many applications it is sufficient to use lumped capacitance (*C*) or distributed series resistance-capacitance model (*RC*)**
- **Valid model depends on ratio of rise/fall times to time-of-flight along wire**
  - l: wire length
  - v: propagation velocity (speed of light)
  - l/v: time-of-flight on wire

Interconnect Models: Regions of Applicability

- **Transmission line modeling (inductance significant):**

$$t_{rise}\ (t_{fall}) < 2.5 \times (l / v)$$

- **Either transmission line or lumped modeling:**

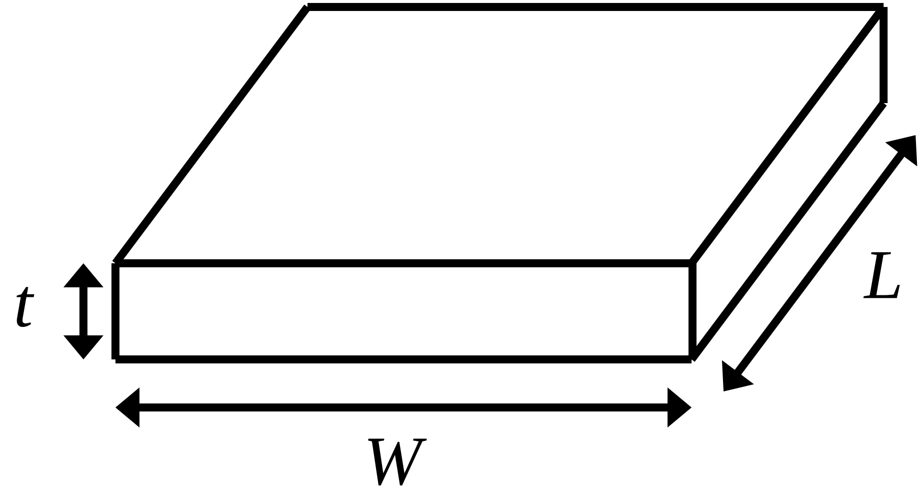
$$2.5 \times (l / v) < t_{rise}\ (t_{fall}) < 5 \times (l / v)$$

- **Lumped modeling:**

$$t_{rise}\ (t_{fall}) > 5 \times (l / v)$$

Resistance

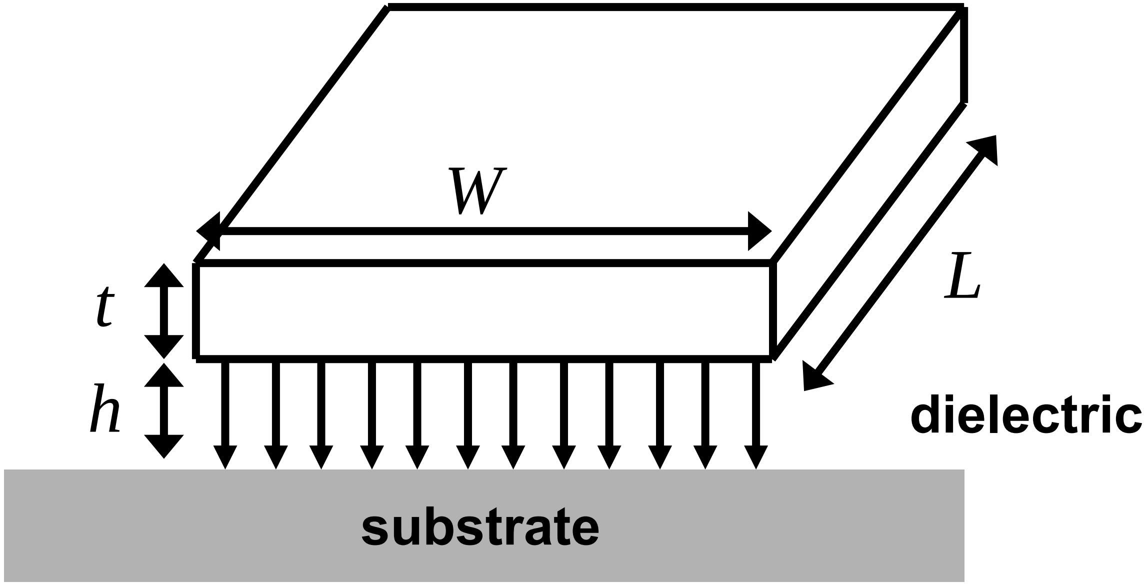
- **Resistance proportional to length and inversely proportional to cross section**
- **Depends on material constant resistivity ρ (Ω-m)**



$$R = \frac{\rho L}{A} = \frac{\rho L}{tW} = R_{sq} \frac{L}{W} \qquad R_{sq} = \frac{\rho}{t}$$

Parallel-Plate Capacitance

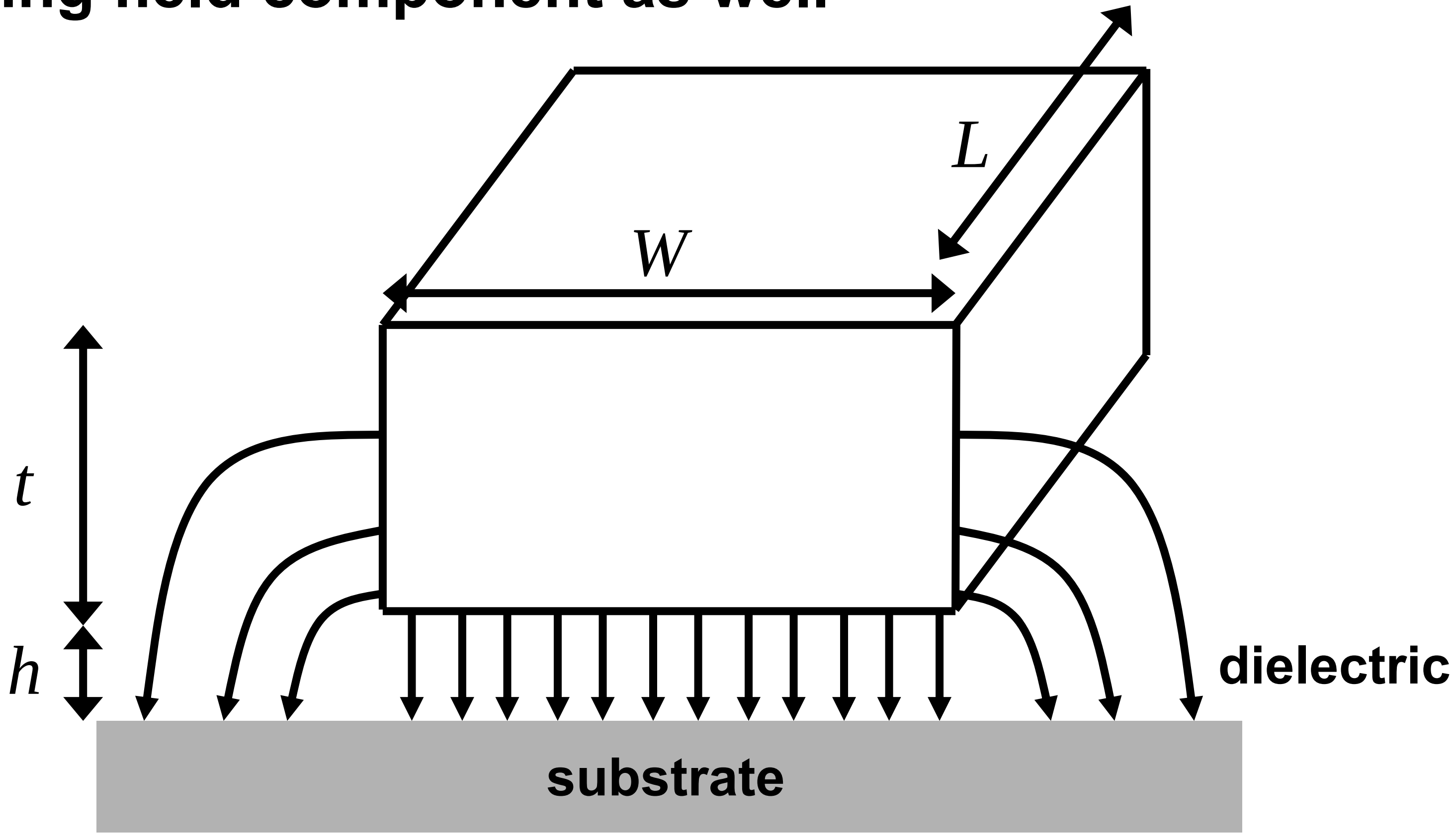
- **Width large compared to dielectric thickness, height small compared to width: E field lines orthogonal to substrate**



$$C = \frac{\varepsilon_r}{h} WL$$

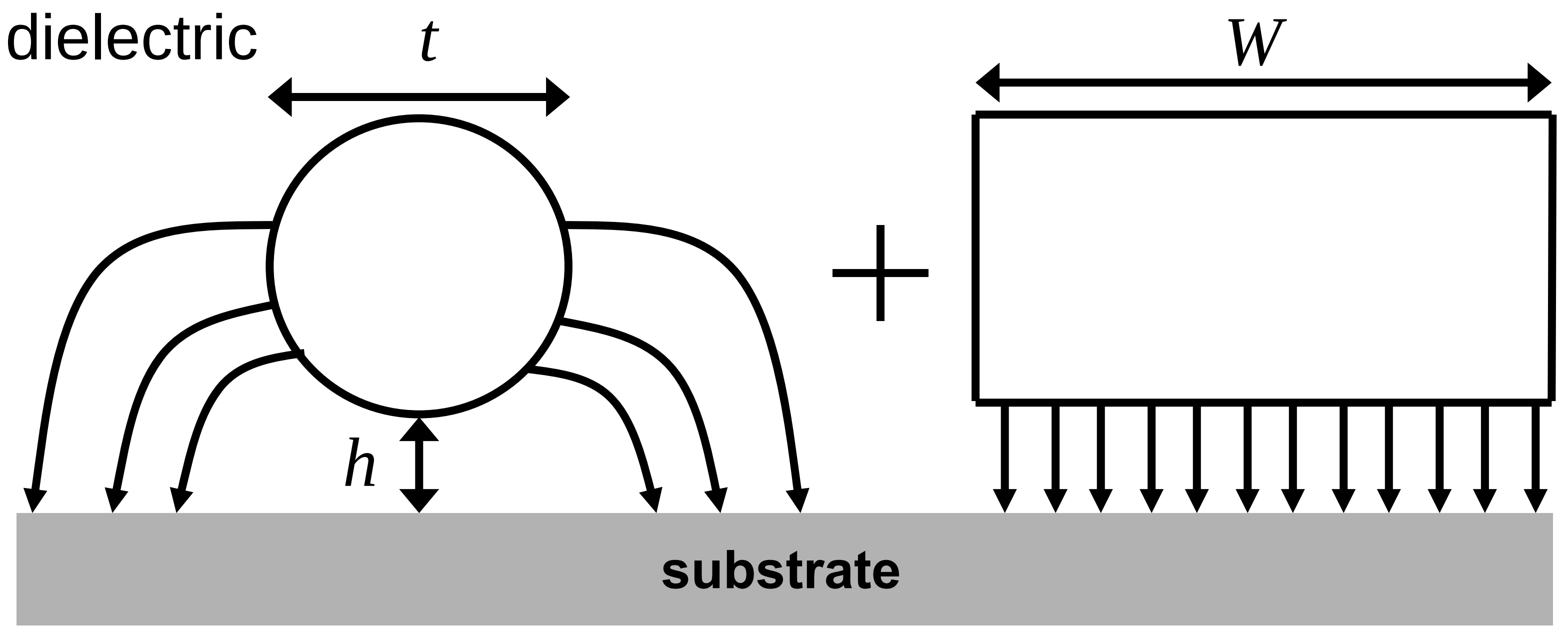
Fringing Field Capacitance

- **When height comparable to width, must account for fringing field component as well**



Total Capacitance Model

- When height comparable to width, must account for fringing field component as well
- Model as a cylindrical conductor above substrate



Total Capacitance Model

- **Total capacitance per unit length is parallel-plate (area) term plus fringing-field term:**

$$c = c_{pp} + c_{fringe} = \frac{\varepsilon_r}{h}\left(W - \frac{t}{2}\right) + \frac{2\pi\varepsilon_r}{\log\left(2h/t + 1\right)}$$

- **Model is simple and works fairly well (Rabaey, 2nd ed.)**
  - More sophisticated numerical models also available
- **Process models often give both area and fringing (also known as sidewall) capacitance numbers per unit length of wire for each interconnect layer**

Alternative Total Capacitance Models

- **For wide lines (w ≥ t/2) Kang & Leblebici Eq. 6.53:**

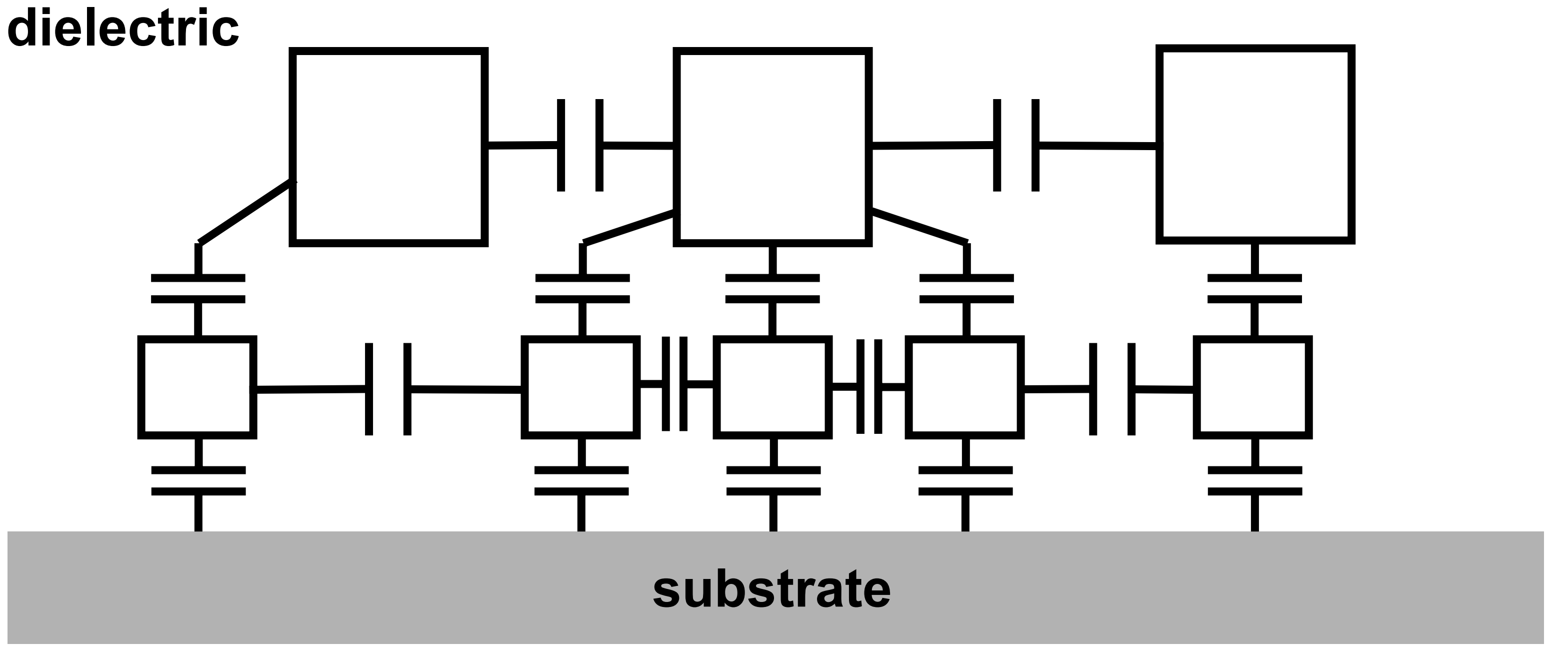
$$C = \frac{\varepsilon_r}{h}\left(W - \frac{t}{2}\right) + \frac{2\pi\varepsilon_r}{\ln\left(1 + \frac{2h}{t} + \sqrt{\frac{2h}{t}\left(\frac{2h}{t} + 2\right)}\right)}$$

- **For narrow lines (w ≤ t/2) Kang & Leblebici Eq. 6.54:**

$$C = \frac{\varepsilon_r W}{h} + \frac{\pi\varepsilon_r\left(1 - 0.0543\frac{t}{2h}\right)}{\ln\left(1 + \frac{2h}{t} + \sqrt{\frac{2h}{t}\left(\frac{2h}{t} + 2\right)}\right)} + 1.47\varepsilon_r$$

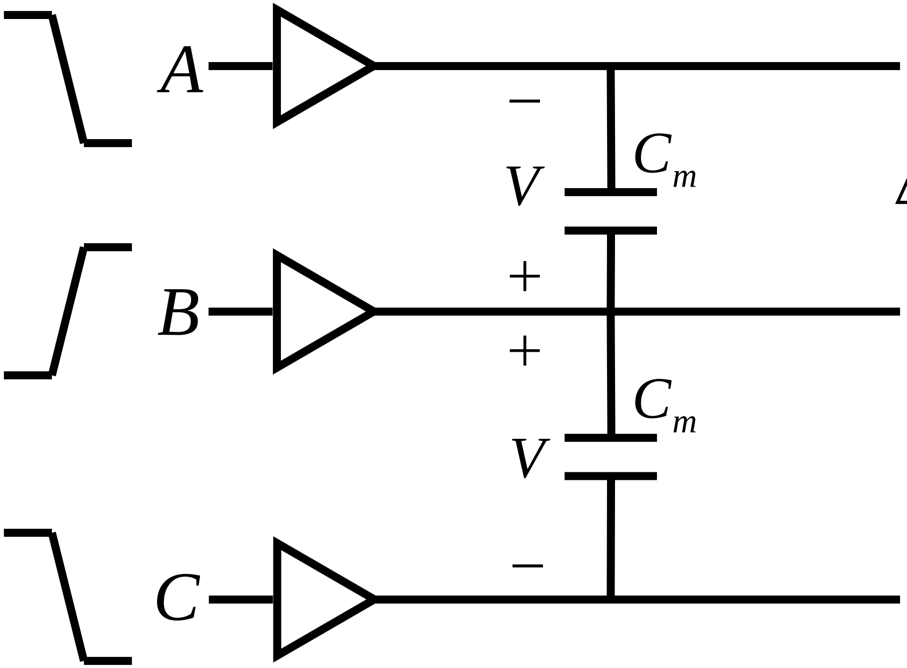
Capacitive Coupling

- **Fringing fields can terminate on adjacent conductors as well as substrate**
- **Mutual capacitance between wires implies crosstalk, affects data dependency of power**



Miller Capacitance

- **Amount of charge moved onto mutual capacitance depends on switching of surrounding wires**
- **When adjacent wires move in opposite direction, capacitance is effectively doubled (Miller effect)**



$$
\begin{aligned}
\Delta Q &= C_m\left(V_f - V_i\right) \\
&= C_m\left(V_{DD} - \left(-V_{DD}\right)\right) \\
&= 2C_m V_{DD}
\end{aligned}
$$

Data Dependent Switched Capacitance 1

- **When adjacent wires move in same direction, mutual capacitance is effectively eliminated**

$$A\uparrow\ B\uparrow\ C\uparrow \quad \text{OR} \quad A\downarrow\ B\downarrow\ C\downarrow \qquad C_{eff} = 0$$

$$A\downarrow\ B\uparrow\ C\downarrow \quad \text{OR} \quad A\uparrow\ B\downarrow\ C\uparrow \qquad C_{eff} = 4C_m$$

$$A\downarrow\ B\uparrow\ C\uparrow \quad \text{OR} \quad A\downarrow\ B\downarrow\ C\uparrow$$

$$A\uparrow\ B\uparrow\ C\downarrow \quad \text{OR} \quad A\uparrow\ B\downarrow\ C\downarrow \qquad C_{eff} = 2C_m$$

Data Dependent Switched Capacitance 2

- **When adjacent wires are static, mutual capacitance is effectively to ground**

$0B\uparrow 0$ OR $1B\downarrow 1$

$1B\uparrow 0$ OR $0B\downarrow 1$

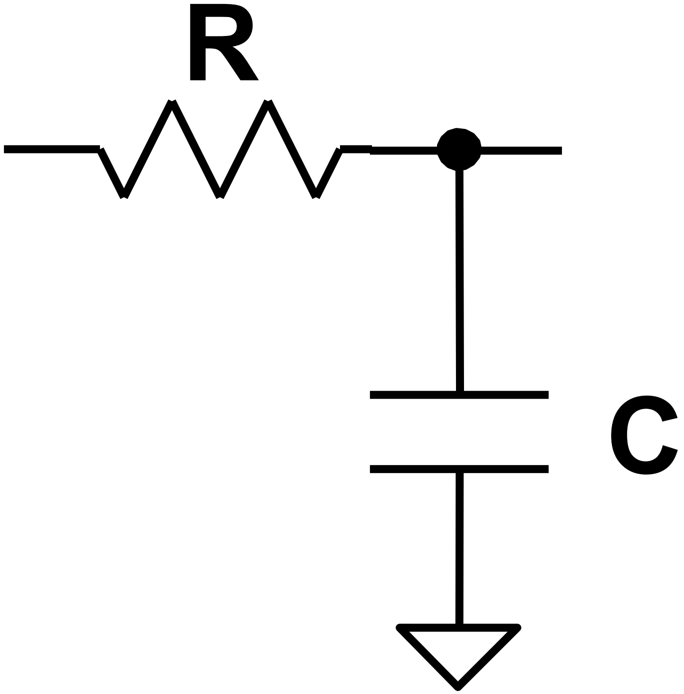
$0B\uparrow 1$ OR $1B\downarrow 0$

$1B\uparrow 1$ OR $0B\downarrow 0$

$$C_{eff} = 2C_m$$

- **Remember: it is the *charging* of capacitance where we account for energy from supply, <u>not</u> discharging**

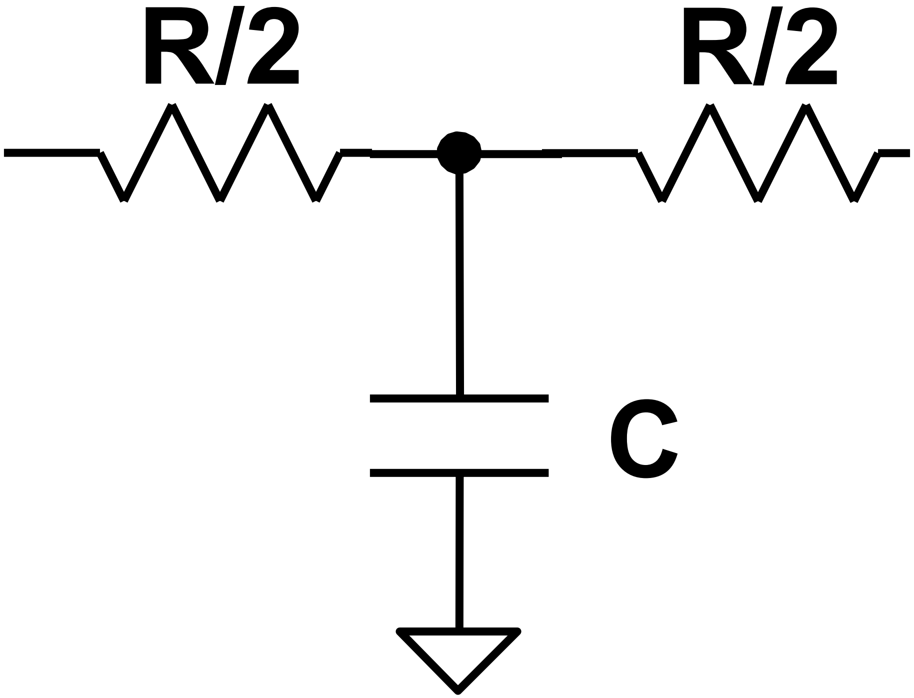
Lumped RC Model



- **Simplest model used to represent the resistive and capacitive interconnect parasitics**
- **Propagation delay (same as FET switch model):**

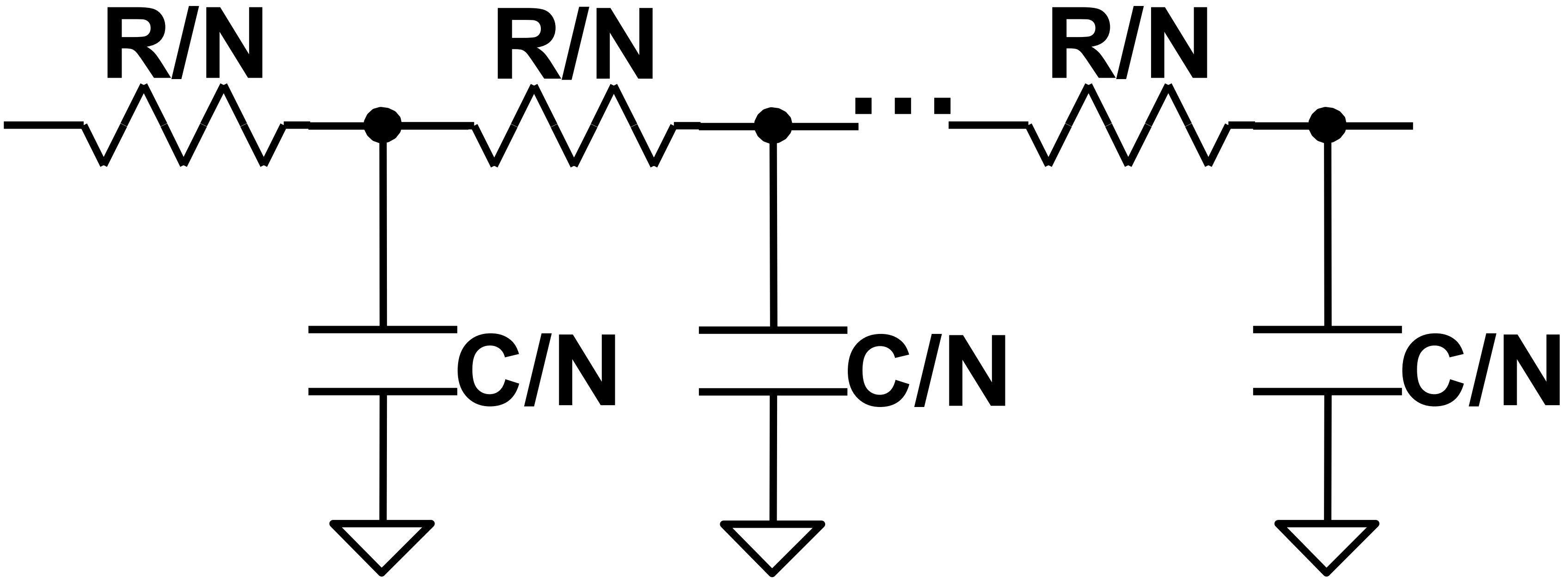
$$t_{PLH} \approx 0.69RC$$

RC T-Model



- **Significantly improves accuracy of transient behavior over the lumped RC model**
- **Useful if simulation time is a bottleneck, much simpler than fully distributed model**

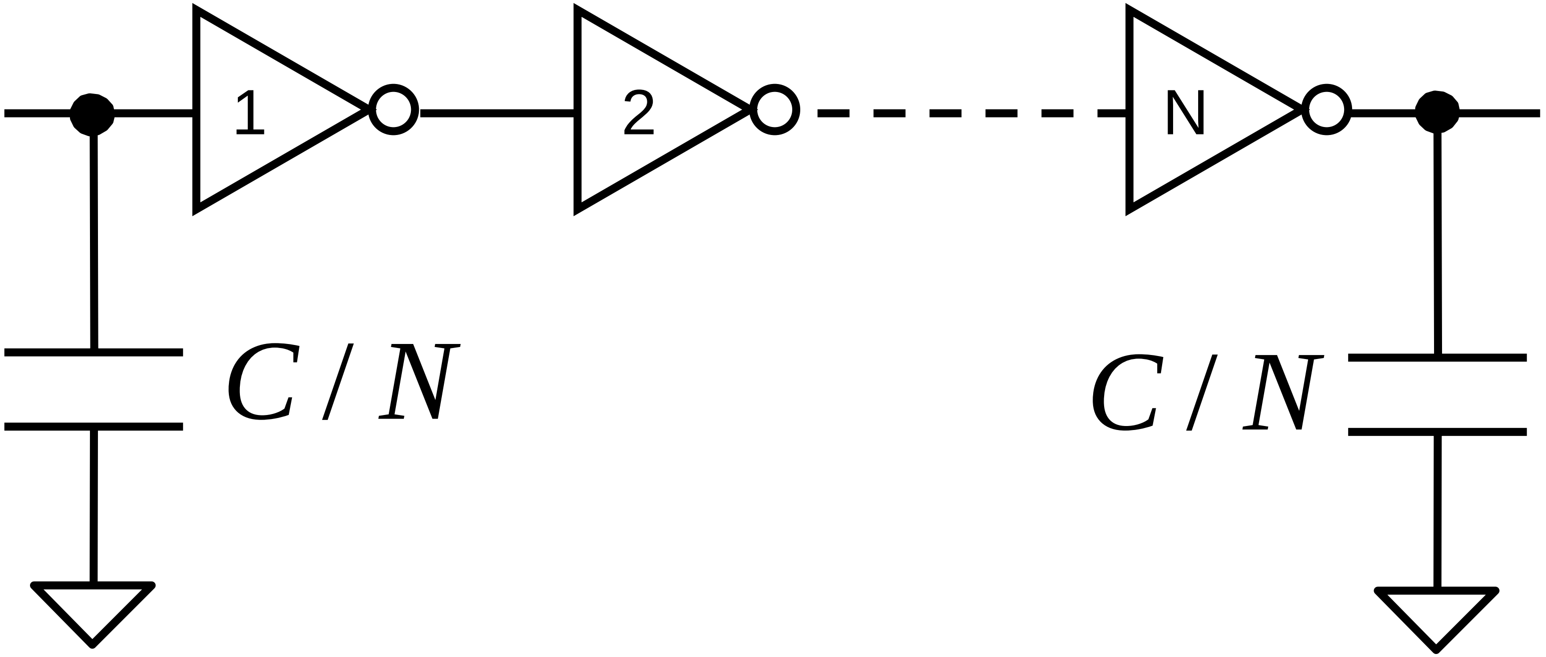
Distributed RC Model



- **Elmore delay approximation for *RC* ladder network:**

$$t_{DN} = \frac{RC}{2} \quad \text{as} \quad N \rightarrow \infty$$

Repeater Insertion to Reduce Wire Delay



- Insert inverters along long wires at regular intervals
- Breaks up resistance and capacitance, reducing delay dramatically

Inductance

- **Inductance can be determined by direct application of definition:**

$$\Delta V = L \frac{di}{dt}$$

- **Can compute inductance directly from wire geometry and surrounding environment using field solver**

- **Simpler approach relates capacitance per length *c* with inductance per length *l:***

$$cl = \varepsilon\mu$$

  - Assumes uniform or “average” dielectric

Summary

- **Many important effects to consider in interconnect design**
  - Resistance, capacitance, inductance can all affect signal performance
  - Long rise/fall time signals, only resistance and capacitance needs to be considered
- **Several models useful for RC interconnect delay analysis**
  - Simple lumped (1 R, 1 C) model: easy to analyze and/or simulate, will be pessimistic
  - T-model (2 R_{eq} = R/2, 1 C): more accurate than lumped
  - Distributed model (N R_{eq} = R/N, N C_{eq} = C/N): most accurate, use Elmore delay approximation for hand analysis

Next Topic: Design for Manufacturability

- **Parameter variations in CMOS digital circuits**
- **Yield maximization and worst-case design**