EEC 118 Spring 2011 Lab #6
SRAM Cell Design

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Due: June 2, 2011, 5 PM in 3173 Kemper.

1 OBJECTIVE

The objective of this lab is to use Cadence to build and simulate two SRAM circuits and explore their robustness by modifying transistor sizes.

2 PRELAB

There is no prelab for this lab.

3 6T SRAM CELL SIZING

In this section you will attempt to evaluate the robustness of a six transistor (6T) SRAM cell by adjusting the W/L ratios of various devices until the cell fails. Create a new cell in your library called `sram6T` and generate a schematic similar to the one shown in Figure 1 and a corresponding symbol view. You can choose initial sizes for the transistors as shown in Figure 1. Create a testbench cell called `lab6_sram_tb`, a schematic view for the cell, and instantiate a voltage source for the power supply, copies of the 6T SRAM cell as your DUTs, and any other voltage sources you may need to evaluate the read and write transistor size margins.

Part 3.1 Sizing for Read Margin Set up and run a Cadence Spectre (i.e., analog) simulation for reading a logic 0 from the 6T SRAM cell stored at node Q. You may need to set initial conditions at Q and Qb of 0V and 1.8V, respectively. Choose connections for the access transistors and bitlines such that a worst case voltage disturbance on node Q occurs. For the initial set of transistor sizes, you should find that Q gets pulled up to about 400mV from 0V under these conditions. Plot the voltage waveforms at Q and Qb and show them to the TA or instructor for checkoff.

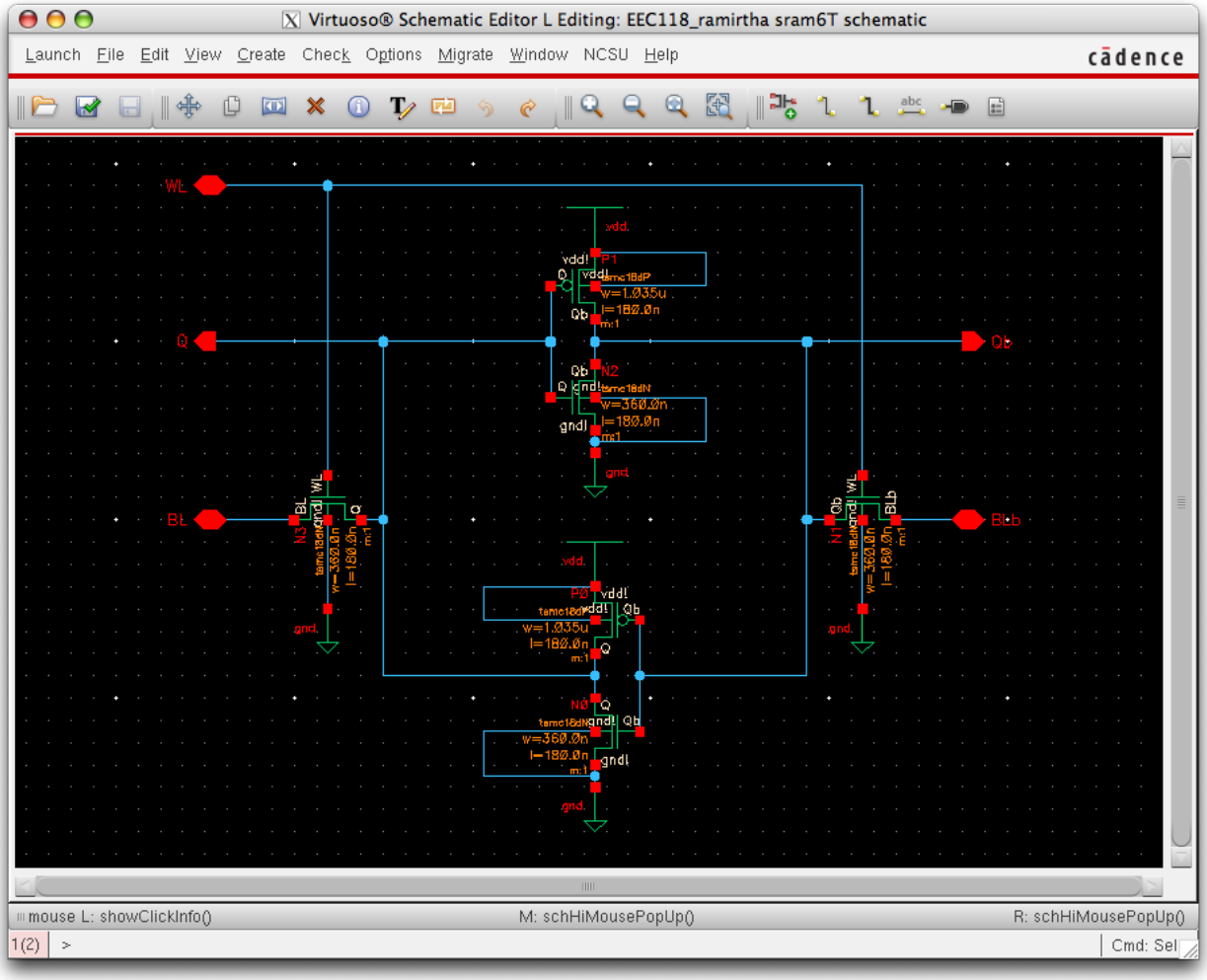

Figure 1: 6T SRAM cell schematic.

Next modify the sizes of NMOS devices N3 and N0 until node Q rises to $V_{DD}/2$, which is at the edge of a read 0 failure. Note that you must make identical changes to N2 and N1 to maintain the symmetry of the cell. Plot the corresponding waveforms and show them to the TA or instructor for checkoff. Enter the read 0 failure sizes in the summary table.

Part 3.2 Sizing for Write Margin Set up and run a Cadence Spectre (i.e., analog) simulation for writing a logic 0 into the 6T SRAM cell stored at node Q. You may need to set initial conditions at Q and Qb of 1.8V and 0V, respectively. Choose connections for the access transistors and bitlines such that the voltage on node Q changes from a logic 1 to a logic 0. For the initial set of transistor sizes, you should find that Q is written easily and quickly (in less than 2ns). Plot the voltage waveforms at Q and Qb and show them to the TA or instructor for checkoff.

Next modify the sizes of NMOS device N3 and PMOS device P0 until node Q just barely fails to change its state. Note that you must make identical changes to N1 and P1 to maintain the symmetry of the cell. Plot the corresponding waveforms and show them to the TA or instructor for checkoff. Enter the write 0 failure sizes in the summary table.

4 8T SRAM CELL SIZING

To decouple the sizing tradeoffs between reading and writing the 6T SRAM cell, one can add a few extra transistors to create a separate read port. The extra degree of freedom this provides allows the designer to choose W/L ratios for the transistors involved in the write configuration independently of the transistors involved in the read configuration. In this section you will attempt to evaluate the robustness of an eight transistor (8T) SRAM cell by adjusting the W/L ratios of various devices until the cell fails.

Create a new cell in your library called `sram8T` and generate a schematic similar to the one shown in Figure 2 and a corresponding symbol view. You can choose initial sizes for the transistors as shown in Figure 2. To your testbench cell `lab6_sram_tb`, add copies of the 8T SRAM cell as additional DUTs, and any other voltage sources you may need to evaluate the read and write transistor size margins.

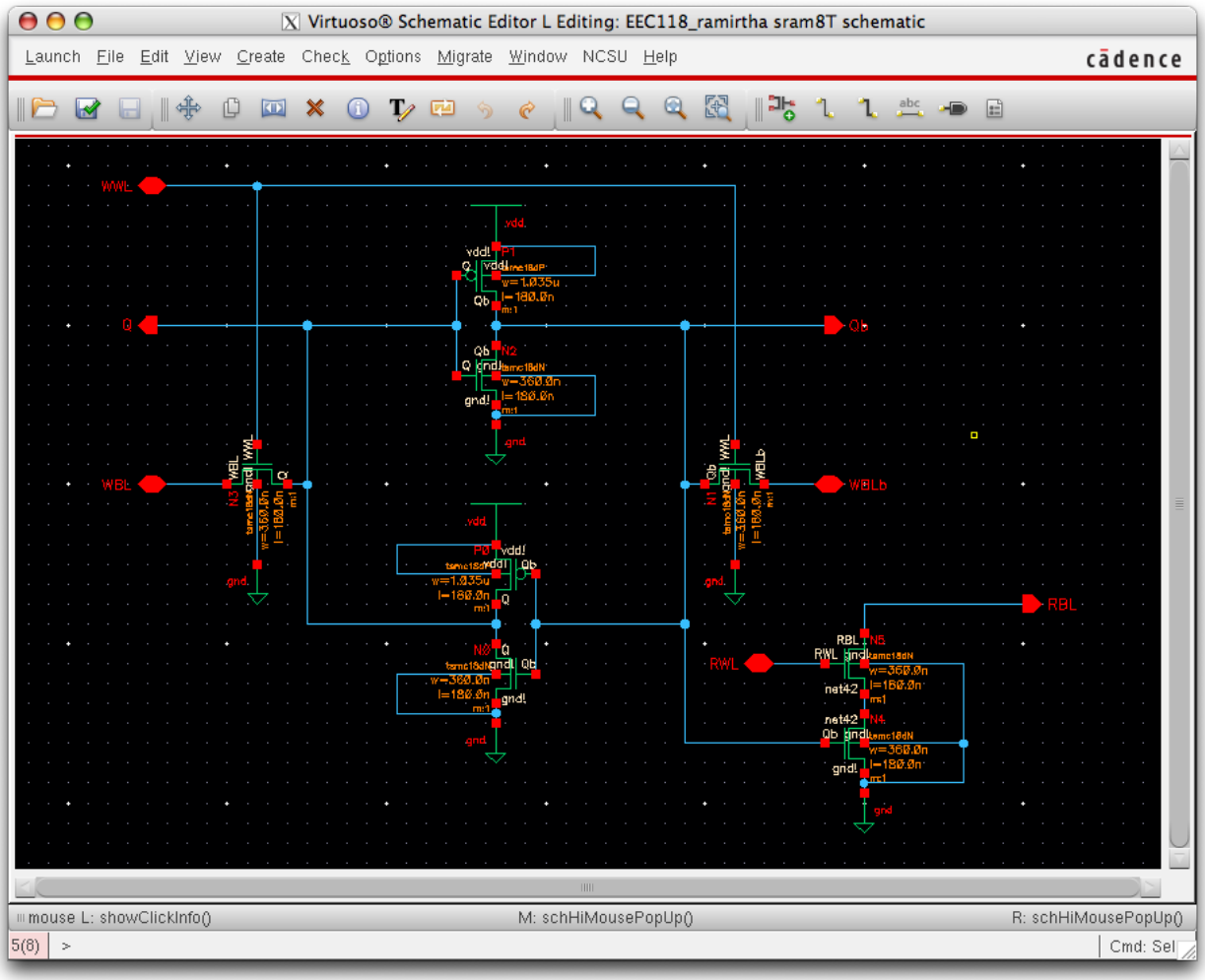

Figure 2: 8T SRAM cell schematic.

Part 4.1 Sizing for Read Margin Set up and run a Cadence Spectre (i.e., analog) simulation for reading a logic 0 from the 8T SRAM cell stored at node Q. You may need to set initial conditions at Q and Qb of 0V and 1.8V, respectively. Choose connections for the

access transistors and bitlines such that a worst case voltage disturbance on node Q or Qb occurs. For the initial set of transistor sizes, you should find that Q and Qb do not change significantly under these conditions. Plot the voltage waveform at Q and Qb and show them to the TA or instructor for checkoff.

Is it possible to modify the sizes (within a reasonable range) of any transistors in the 8T cell such that node Q or Qb approaches $V_{DD}/2$, which is at the edge of a read 0 failure? Be prepared to justify your answer in your lab report.

Part 4.2 Sizing for Write Margin Set up and run a Cadence Spectre (i.e., analog) simulation for writing a logic 0 into the 8T SRAM cell stored at node Q. You may need to set initial conditions at Q and Qb of 1.8V and 0V, respectively. Choose connections for the access transistors and bitlines such that the voltage on node Q changes from a logic 1 to a logic 0. For the initial set of transistor sizes, you should find that Q is written easily and quickly (in less than 2ns). Plot the voltage waveforms at Q and Qb and show them to the TA or instructor for checkoff.

Next modify the sizes of NMOS device N3 and PMOS device P0 until node Q just barely fails to change its state. Note that you must make identical changes to N1 and P1 to maintain the symmetry of the cell. Plot the corresponding waveforms and show them to the TA or instructor for checkoff. Enter the write 0 failure sizes in the summary table. Be sure to note any differences in the sizes relative to the 6T SRAM cell in your report.

Checkoff

Show your completed schematics and all waveform plots to the TA for checkoff.

Report

Write up your simulation results in a lab report. Your report can be brief, but must include the following sections in addition to the completed summary sheet attached at the end of this lab. The summary sheet will be the cover page of your lab. Be sure to include schematics of your circuits and any waveform plots.

1. Overview: Describe in one paragraph the objectives of the lab. State what you were designing and testing and what data you expected to gather as a result of your experiments. Also, describe how you expected the two SRAM cells to perform under the different sizing and test conditions.

2. Test Conditions and Sizing Strategy: Describe the voltage bias conditions at the wordlines and bitlines and the initial conditions of the storage nodes which you used to test the read and write operations above. **Be sure to include circuit schematics which show these biases and initial conditions in your report.** Explain how you chose transistor sizes to force the read and write cell failures you observed. Be sure to discuss in detail your answer to sizing for a read failure for the 8T SRAM cell as outlined in Section 4.1.

3. Results and Discussion: Review the sizing results listed in the summary table. Do the results make intuitive sense? If not, explain why they might contradict your intuition. Which SRAM cell has better read stability and why? Which SRAM cell has better write stability and why?

EEC 118 Spring 2011 Lab #6 Summary

Name:

Grading:

Part	Checkoff	TA Initials	Date
6T SRAM Schematic 8T SRAM Schematic Testbench Schematic 3.1 6T SRAM Read 0 Initial Waveform Plot 3.1 6T SRAM Read 0 Failure Waveform Plot 3.2 6T SRAM Write 0 Initial Waveform Plot 3.2 6T SRAM Write 0 Failure Waveform Plot 4.1 8T SRAM Read 0 Initial Waveform Plot 4.2 8T SRAM Write 0 Initial Waveform Plot 4.2 8T SRAM Write 0 Failure Waveform Plot			
	Value		
3.1 6T SRAM Read 0 Failure N3 W/L 3.1 6T SRAM Read 0 Failure N0 W/L 3.2 6T SRAM Write 0 Failure N3 W/L 3.2 6T SRAM Write 0 Failure P0 W/L 4.2 8T SRAM Write 0 Failure N3 W/L 4.2 8T SRAM Write 0 Failure P0 W/L			