EEC 118 Spring 2011 Lab #2: CMOS Inverter and Gates

Dept. of Electrical and Computer Engineering
University of California, Davis

March 27, 2011

Reading: Rabaey Section 1.3.3, Chapter 5 [1].
Reference: Kang and Leblebici Chapter 5, Section 7.3 [2].

I OBJECTIVE

The objective of this experiment is to determine the Voltage Transfer Characteristic (VTC) of a CMOS inverter and to observe its characteristics in circuit connections.

II PRELAB

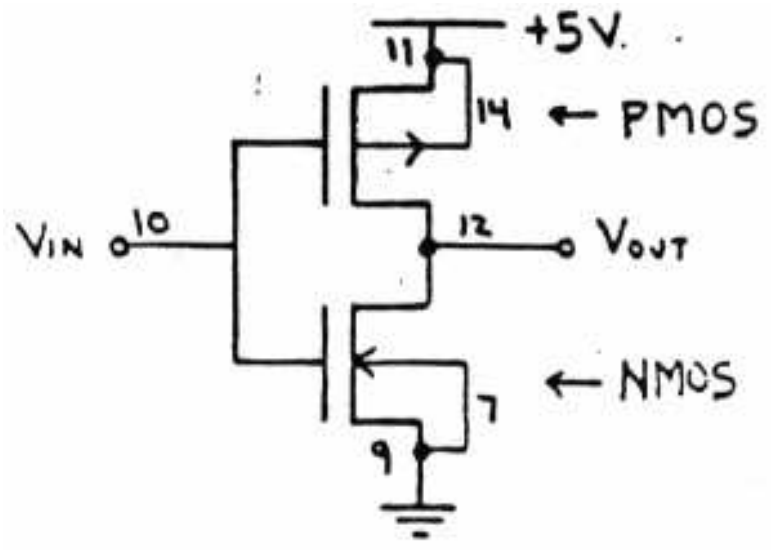

Figure 1: CMOS inverter wiring diagram.

Problem 1 (10 points) Use your transistor data from Lab #1 to calculate at least ten points on the VTC, including V_{OH}, V_{IH}, V_{OL}, and V_{IL}, for the CMOS inverter shown in Figure 1.
HINT: For simplicity in hand calculations, take output voltage as the independent parameter; calculate I_D and input voltage from it.

III VOLTAGE TRANSFER CHARACTERISTIC

Part 1 (20 points) Wire up the CMOS inverter shown in Figure 1 and observe its VTC. Measure the same ten points you computed in the Prelab. Compare with your calculated results from the Prelab.

Part 2 (20 points) Wire up a 2 input CMOS NOR gate using the transistors in the 4007 package. (a) Show the schematic in your lab report (be sure to label the pins). Verify the NOR gate truth table. (b) Connect the two inputs together. Measure the VTC of this inverter. How does the VTC for this inverter-connected NOR gate differ from the inverter in Figure 1? Explain any observed differences.

IV GATE CONNECTION-RING OSCILLATOR

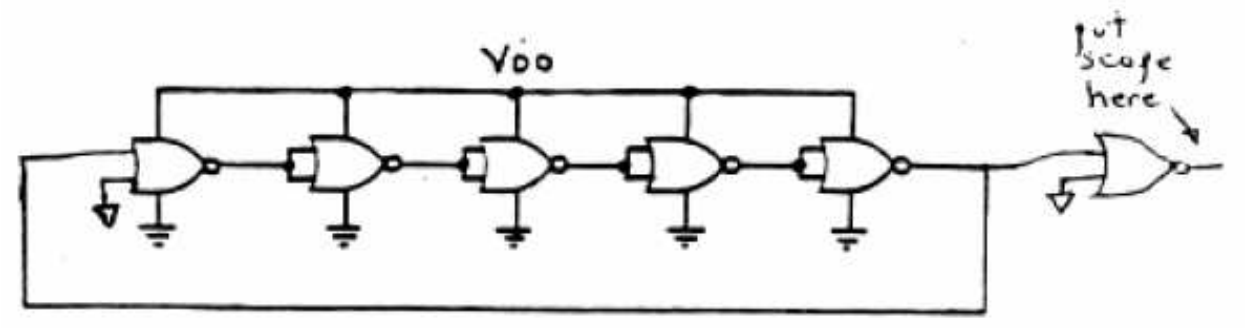

Figure 2: Connections for NOR gate ring oscillator.

Part 3 (10 points) The ring oscillator configuration shown in Figure 2 is often used to measure the average propagation delay time. Derive a formula which relates the average delay time to the period of the waveform observed at the output of any of the gates in the oscillator.

Part 4 (20 points) Wire up 5 CD4001 CMOS NOR gates to form a *ring oscillator* as shown in Figure 2. Use the oscilloscope to measure its oscillation frequency at supply voltages of 5, 7.5, 10, 12.5, and 15 V. Also measure the current I_{DD} drawn from the supply at each voltage. From your results, calculate the average propagation delay *per gate*, t_p, at each of these voltages. Explain the t_p vs. V_{DD} trend. Also compute the gate power-delay product at each voltage (gate power dissipation X t_p). Explain its variation with V_{DD}.

Part 5 (20 points) Load each of the five output nodes of your ring oscillator with the same capacitance value of 50 pF. Measure the oscillation frequency at $V_{DD} = 10$ V. Assume that propagation delay is a linear function of total capacitance at the output node of a gate (a good assumption), and calculate the approximate equivalent capacitance (due to internal nodes, package, and external wiring) present at the output of each gate with no capacitors added.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.