EEC 118 Spring 2011 Homework #2

Rajeevan Amirtharajah
Dept. of Electrical and Computer Engineering
University of California, Davis

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Reading: Rabaey, Chapters 3 and 5 [1].
Reference: Kang and Leblebici, Chapters 3 and 5 [2].

1 FET Capacitances

An NMOS transistor is fabricated with the following physical dimensions and dopant concentrations:

- $t_{ox} = 200\text{Å}$
- $W = 10\mu\text{m}$
- $L_d = 1.5\mu\text{m}$
- $x_d = 0.25\mu\text{m}$
- $L_S = 5\mu\text{m}$
- $x_j = 0.4\mu\text{m}$
- $N_D = 10^{20}\text{cm}^{-3}$
- Substrate Doping $N_A = 10^{16}\text{cm}^{-3}$
- Channel Stop Implant Doping $N_A^+ = 10^{19}\text{cm}^{-3}$

Problem 1.1 Determine the drain diffusion capacitance for $V_{DB} = 5\text{V}$ and 2.5V.

Problem 1.2 Calculate the overlap capacitance between gate and drain.

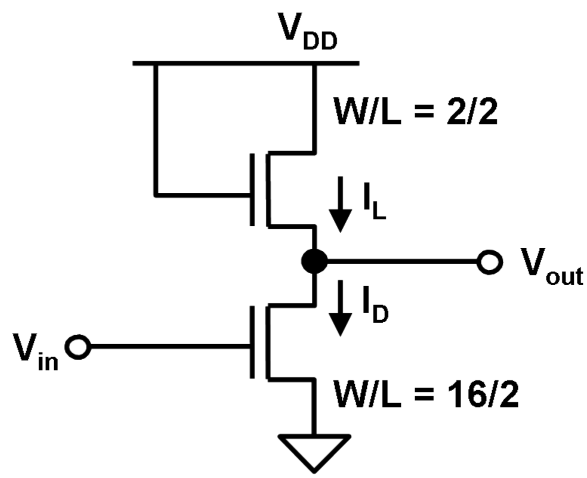

Figure 1: NMOS enhancement load inverter.

2 Enhancement Load Inverter

Consider the NMOS inverter circuit shown in Figure 1 which consists of two enhancement-mode NMOS transistors with the following parameters: $V_{T0} = 0.8\text{V}$, W/L ratios as shown in the figure, $\gamma = 0.38\text{V}^{1/2}$, $\lambda = 0.0\text{V}^{-1}$, $\mu C_{ox} = 45\mu\text{A/V}^2$, $-2\Phi_F = 0.6\text{V}$, and $V_{DD} = 5\text{V}$.

Problem 2.1 Calculate values for V_{OH} and V_{OL}. Note that the substrate-bias effect for either or both devices must be taken into consideration.

Problem 2.2 Interpret your results for Problem 2.1 in terms of noise margins and static (DC) power dissipation.

Problem 2.3 Calculate the steady-state current which is drawn from the DC power supply when the input is a logic "1", i.e. when $V_{in} = V_{OH}$.

3 CMOS Inverter

Consider a CMOS inverter with the following transistor parameters:

- NMOS: $V_{T0} = 0.6\text{V}$, $W/L = 8$, $\lambda = 0.0\text{V}^{-1}$, $\mu C_{ox} = 60\mu\text{A/V}^2$
- PMOS: $V_{T0} = -0.7\text{V}$, $W/L = 12$, $\lambda = 0.0\text{V}^{-1}$, $\mu C_{ox} = 25\mu\text{A/V}^2$

Assume $V_{DD} = 3.3\text{V}$.

Problem 3.1 Calculate the noise margins and the switching threshold (V_M) of this circuit.

Problem 3.2 For this problem and the next, assume the channel length of both transistors is $0.8\mu\text{m}$. Determine the W_P/W_N ratio so that the switching threshold of the inverter is $V_M = 1.4\text{V}$.

Problem 3.3 The CMOS fabrication process used to manufacture this inverter allows a variation in the NMOS threshold voltage $V_{T0,n}$ of $\pm 15\%$ around its nominal value of 0.6V, and a variation in the PMOS threshold voltage $V_{T0,p}$ of $\pm 20\%$ around its nominal value of -0.7V. Assuming that all other device parameters always retain their nominal values, find the upper and lower limits of the switching threshold V_M of the circuit you designed in Problem 3.2.

4 CMOS Inverter in Feedback

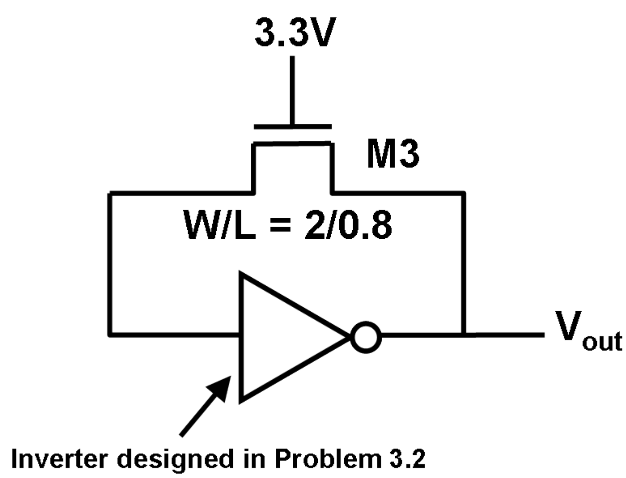

Figure 2: CMOS inverter in feedback configuration with NMOS device M3.

Consider the CMOS inverter you designed in Problem 3.2, with the circuit configuration shown in Figure 2.

Problem 4.1 Calculate the output voltage level V_{out}.

Problem 4.2 Determine if the process-related variation of $V_{T0,n}$ of transistor M3 has any influence on the output voltage V_{out}.

Problem 4.3 Calculate the **total current** being drawn from the power supply source, and determine its variation due to process-related threshold voltage variations.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.