EEC 118 Spring 2011 Homework #1

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Reading: Rabaey, Chapters 1 and 3 [1].
Reference: Kang and Leblebici, Chapters 1 and 3 [2].

1 IC Trends

Problem 1.1 Moore's Law for Microprocessors. Figure 1 shows an updated plot of transistor count for microprocessors [3]. Based on the evolutionary trends described in Chapter 1 of Rabaey, predict the integration complexity and the clock speed of a microprocessor in the years 2010, 2015, and 2020.

Problem 1.2 Moore's Law for DRAM. Determine also how much DRAM should be available on a single chip at those points in time, if Moore's law would still hold.

2 Quality Metrics

Problem 2.1 Metrics Priority. Consider the four quality metrics described in Chapter 1: cost, functionality and robustness, performance, and power. If you were managing an IC design team, how would you rank these metrics from most important to least important for your product? Justify your answer.

3 MOS Transistor

Problem 3.1 Threshold Voltage. While the threshold voltage parameter V_{T0} is typically determined empirically, a simple analytical model can be developed for it [2]:

$$V_{T0} = \phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \tag{1}$$

where Q_{B0} is the depletion region charge density surface inversion ($\phi_s = -\phi_F$):

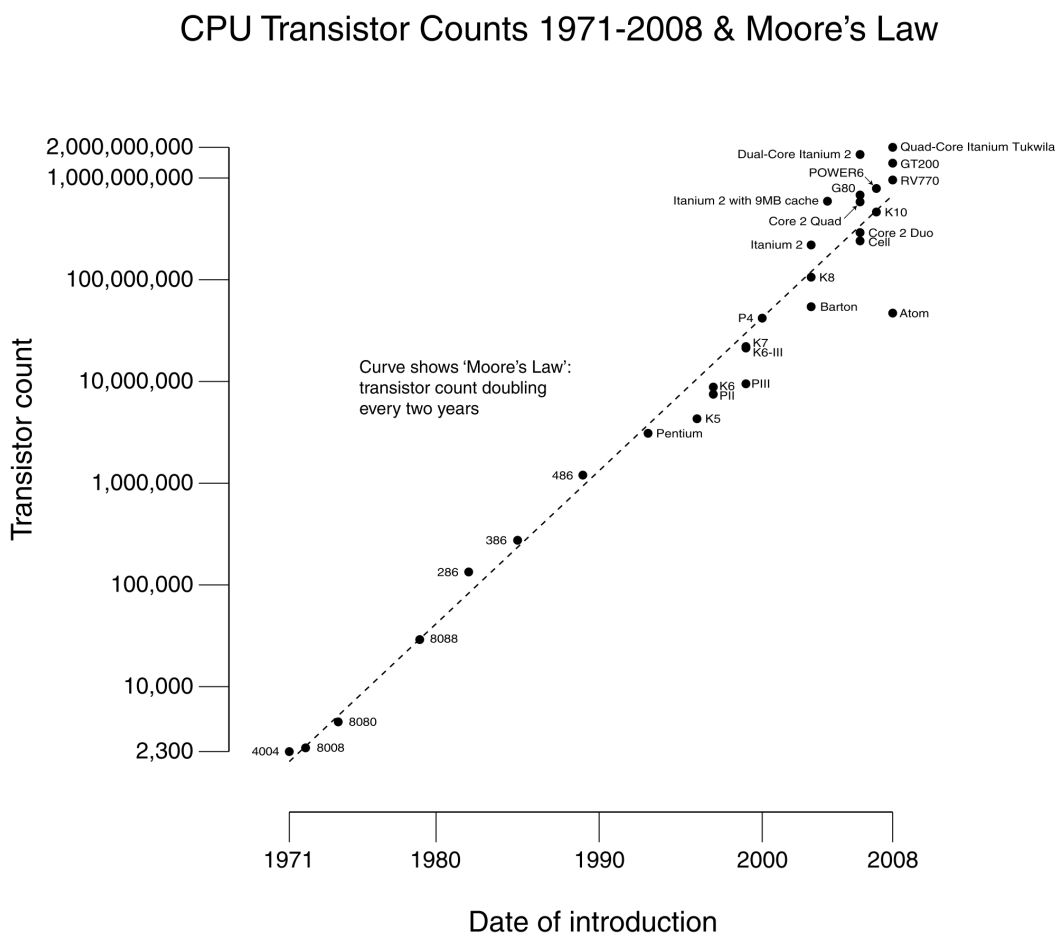

Figure 1: Moore's Law [3].

$$Q_{B0} = -\sqrt{2qN_A\epsilon_{Si}|-2\phi_F|} \tag{2}$$

Note the change in sign compared to Equation 3.17 on p. 90 in Rabaey [1].

Consider an MOS system with the following parameters:

- $t_{ox} = 200\text{Å}$
- $\phi_{GC} = -0.85\text{V}$
- $-2\phi_F = 0.6\text{V}$
- $N_A = 2 \times 10^{15}\text{cm}^{-3}$
- $Q_{ox} = 2 \times 10^{11}\text{C/cm}^2$

Determine the threshold voltage parameter V_{T0} under zero bias at rooom temperature ($T = 300\text{K}$) given that $\epsilon_{ox} = 3.97\epsilon_0$ and $\epsilon_{Si} = 11.7\epsilon_0$.

Problem 3.2 Channel Implant. The amount of change in the threshold voltage resulting from extra dopants implanted in the channel can be approximated by $\frac{qN_I}{C_{ox}}$, where N_I [cm^{-2}] is the density of implanted impurities. Determine the type (p-type or n-type) and amount of channel implant to change the threshold voltage to 0.8V.

Problem 3.3 Channel Length. Describe the relationship between the drawn channel length L_d and the electrical channel length L. Are they identical? If not, how would you express L in terms of L_d and other device parameters?

Problem 3.4 Biasing. Draw and label an NMOS and PMOS transistor with source, drain, and gate terminals clearly labeled S, D, and G respectively. Assume $V_{SB} = 0\text{V}$. Find the mode of operation (cutoff, linear, or saturation) and drain current I_D for each of the applied biases given below. Assume for the NMOS that $V_{T0} = 1\text{V}$, $W/L = 4/1$, $\gamma = 0.35\text{V}^{1/2}$, $\lambda = 0.05\ \text{V}^{-1}$, $\mu C_{ox} = 350\ \mu\text{A/V}^2$, and $-2\Phi_F = 0.6\ \text{V}$. Assume identical parameters for the PMOS except $V_{T0} = -1\text{V}$ and $\mu C_{ox} = 150\ \mu\text{A/V}^2$. Ignore velocity saturation and subthreshold conduction.

1. NMOS: $V_{GS} = 1.8\text{V}$, $V_{DS} = 1.8\text{V}$; PMOS: $V_{GS} = -1.1\text{V}$, $V_{DS} = -50\text{mV}$
2. NMOS: $V_{GS} = 0.9\text{V}$, $V_{DS} = 1.8\text{V}$; PMOS: $V_{GS} = -2.5\text{V}$, $V_{DS} = -1\text{V}$
3. NMOS: $V_{GS} = 1.5\text{V}$, $V_{DS} = 0.4\text{V}$; PMOS: $V_{GS} = -1.8\text{V}$, $V_{DS} = -1.6\text{V}$

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.

[3] (2010, March) Moore's law. Wikimedia Foundation, Inc. [Online]. Available: http://en.wikipedia.org/wiki/Moore's_law