Problem 1 (7 points) Complete the following Domino-style dynamic logic three-input AND gate. Size the transistors such that the worst case precharge time (rise time for min. size inverter) equals the worst case evaluation time assuming $V_{DD}=3.3\, \text{V}$, $|V_{TN}|=|V_{TP}|=1\, \text{V}$, $\mu_N=3\mu_p=300\, \mu\text{A}/\sqrt{\text{V}}$, $\gamma=0$, $\lambda=0$, $W_{min}=1\, \mu\text{m}$, $L_{min}=1\, \mu\text{m}$. Label the inputs $A$, $B$, $C$, $clk$, the dynamic node $X_b$, and the output $X$.

Problem 2 (3 points) For the following 1 transistor DRAM cell, fill in the boxes labeling the corresponding wires with the appropriate signal names:

- Q: data storage bit
- BL: bit line
- WL: word line

\[ \text{Diagram of 1 transistor DRAM cell} \]