1.1 \[ V_{th} = V_{in} = V_{out} = 1.4 \text{ V} \]

**PMOS**
\[ |V_{ds}| = 1.9 \text{ V} \]
\[ V_{gs} = 3.3 \text{ V} \]
\[ V_{to} = 0.7 \text{ V} \]

\[ |V_{gs} - V_{to}| = 2.6 \text{ V} \]

**NMOS**
\[ V_{ds} = 1.4 \text{ V} \]
\[ V_{gs} = 1.4 \text{ V} \]
\[ V_{ds} > |V_{gs} - V_{to}| \]

\[ I_D = \frac{M_n C_o x}{2} \frac{W}{L} \left( \frac{2(3.3 - 0.7)}{1.9} \right)^2 \]

\[ I_D = I_D \]

\[ \frac{W_n}{W_p} = 4.08 \]

It is 4.38 times bigger than that \[ \frac{W_n}{W_p} \]

We need bigger NMOS here.

1.2 \[ V_{oh} \]

\[ V_{in} = 0 \Rightarrow \text{then NMOS is cut-off,} \]
\[ V_{ds} > V_{to} \text{ conducts but no current then} \]
\[ \text{no voltage drop at } V_{ds} \Rightarrow V_{out} = V_{oh} = 3.3 \text{ V} \]

\[ V_{oh} \]

Assume \[ V_{in} = V_{oh} = V_{dd} = 3.3 \text{ V} \] then NMOS is linear b/c \[ V_{ds} < (V_{gs} - V_{to}) \]

PMOS is in saturation

\[ I_D = \frac{M_n C_o x}{2} \frac{W}{L} \left( 2(3.3 - 0.6)V_{ol} - V_{ol}^2 \right) \]

\[ I_D = \frac{M_n C_o x}{2} \frac{W}{L} \left( 3.3^2 - 1.071 \right)^2 \]

\[ I_D = I_D \Rightarrow V_{ol} = 5.4V_{ol} + 0.69 = 0 \]

\[ V_{ol} = 0.13 \text{ V} \]
\[ V_{in} = V_{IL} \text{ then } \text{NMOS } V_{bs} > (V_{GS} - V_t) \text{ saturation} \]
\[ \text{PMOS } V_{bs} > V_{GS} - V_t \text{ linear region} \]
\[ I_{DN} = I_{DP} \]
\[ \frac{M_n \text{Cox}}{2} = \frac{W_n}{L} (V_{IL} - 0.6)^2 = \frac{M_p \text{Cox}}{2} \frac{W_p}{L} (2\sigma_3 - 1.07)(V_{out} - 3.3) - (V_{out} - 3.3)^2 \]
\[ V_{out} = 9.79 V_{IL} - 5.175 \]
\[ \frac{dV_{out}}{dV_{in}} = 9.79 (2(V_{IL} - 0.6)) = -5.2 \left( \frac{-1}{dV_{out}} \right) - 2 \left( \frac{-1}{dV_{in}} \right)(V_{out} - 3.3) \]
\[ V_{out} = 0.85 \text{v} \]

\[ V_{IH} \]
\[ V_{in} = V_{IH} \text{ then } \text{NMOS } V_{bs} > V_{GS} - V_t \text{ linear} \]
\[ \text{PMOS } V_{bs} > V_{GS} - V_t \text{ saturation} \]
\[ \frac{M_n \text{Cox}}{2} = \frac{W_n}{L} \left[ 2(V_{IH} - 0.6)V_{out} - V_{out}^2 \right] = \frac{M_p \text{Cox}}{2} \frac{W_p}{L} (3.3 - 0.7)^2 \]
\[ \frac{dV_{out}}{dV_{in}} = 2V_{out} + 2(V_{IH} - 0.6)\left( \frac{-1}{dV_{out}} \right) - 2V_{out} \cdot \left( \frac{-1}{dV_{in}} \right) = 0 \Rightarrow V_{out} = 0.5V_{IH} - 0.3 \]

\[ V_{IH} = 1.56 \text{v} \]
1.3) Want \( V_{OL} = 0.6V \)

PMOS: \( V_{DS} = -3.3V \), \( V_{GS} = -7.7V \), \( V_{DS} - V_{TP} = -3.3V - (-0.7V) = -2.6V \) 

\( \text{saturation} \)

NMOS: \( V_{GS} = V_{OL} = 0.6V \)

\( \text{Assume linear} \)

\[
I_{DS} = I_{OS} \Rightarrow \frac{\mu C_{ox} L}{2} \left[ 2 (V_{in} - V_{TH,N}) V_{OL} - V_{OL}^2 \right] = \frac{\mu C_{ox} L}{2} \left[ -V_{DS} - V_{TH,P} \right]^2
\]

\[
\frac{60 \mu A/V^2}{8} \left[ 2 (V_{in} - 0.6V) (0.6V) - (0.6V)^2 \right] = \frac{25 \mu A/V^2}{2} \left[ 3.3V + 0.7V \right]^2
\]

\( V_{in} = 4.42V \)

\( V_{DS} = V_{in} \), \( 4.42V - 0.6V = 3.82V > V_{DS} = 0.6V \) \( \text{linear} \)
2.1. The highest voltage $V_{out}$ can reach before NMOS cuts off is $V_{DD} - V_{T,n} \Rightarrow V_{OH} = V_{DD} - V_{T,n}$.

The lowest voltage $V_{out}$ can reach before PMOS cuts off is $0V - V_{T,p} \Rightarrow V_{OL} = |V_{T,p}|$ ($V_{T,p} < 0$).

![Circuit Diagram](image)

**Figure 2:** Circuit X.

**VTC:**

$V_{OH} = V_{DD} - V_{T,n}$

$V_{OL} = |V_{T,p}|$

**Truth Table:**

<table>
<thead>
<tr>
<th>in</th>
<th>out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

buffer!

$F = X$
Not enough information to calculate exactly, so make some plausible assumptions:

Assume $K_R = 1$ (just like ideal CMOS inverter)

$V_{T,n} = |V_{T,p}|$ (symmetric device thresholds)

$V_{DD} > V_{T,n} + |V_{T,p}|$ (devices both on at same time under some $V_{in}$ conditions)

Under these assumptions, the device currents for both NMOS and PMOS are equal for equal $V_{GS}$ ($V_{GS,n} = V_{GS,p}$).

Since $V_{TH} = V_{in} = V_{out} \Rightarrow V_{GS,p} = V_{GS,n} = 0 \Rightarrow$ NMOS, PMOS both in cutoff, $I_{D,n} = I_{D,p} = 0$

However, they have finite impedance due to subthreshold conduction, these will be equal, therefore:

$$V_{TH} = \frac{V_{DD}}{2}$$

**Graphical solution:**

(same assumptions as above)

Three points where $V_{TC}$ meets $V_{in} = V_{out}$ line. Two of those points are where $V_{out} = V_{OL}$ and $V_{out} = V_{OH} \Rightarrow$ circuit is not switching.

$$V_{TH} = \frac{V_{DD}}{2}$$ (third point)
2.3 Suppose the input can swing between 0V and \( V_{DD} \):
\[
\Delta V_{in} = V_{DD} - 0V = V_{DD}
\]
The output can only swing from
\[
\Delta V_{out} = V_{OH} - V_{OL} = V_{DD} - V_{Tn} = |V_{Tp}| < \Delta V_{in}
\]

2.4 Normally, we want logic gate output swings to be larger than input swings (this is called level restoration) so that input noise affects the output less. Therefore, this buffer is not suitable as a logic gate since \( \Delta V_{out} < \Delta V_{in} \).