EEC 118 Lecture #5: MOS Fabrication

Rajeevan Amirtharajah
University of California, Davis
Jeff Parkhurst
Intel Corporation

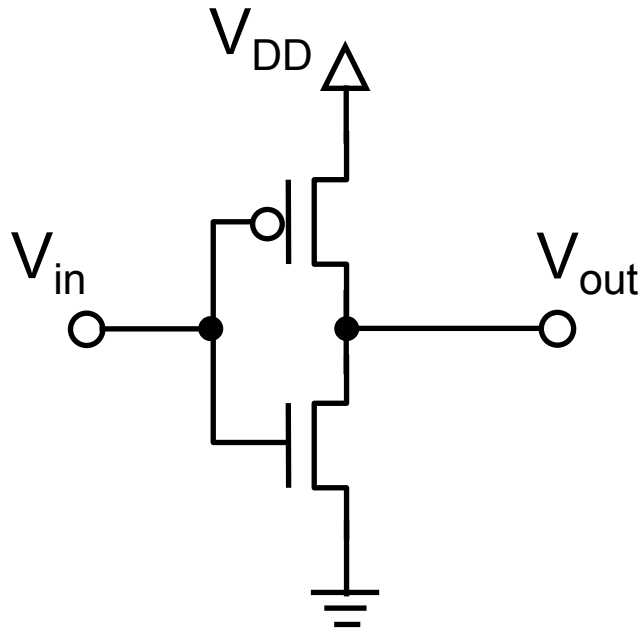
Announcements

- **Lab 3 this week, report due next week**
- **HW 3 due this Friday at 4 PM in box, Kemper 2131**
- **Quiz 1 today!**

Outline

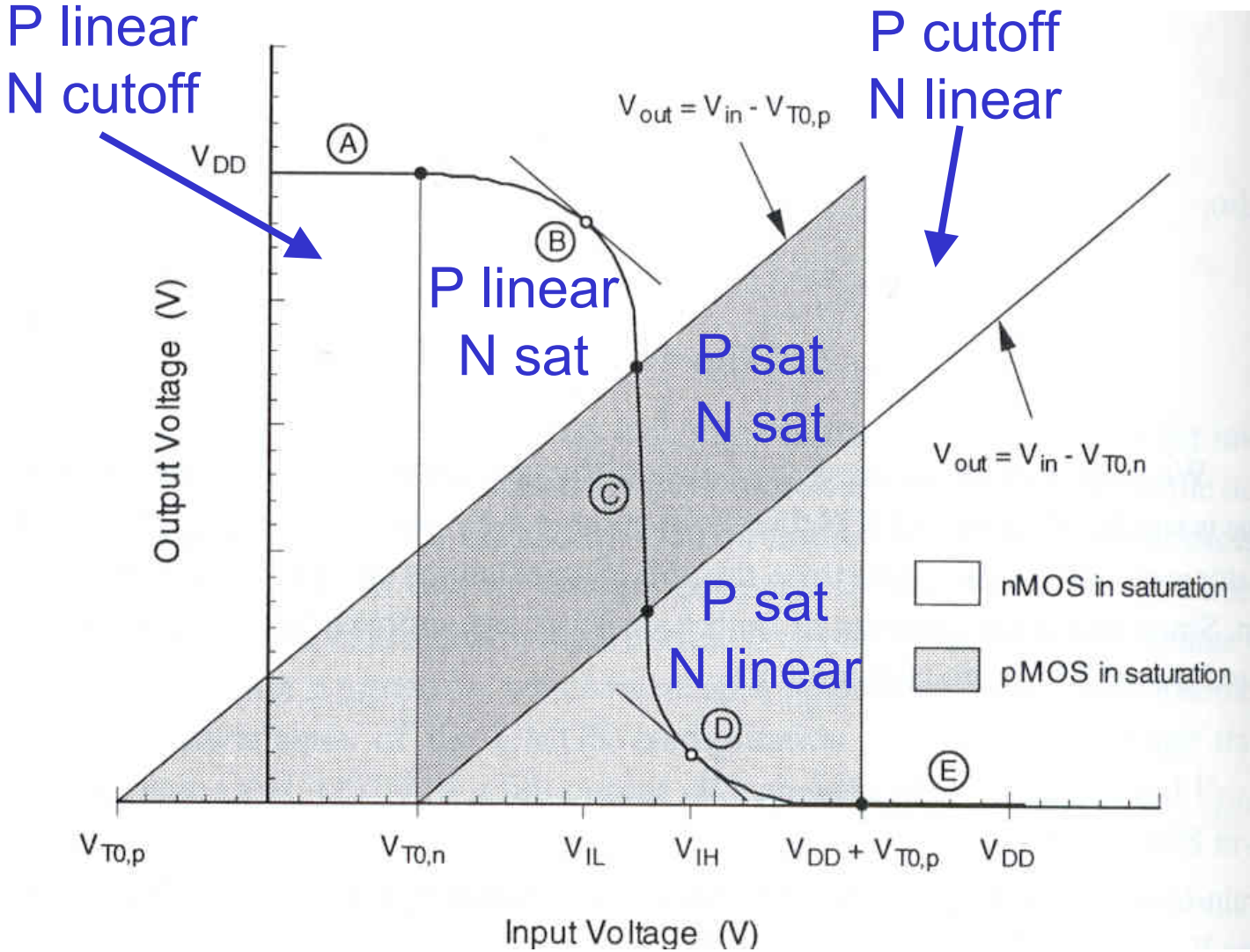
- **Review: CMOS Inverter Transfer Characteristics**
- **CMOS Inverters: Rabaey 5.3-5.5 (Kang & Leblebici, 5.1-5.3 and 6.1-6.2)**
- **MOS Fabrication: Rabaey Chapter 2 (Kang & Leblebici, Chapter 2)**

Review: CMOS Inverter Operation

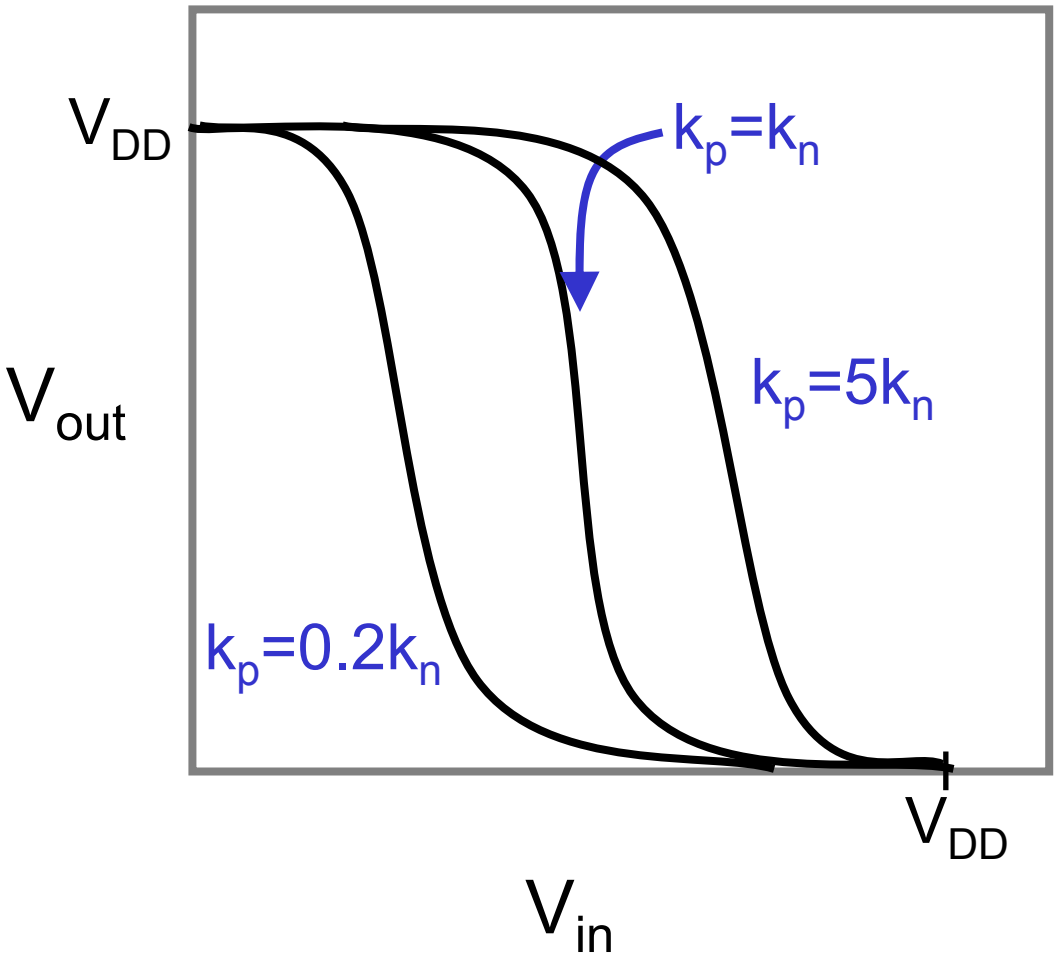


- **NMOS transistor:**
  - Cutoff if $V_{in} < V_{TN}$
  - Linear if $V_{out} < V_{in} - V_{TN}$
  - Saturated if $V_{out} > V_{in} - V_{TN}$
- **PMOS transistor**
  - Cutoff if $(V_{in}-V_{DD}) < V_{TP} \rightarrow V_{in} < V_{DD}+V_{TP}$
  - Linear if $(V_{out}-V_{DD})>V_{in}-V_{DD}-V_{TP} \rightarrow V_{out}>V_{in} - V_{TP}$
  - Sat. if $(V_{out}-V_{DD})<V_{in}-V_{DD}-V_{TP} \rightarrow V_{out} < V_{in}-V_{TP}$

Review: CMOS Inverter VTC Operation

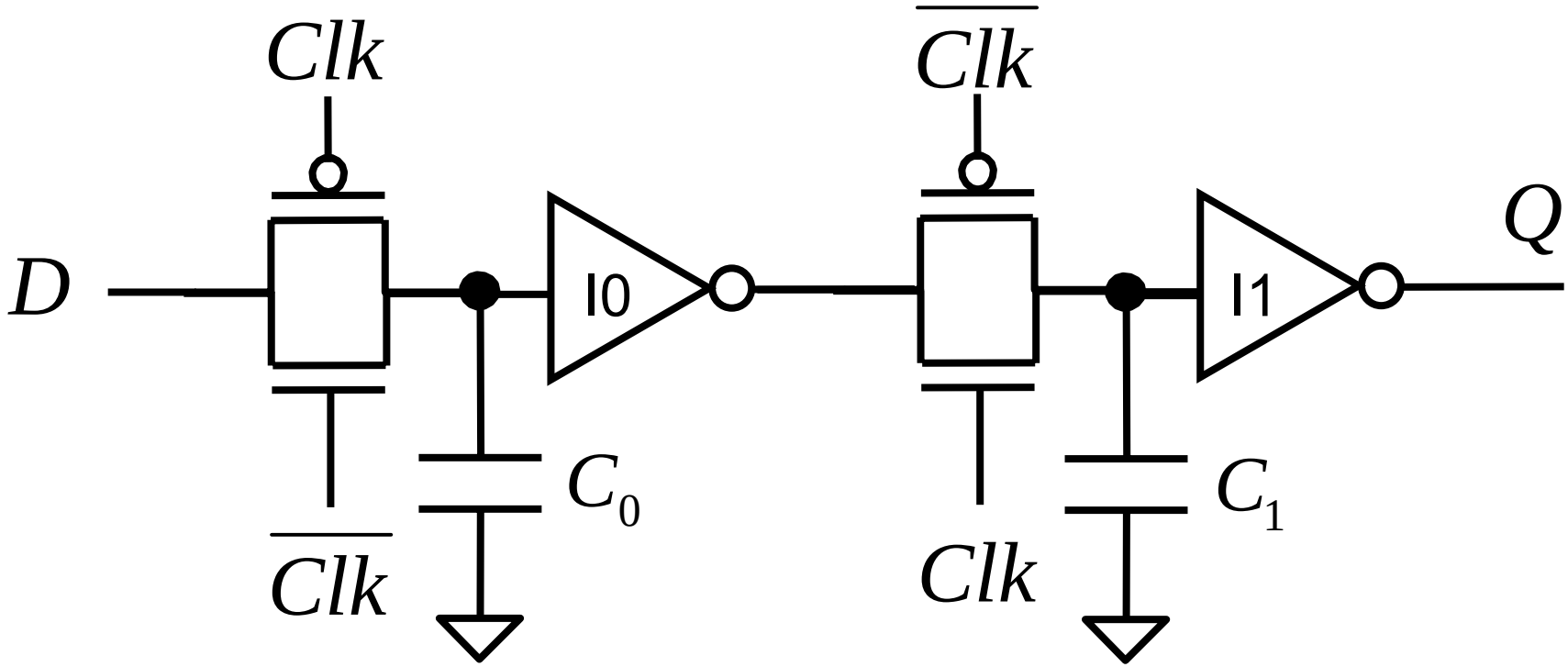


Review: CMOS Inverter VTC Sizing



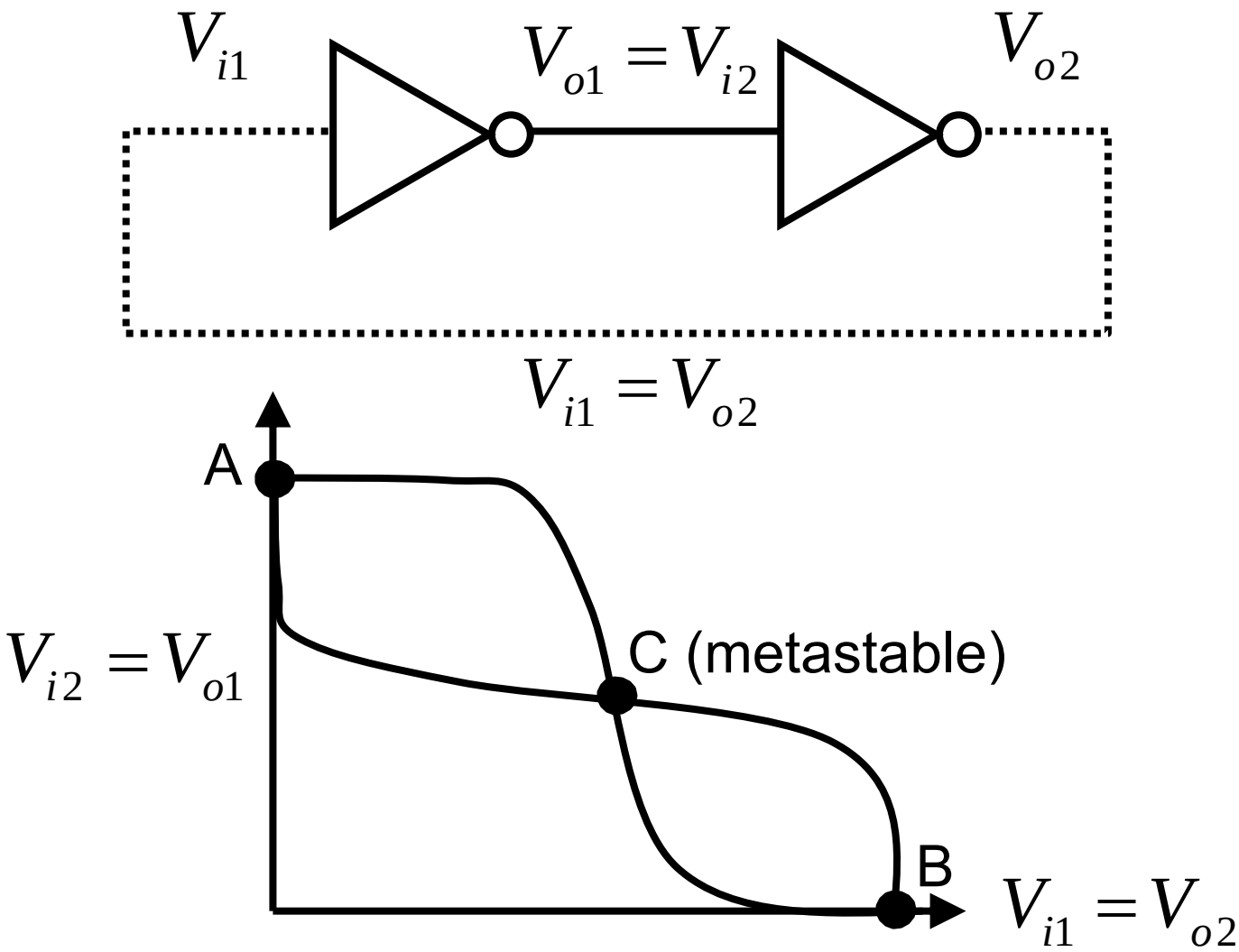
- Increase W of PMOS
  - k_p increases
  - VTC moves to right
- Increase W of NMOS
  - k_n increases
  - VTC moves to left
- For $V_{TH} = V_{DD}/2$
  - $k_n = k_p$
  - $2W_n$ or $3W_n \approx W_p$

Preview: Dynamic Positive Edge-Triggered FF

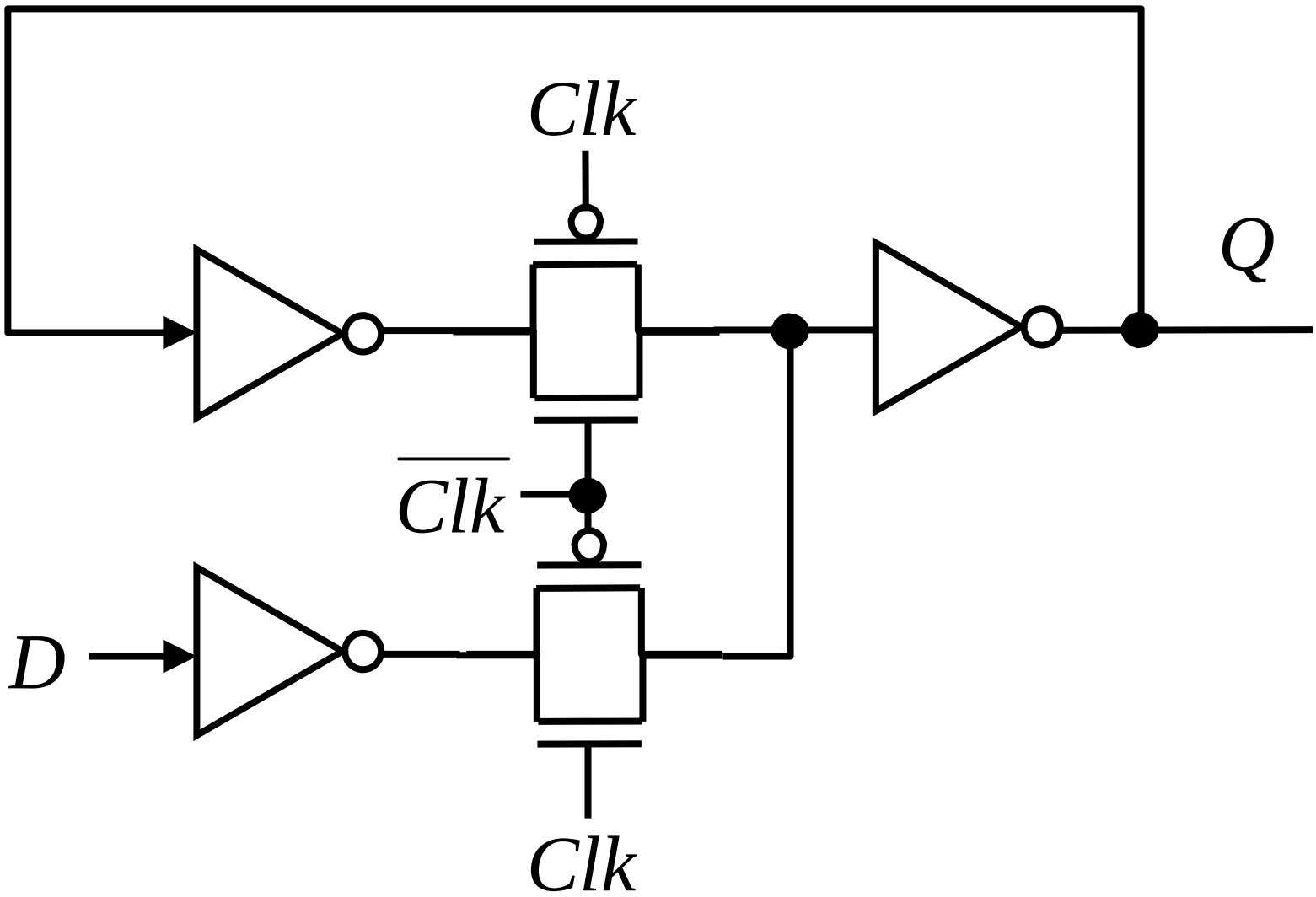


- **No feedback devices**
- **Data stored on input capacitances of inverters I0 and I1**
- **Dynamic logic issues apply: leakage, capacitive coupling, charge sharing**

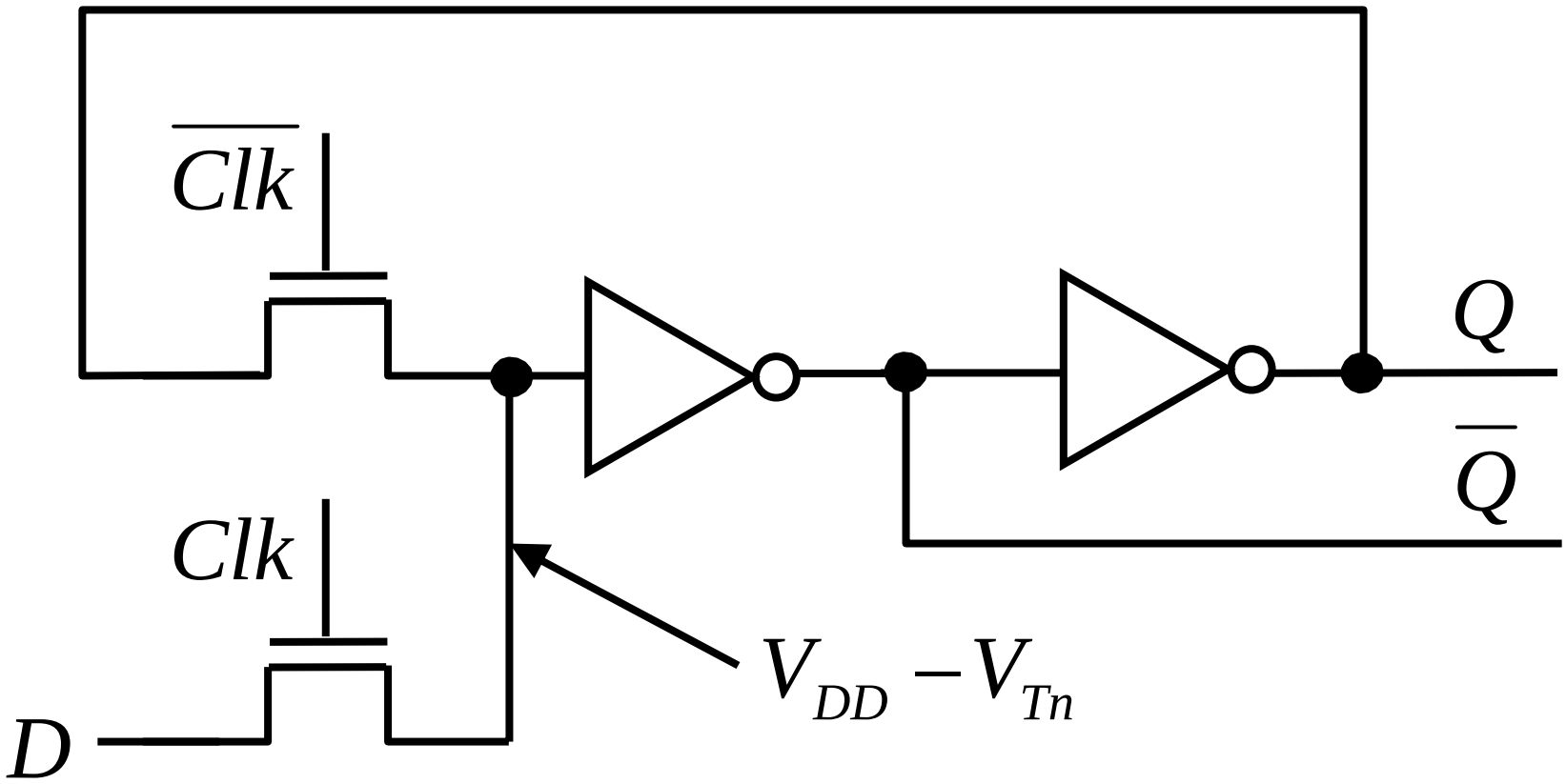
Preview: Static Latch Bistability



Preview: Transmission Gate Positive Latch



Preview: NMOS Pass Gate Positive Latch

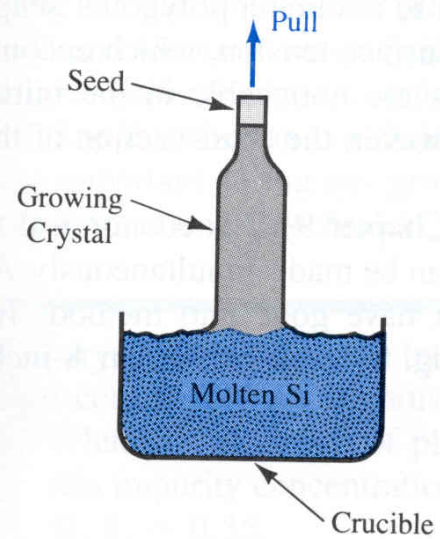


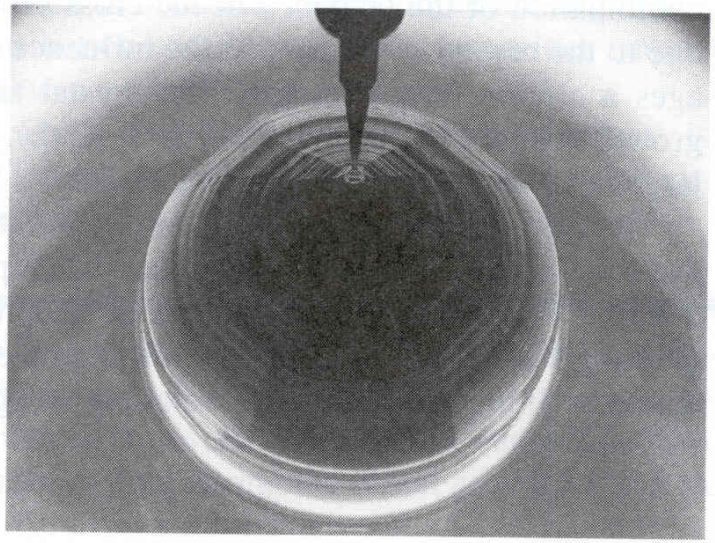
- **Fewer devices, less area, lower clock load**
- **Threshold drop on internal nodes implies more static power, less noise margin**

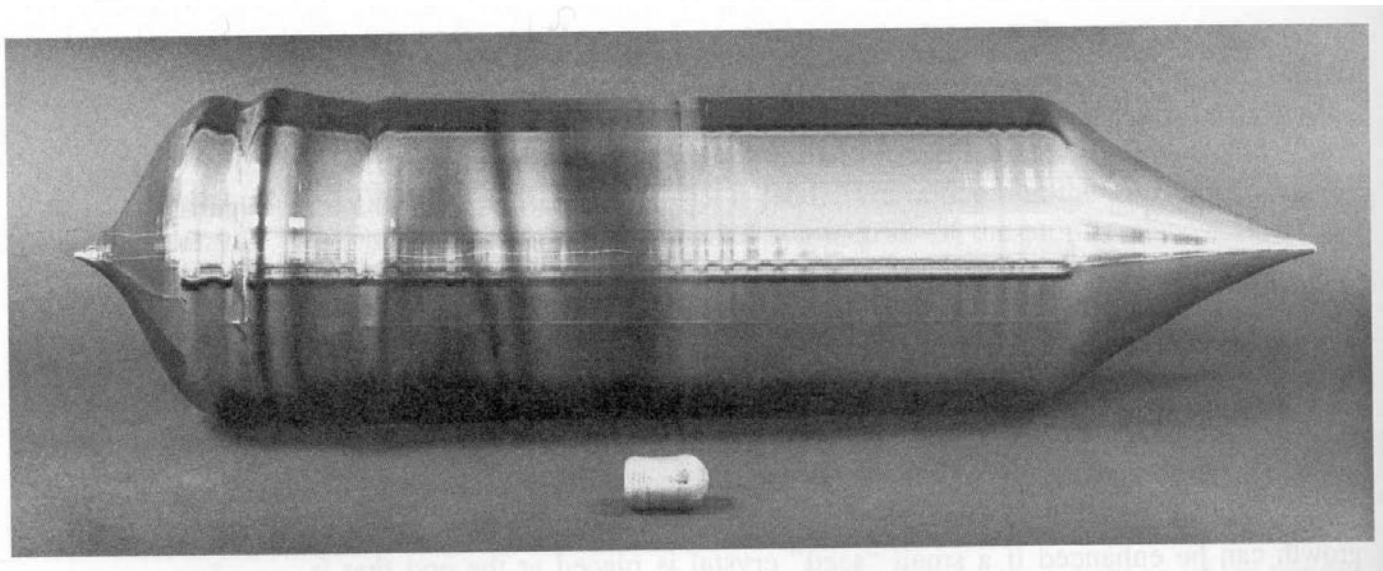
Fabrication Process

- **Substrate is grown and then cut**
  - Round silicon wafers are used
  - Purity emphasized to prevent impurities from affecting operation (99.9999% pure)
- **Each layer deposited separately**
- **Some layers used as masks for later layers**
- **Planar process is important**
  - Requires minimum percent usage of metal to ensure flatness

Silicon Substrate Manufacturing



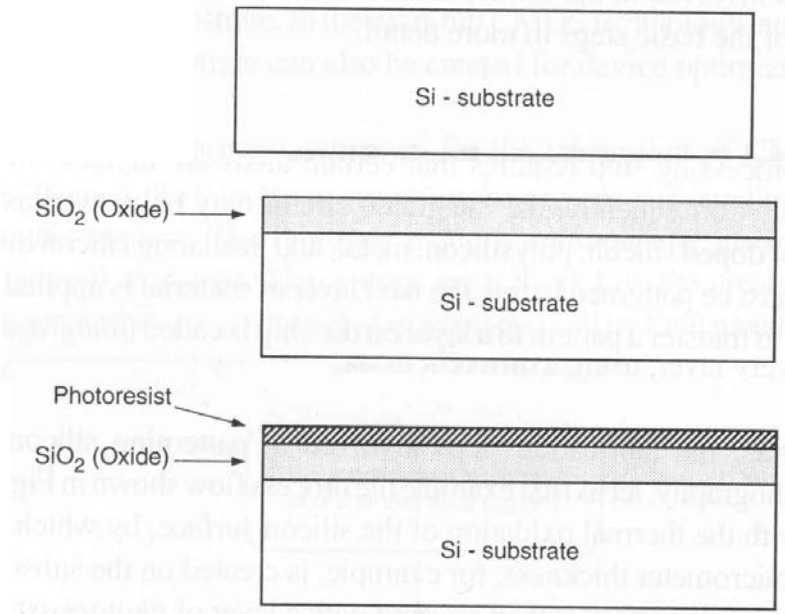


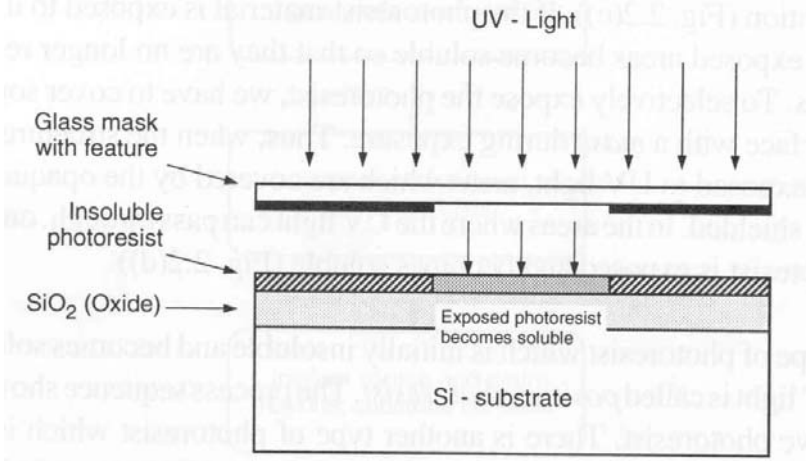


Building a Golf Course with Similar Process

- **Plane drops materials from the air**
  - Sand, then dirt, then grass seeds, then trees
  - Certain masks applied during process to prevent material from hitting particular areas
  - For instance: After Sand, mask placed over areas where sand trap will exist. Mask later taken off at end of process to reveal sand trap.

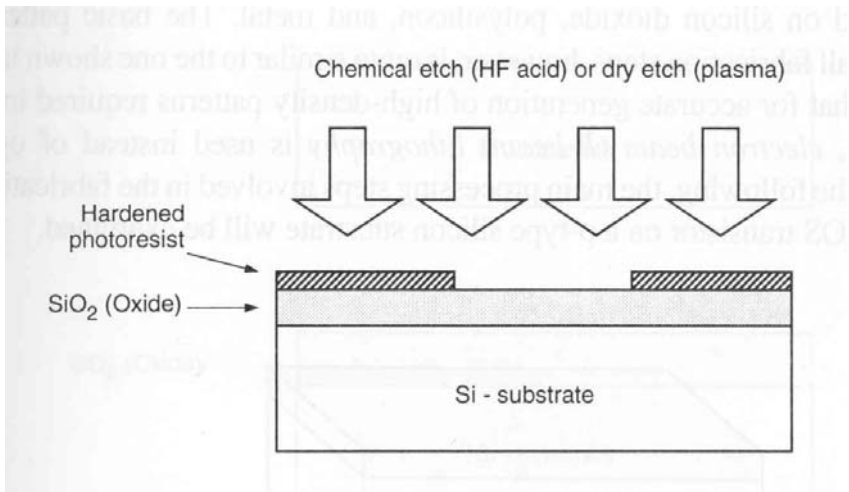
Fabrication: Patterning of SiO_2 Step I

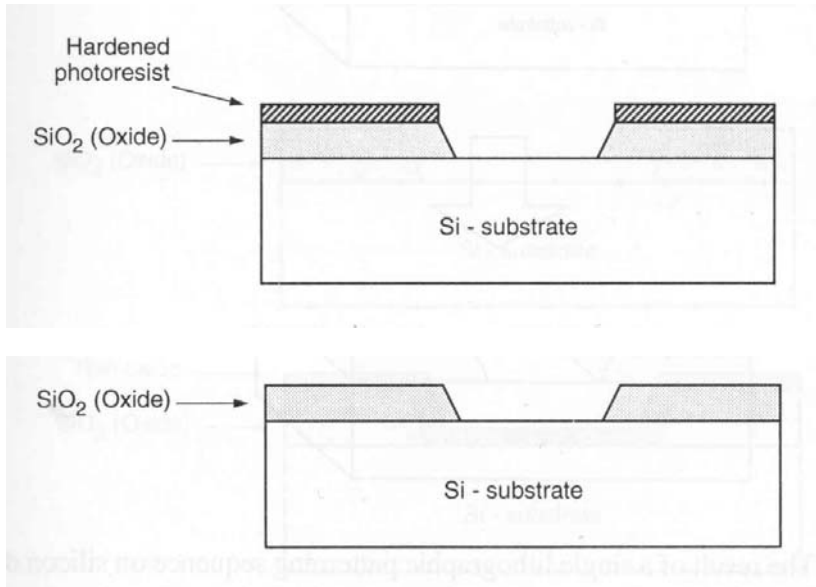




- **Grow SiO_2 on Si by exposing to O_2**
  - High temperature accelerates this process
- **Cover surface with photoresist (PR)**
  - Sensitive to UV light (wavelength determines feature size)
  - Positive PR becomes soluble after exposure
  - Negative PR becomes insoluble after exposure

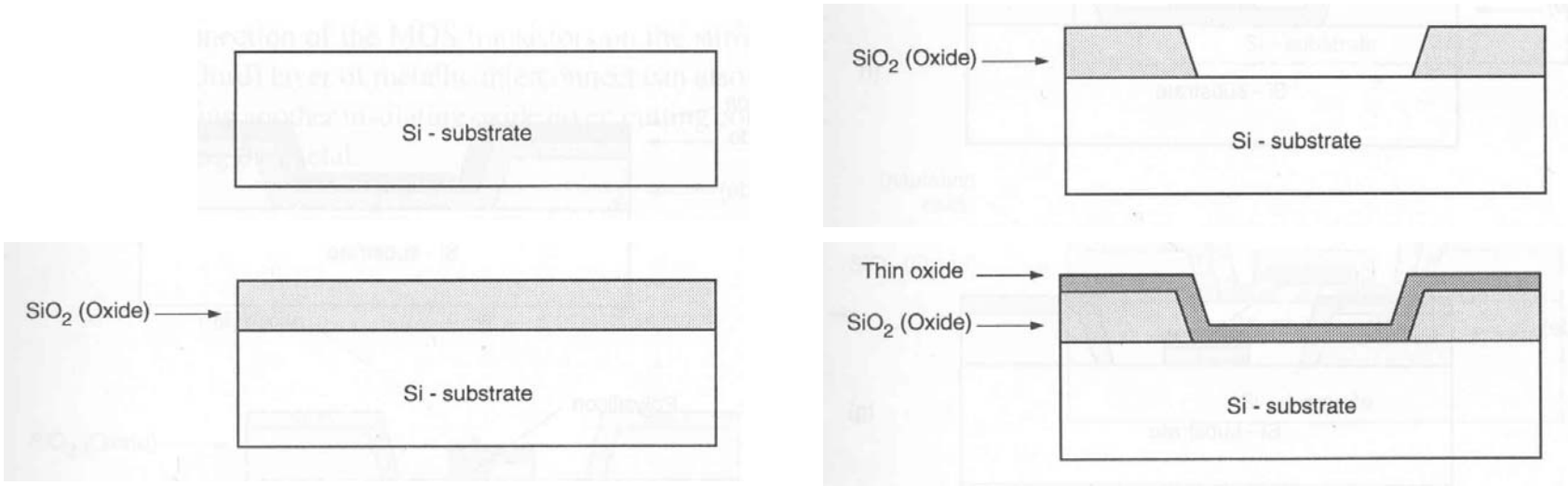
Fabrication: Patterning of SiO_2 Step II





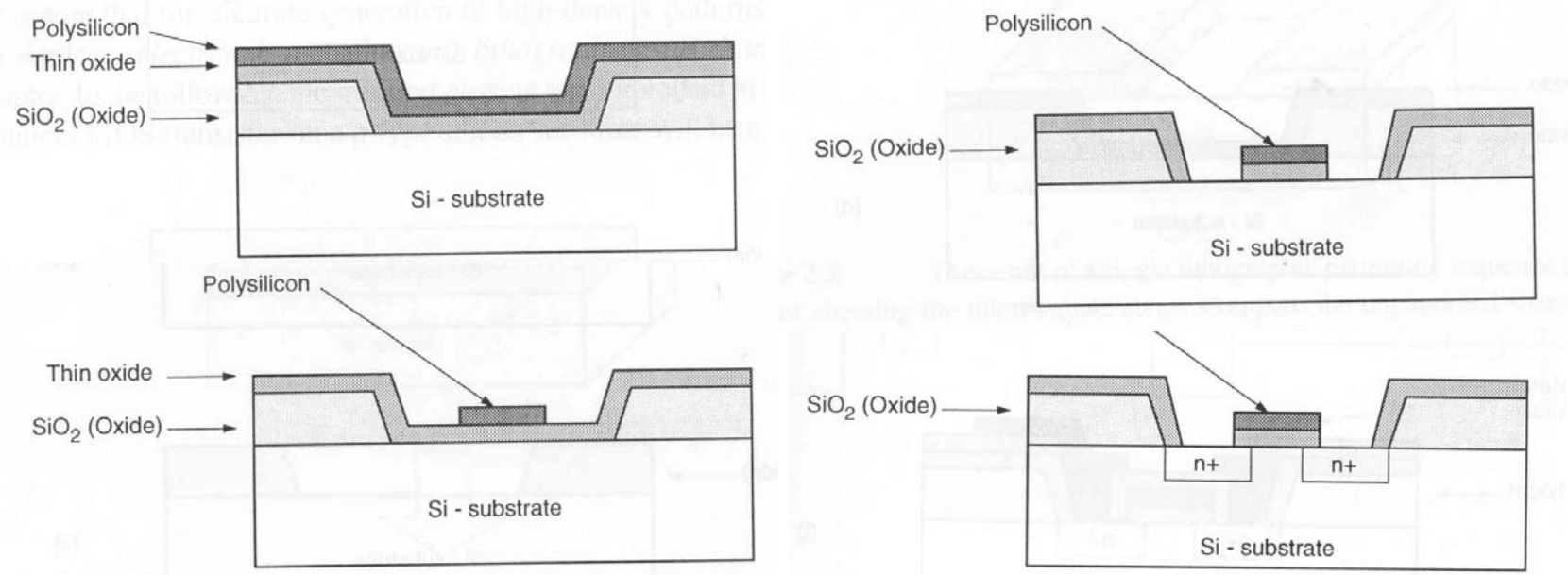
- **Exposed PR removed with a solvent**
- **SiO_2 removed by etching (HF – hydrofluoric acid)**
- **Remaining PR removed with another solvent**

NMOS Transistor Fabrication



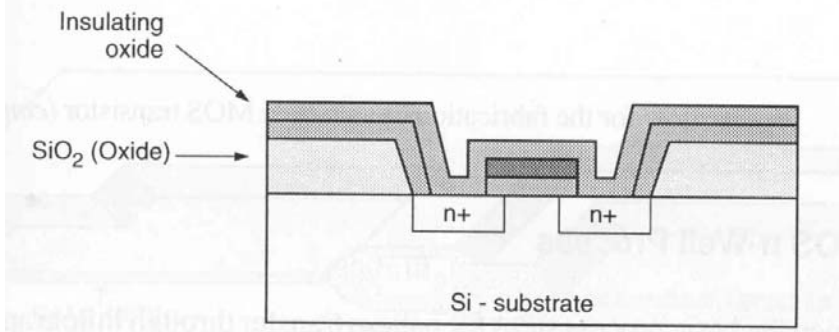
- **Thick field oxide grown**
- **Field oxide etched to create area for transistor**
- **Gate oxide (high quality) grown**

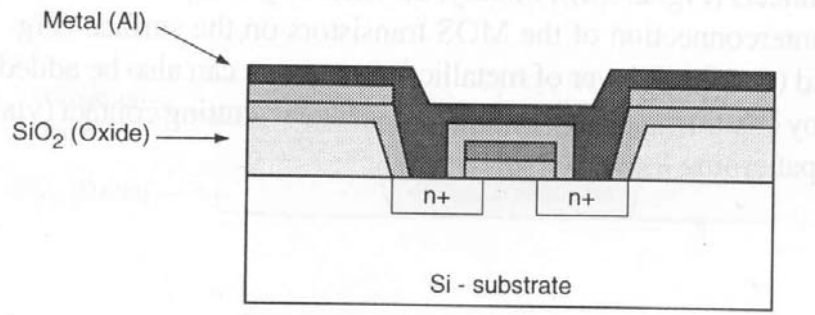
NMOS Transistor Fabrication

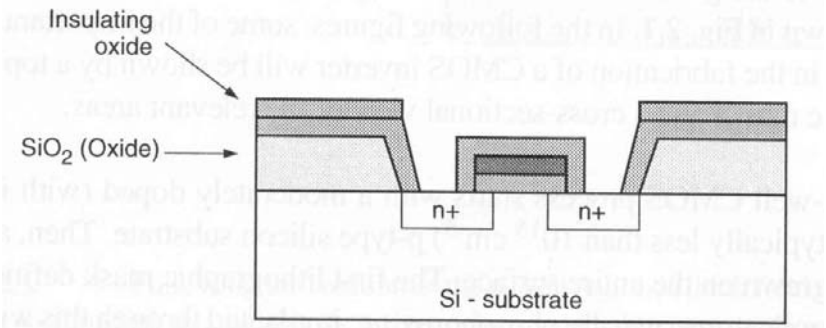


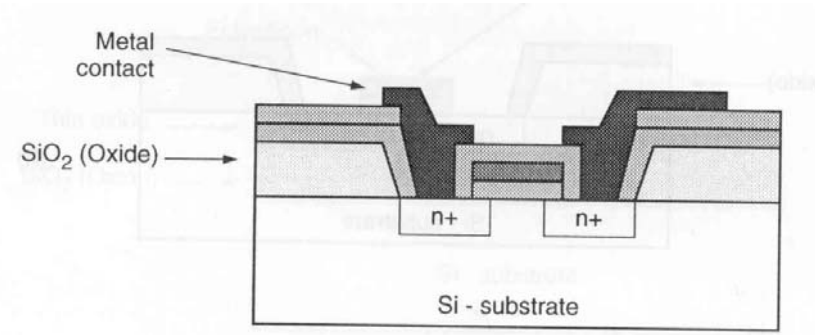
- **Polysilicon deposited (doped to reduce resistance R)**
- **Polysilicon etched to form gate**
- **Gate oxide etched from source and drain**
  - Self-aligned process because source/drain aligned by gate
- **Si doped with donors to create n+ regions**

NMOS Transistor Fabrication



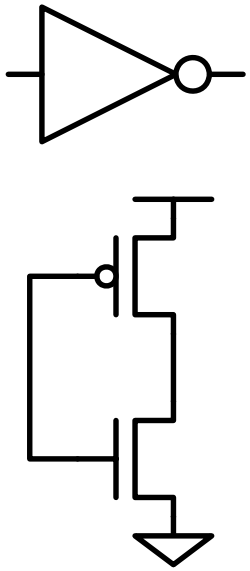


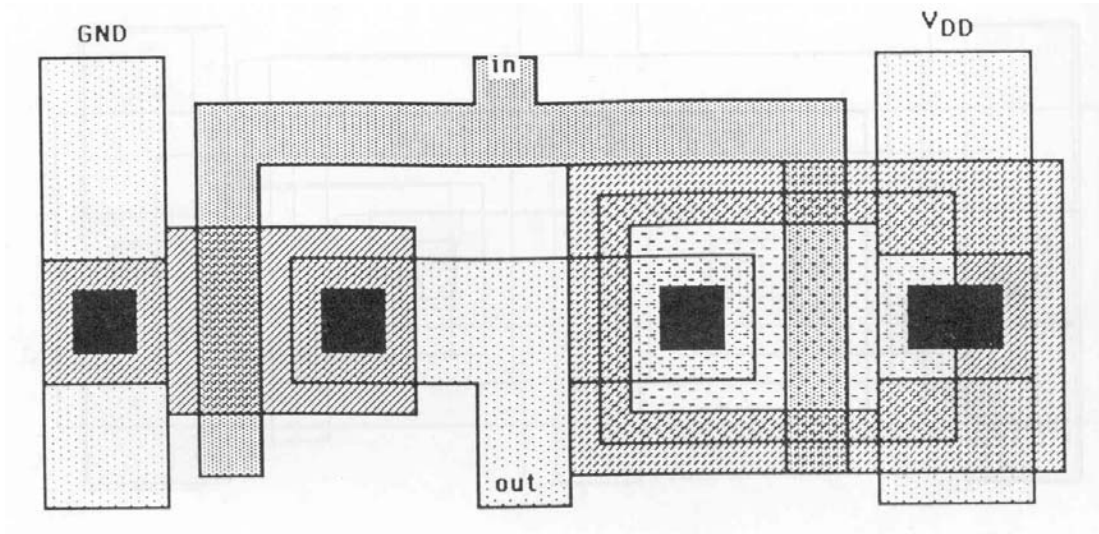




- **Insulating SiO_2 grown to cover surface/gate**
- **Source/Drain regions opened**
- **Aluminum evaporated to cover surface**
- **Aluminum etched to form metal1 interconnects**

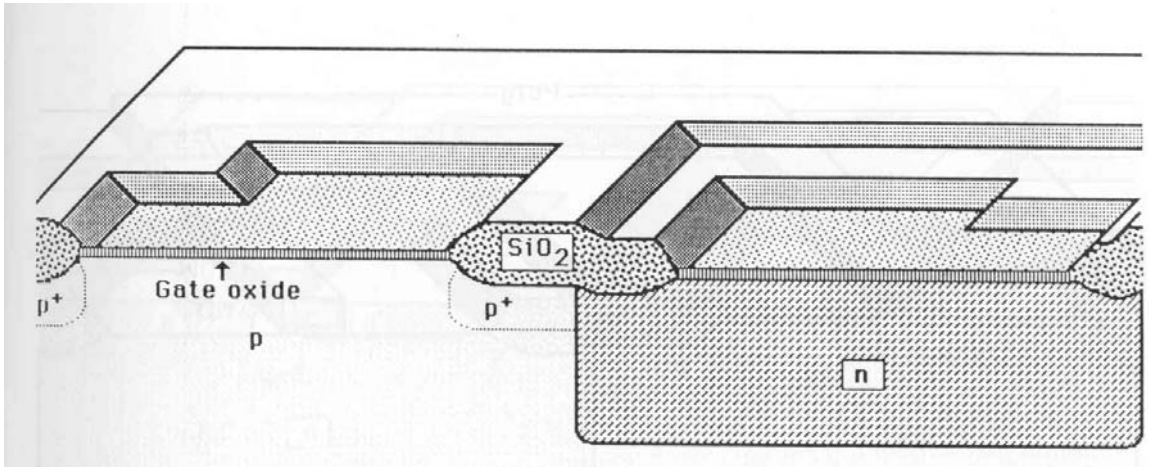
Inverter Fabrication: Layout





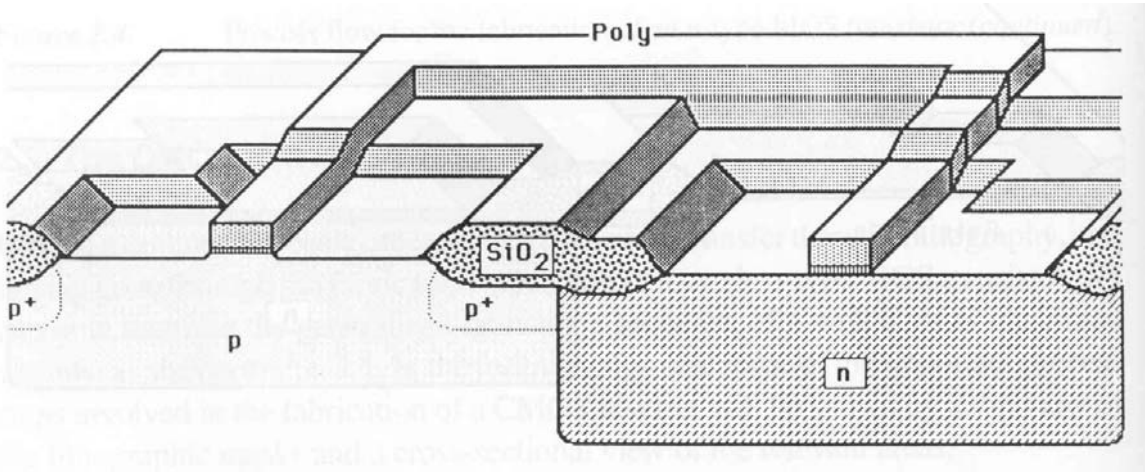
- **Inverter**
  - Logic symbol
  - CMOS inverter circuit
  - CMOS inverter layout (top view of lithographic masks)

Inverter Fabrication: NWELL and Oxides



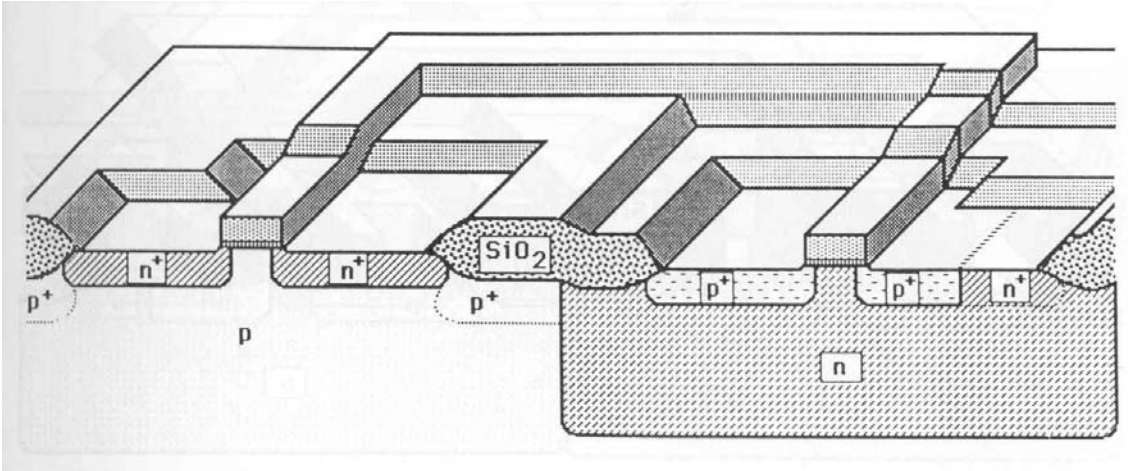
- **N-wells created**
- **Thick field oxide grown surrounding active regions**
- **Thin gate oxide grown over active regions**

Inverter Fabrication: Polysilicon



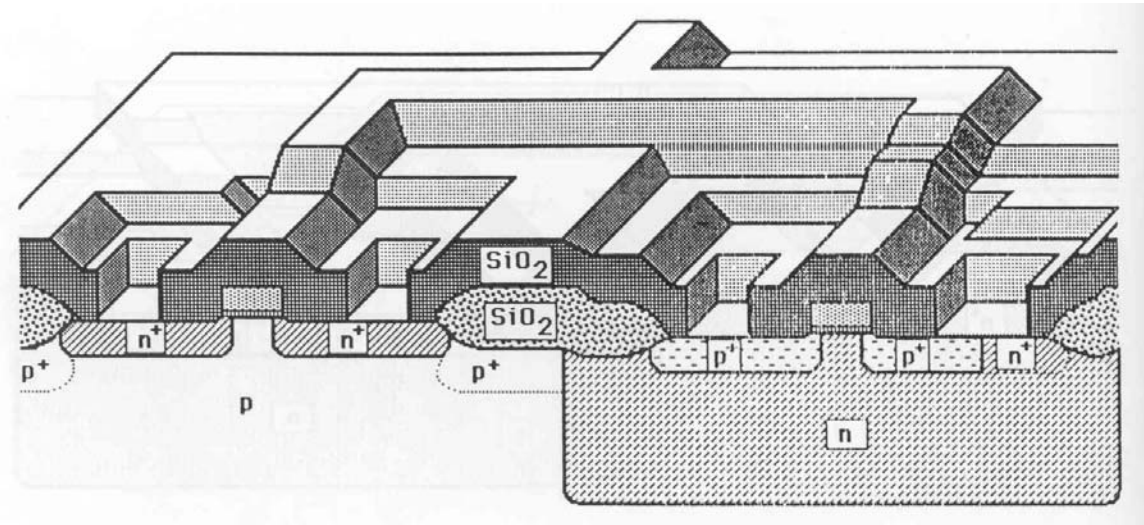
- **Polysilicon deposited**
  - Chemical vapor deposition (Places the Poly)
  - Dry plasma etch (Removes unwanted Poly)

Inverter Fabrication: Diffusions



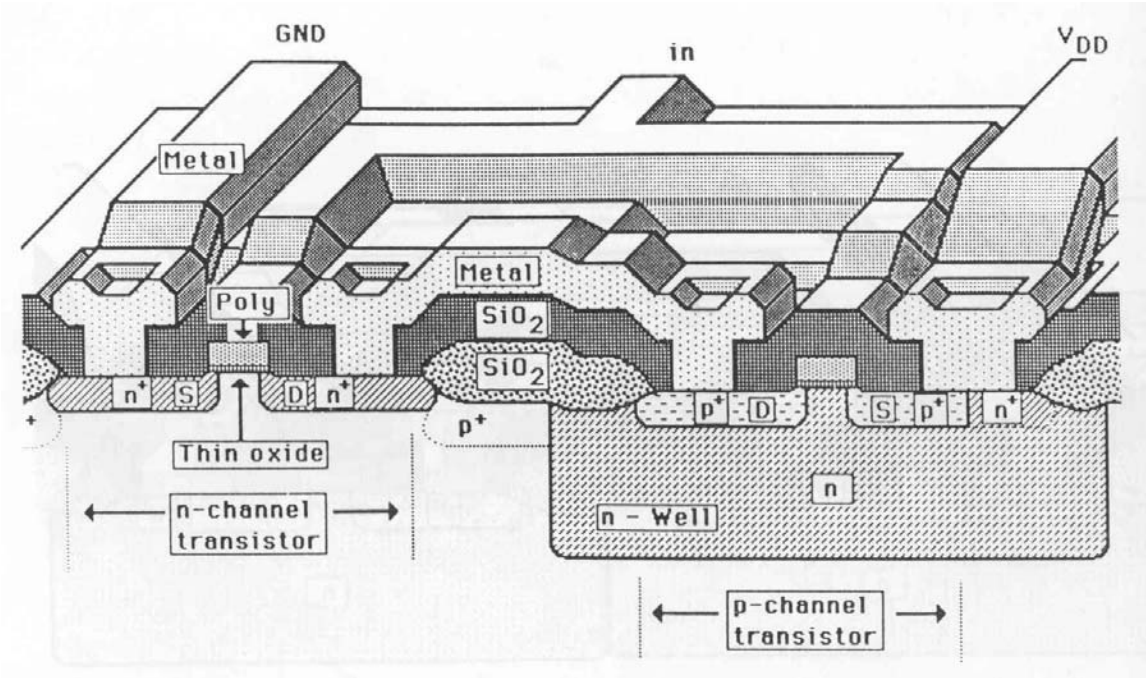
- **N+ and P+ regions created using two masks**
  - Source/Drain regions
  - Self-aligned process since gate is already fabricated
  - Substrate contacts

Inverter Fabrication



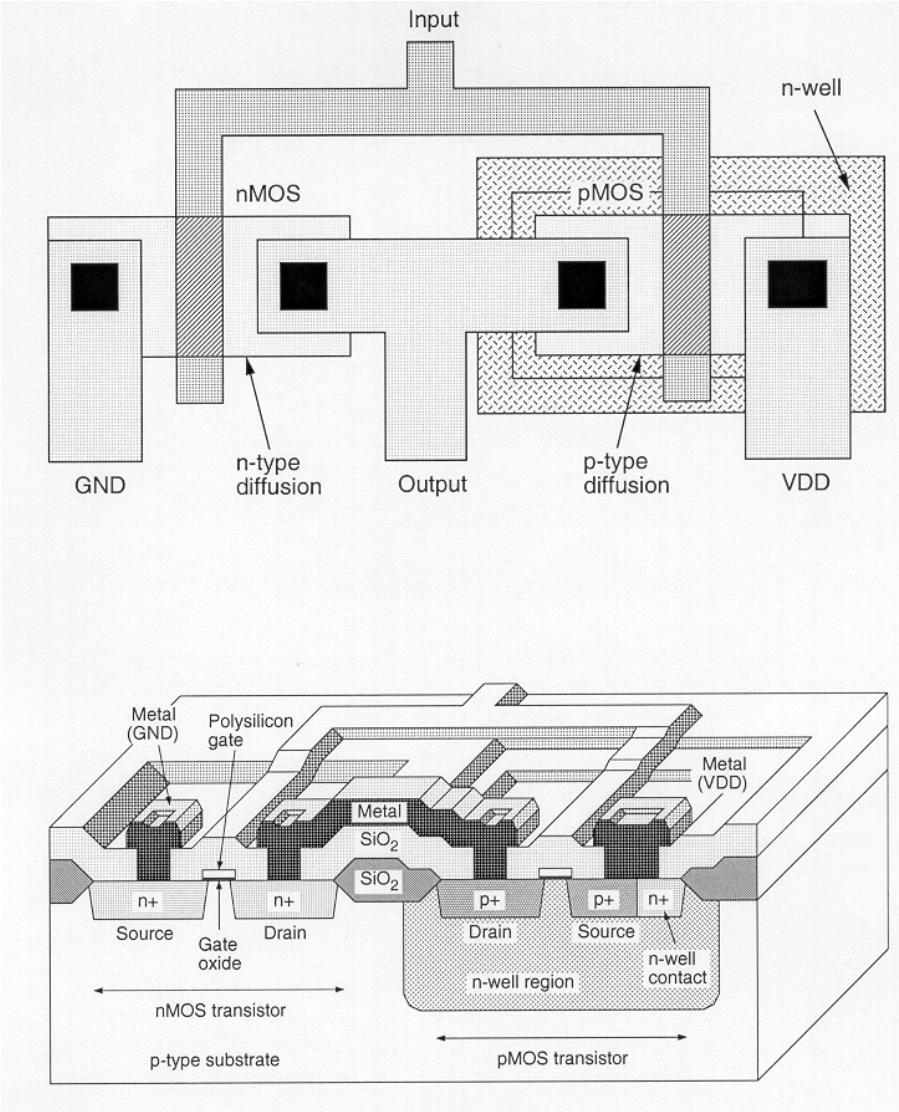
- **Insulating SiO_2 deposited using chemical vapor deposition (CVD)**
- **Source/Drain/Substrate contacts exposed**

Inverter Fabrication



- **Metal (Al, Cu) deposited using evaporation**
- **Metal patterned by etching**
- **Copper is current metal of choice due to low resistivity**

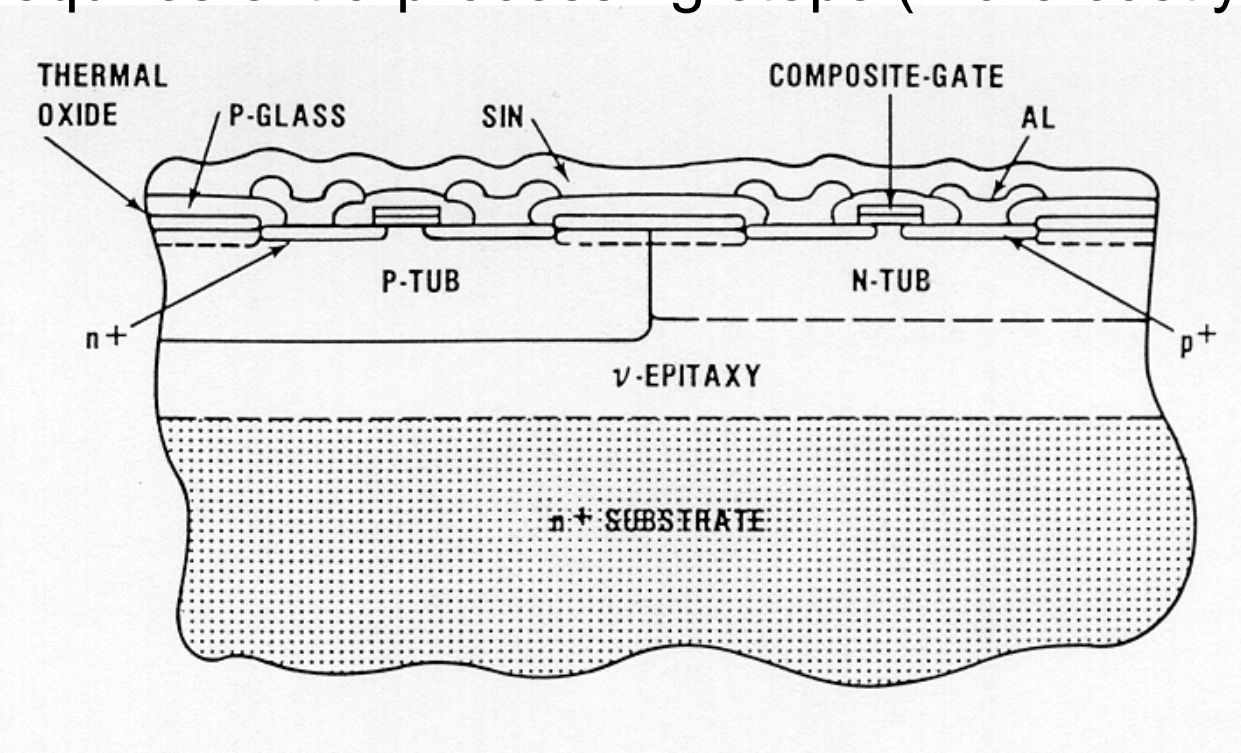
NWELL MOS Process



- **MOS transistors use PN junctions to isolate different regions and prevent current flow.**
- **NWELL is used in P-substrate so that PMOS transistors are isolated and don't share currents.**

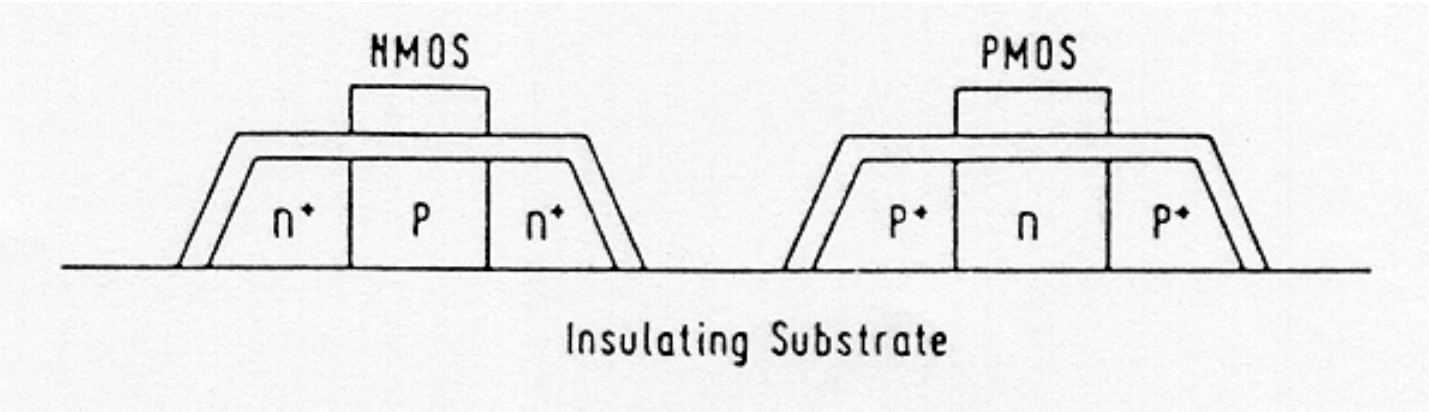
More Complex Processes

- **Twin Well CMOS Process**
  - Can help to avoid body effect
  - Allows for Vt and channel transconductance tuning
  - Requires extra processing steps (more costly)



Silicon-On-Insulator (SOI) Process

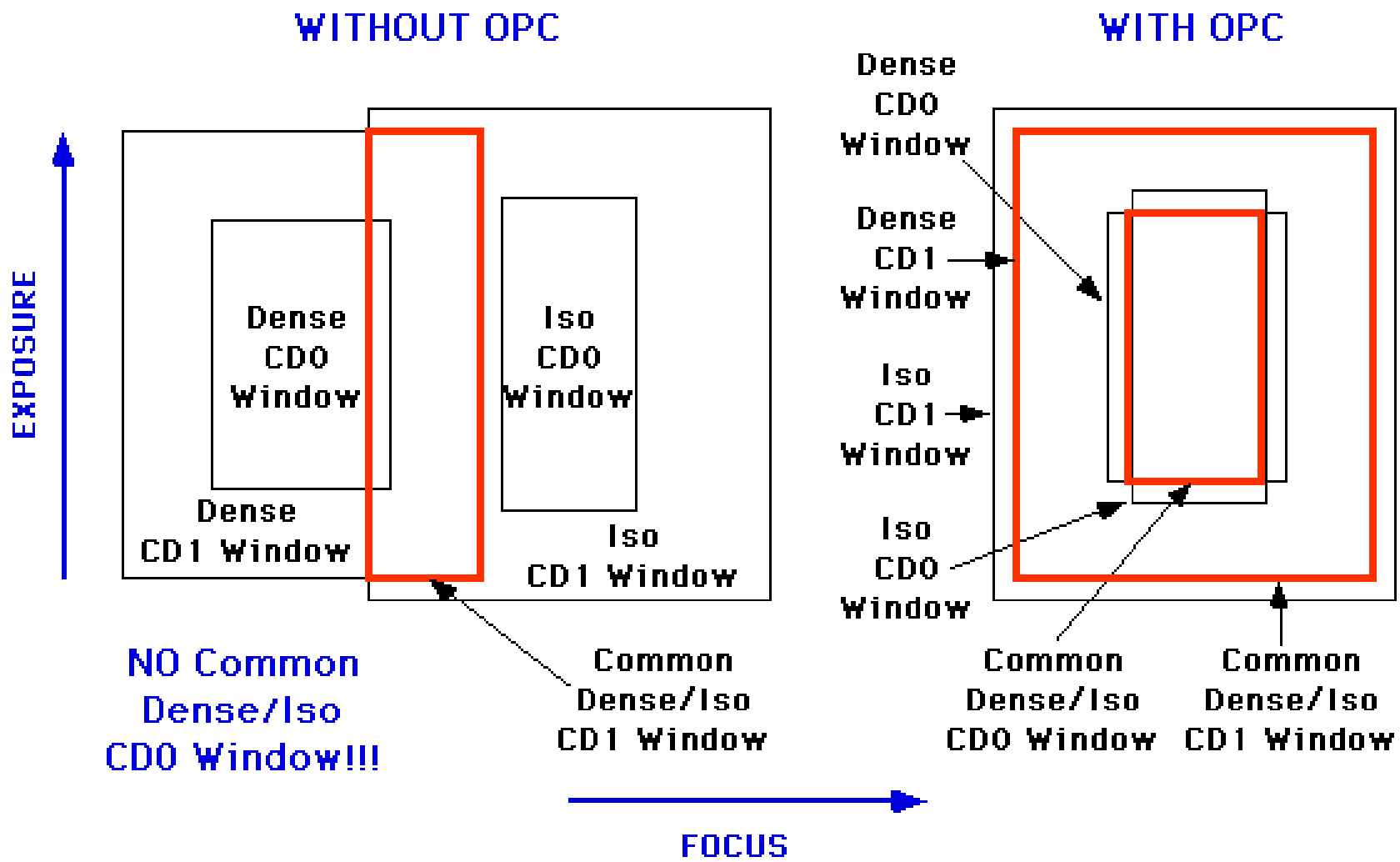
- **Both transistors built on insulating substrate**
  - Allows for tight compaction of design area
  - Some of the parasitic capacitances seen in bulk CMOS disappear
  - Wafer cost is high (IBM produces SOI, Intel doesn't)



Accounting for VDSM Effects

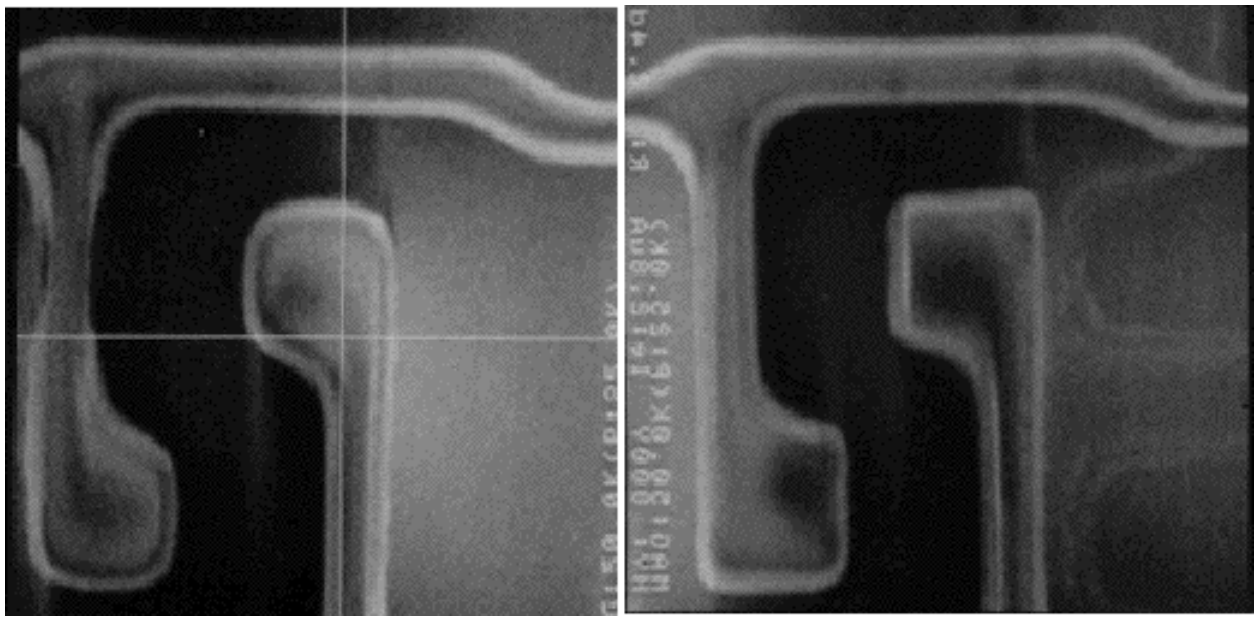
- **VDSM = Very Deep Sub Micron**
  - Effects significant below 0.25 μm (0.18 μm, 130 nm, 90 nm, 65 nm, 45 nm)
- **Compensation made at the mask level**
  - OPC – Optical Proximity Correction
  - Occurs when different mask layers don't align properly
  - Test structures are used to characterize the process
  - Ability to adapt depends on the consistency of the error from process run to process run

Accounting for VDSM Effects: OPC



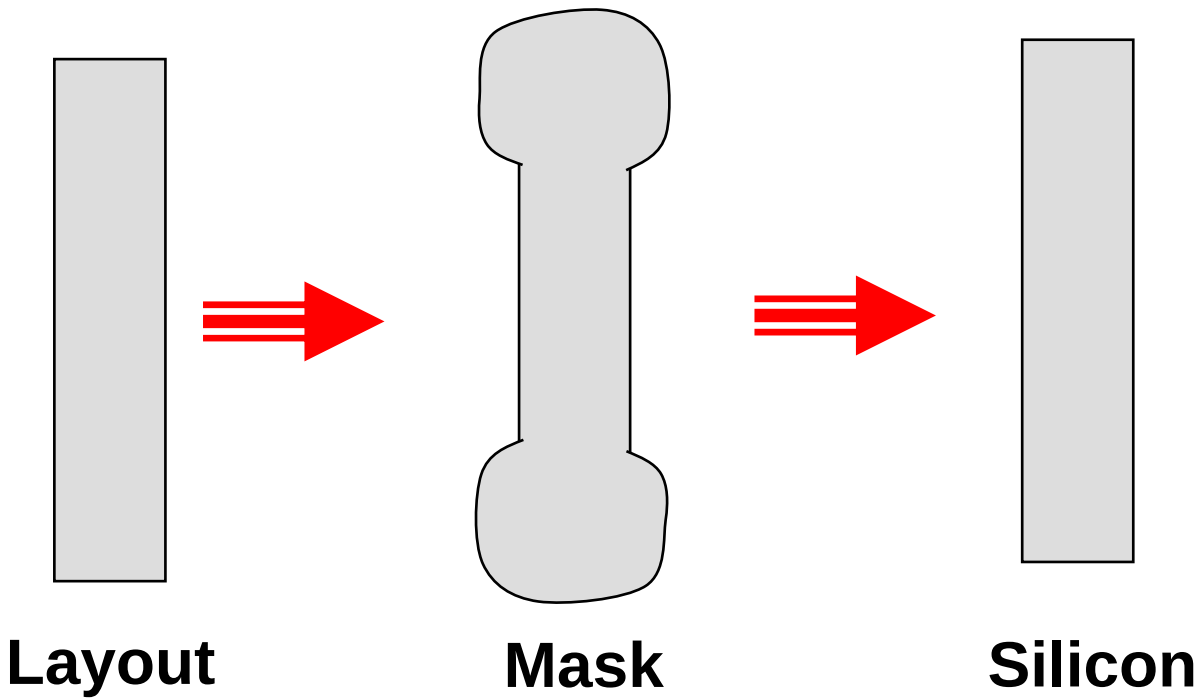
Accounting for VDSM Effects: Example

- **Example of 2D OPC effects: rounded edges, narrowed lines**



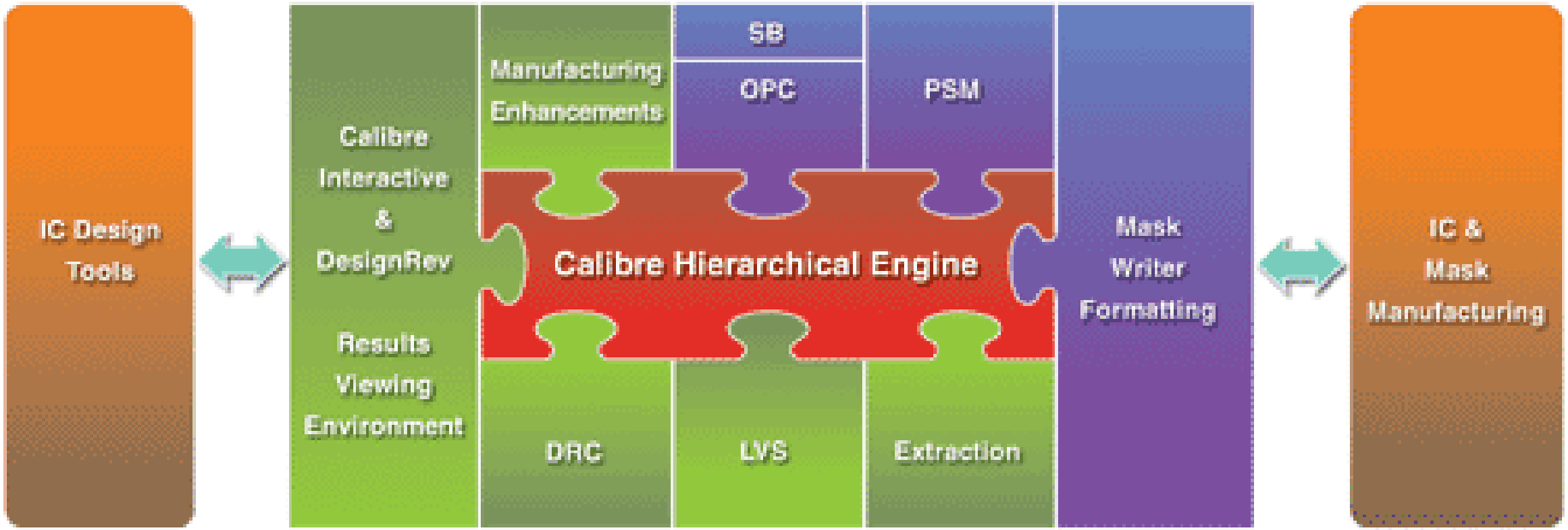
Uncorrected **Corrected**

Compensating for VDSM Effects: Masks



Compensating for VDSM Effects: CAD

- **Flow to compensate is transparent to layout designer**
- **Layout design proceeds as normal**



Mentor Graphics Flow

http://www.mentor.com/calibre/datasheets/opc/html/

References

- **“Design of VLSI Systems”. A web based course located at: http://turquoise.wpi.edu/webcourse/**
- **“Simplified Rule Generation for Automated Rules-Based Optical Enhancement”, Otto et. al. On web at: http://www.jetlink.net/~ootto/bacus95/BACUS95Index.html**
- **Mark Anders and Jim Schantz of Intel Corporation**
- **Jan Rabaey, Lecture notes from his book “Digital Integrated Circuits, A Design Perspective”**

Next Time: AC Characteristics

- **CMOS Inverters**
  - AC Characteristics: Designing for speed
- **Combinational MOS Logic**