# EEC 118 Lecture #4: CMOS Inverters

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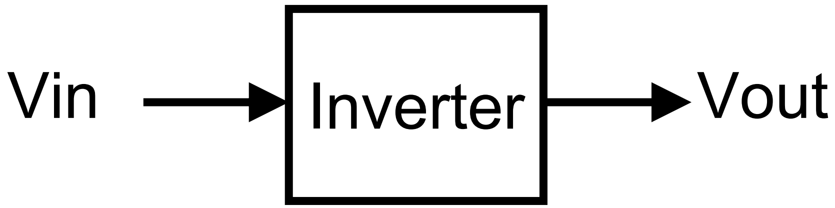
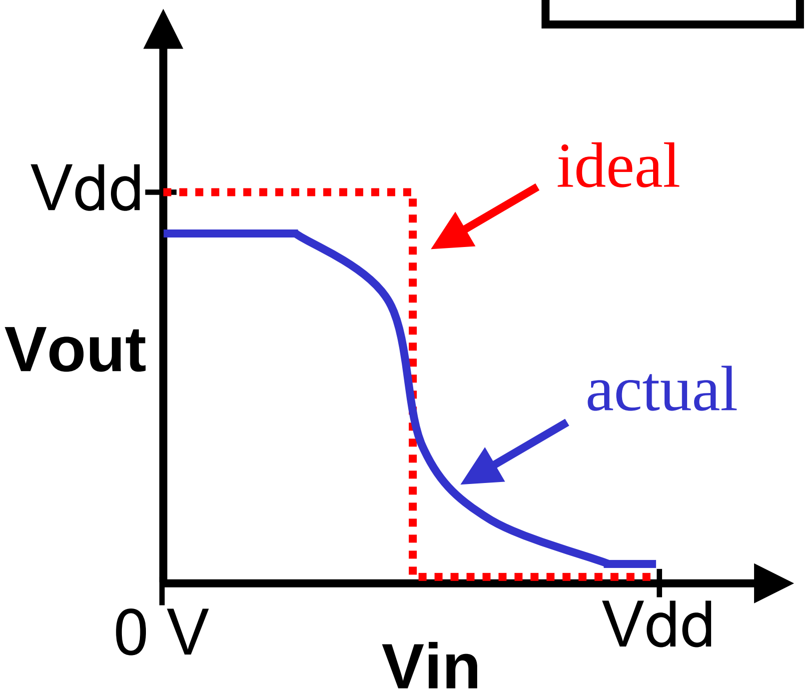
# Outline

- **Review: Inverter Transfer Characteristics**
- **Lecture 3: Noise Margins, Rise & Fall Times, Inverter Delay**
- **CMOS Inverters: Rabaey 1.3.2, 5 (Kang & Leblebici, 5.1-5.3 and 6.1-6.2)**

# Review: Inverter Voltage Transfer Curve

Voltage transfer curve (VTC): plot of output voltage Vout vs. input voltage Vin

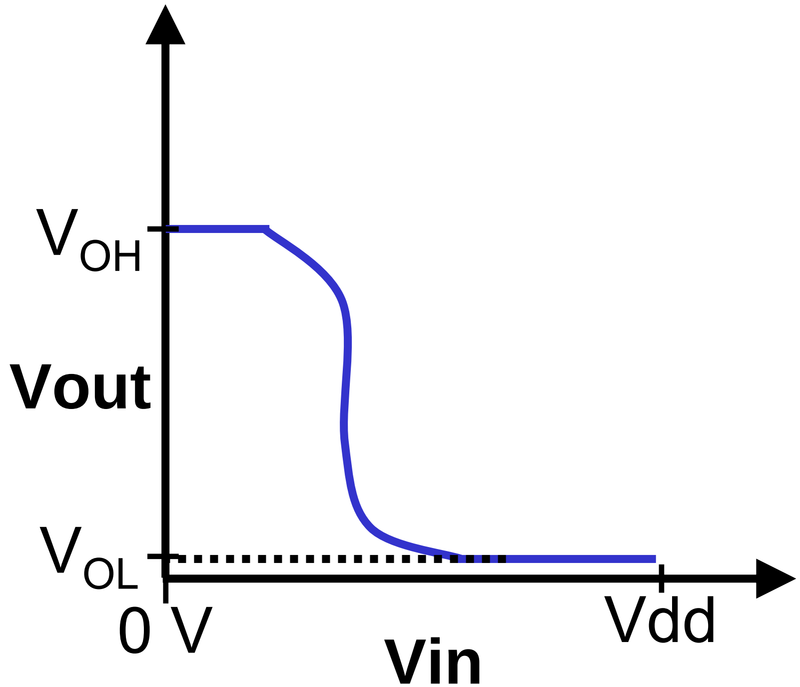



**<u>Ideal digital inverter:</u>**

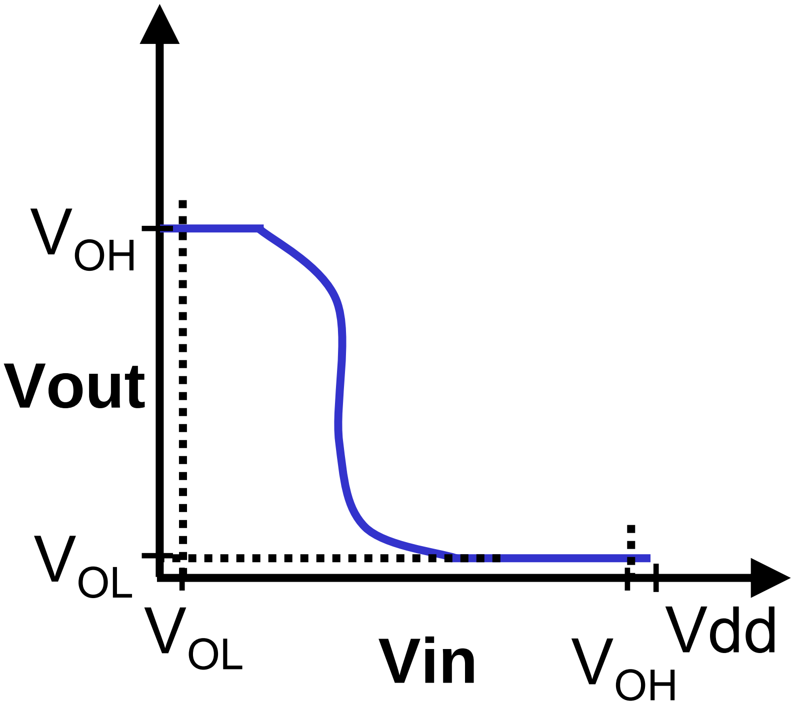
- –When Vin=0, Vout=Vdd
- –When Vin=Vdd, Vout=0
- –Sharp transition region

# Review: Actual Inverter Output Levels



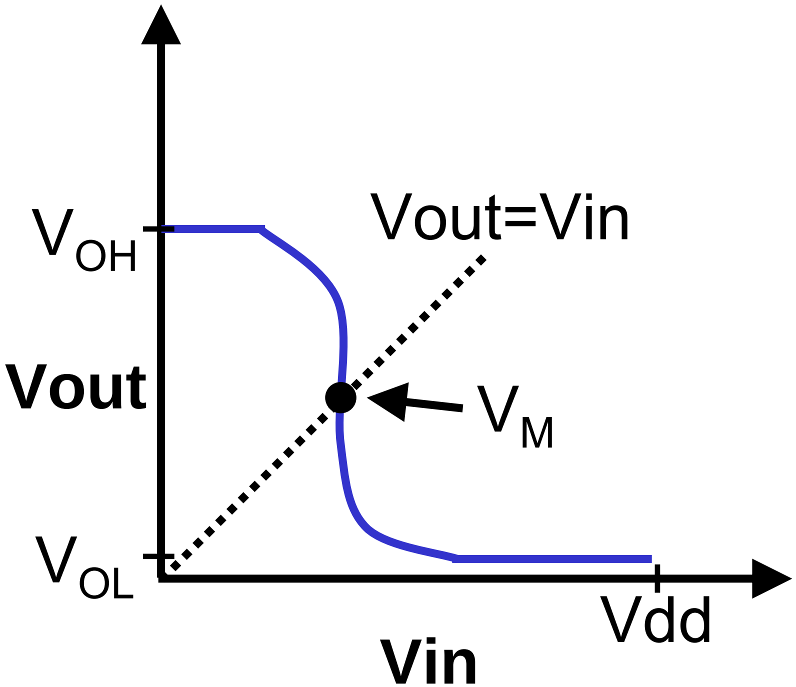

- $V_{OH}$ and $V_{OL}$ represent the "high" and "low" output voltages of the inverter
- $V_{OH}$ = output voltage when Vin = '0' (V Output High)
- $V_{OL}$ = output voltage when Vin = '1' (V Output Low)
- Ideally,
  - $V_{OH}$ = Vdd
  - $V_{OL}$ = 0 V

# Review: VOL and VOH




- **In transfer function terms:**
  - $V_{OL} = f(V_{OH})$
  - $V_{OH} = f(V_{OL})$
  - f = inverter transfer function
- **Difference ($V_{OH}$-$V_{OL}$) is the *voltage swing* of the gate**
  - *Full-swing logic* swings from ground to Vdd
  - Other families with smaller swings

# Review: Inverter Switching Threshold




**Inverter switching threshold:**

- Point where voltage transfer curve intersects line Vout=Vin
- Represents the point at which the inverter switches state
- Normally, $V_M \approx$ Vdd/2
- Sometimes other thresholds desirable

# VTC Mathematical Definitions

- **$V_{OH}$ is the output high level of an inverter**

  $V_{OH} = VTC(V_{OL})$

- **$V_{OL}$ is the output low level of an inverter**

  $V_{OL} = VTC(V_{OH})$

- **$V_M$ is the switching threshold**

  $V_M = V_{IN} = V_{OUT}$

- **$V_{IH}$ is the lowest input voltage for which the output will be ≥ the input (worst case '1')**

  $dVTC(V_{IH})/dV_{IH} = -1$

- **$V_{IL}$ is the highest input voltage for which the output will be ≤ the input (worst case '0')**

  $dVTC(V_{IL})/dV_{IL} = -1$

# Noise Margin and Delay Definitions

- **$NM_L$ is the difference between the highest acceptable '0' and the lowest possible '0'**

$$NM_L = V_{IL} - V_{OL}$$

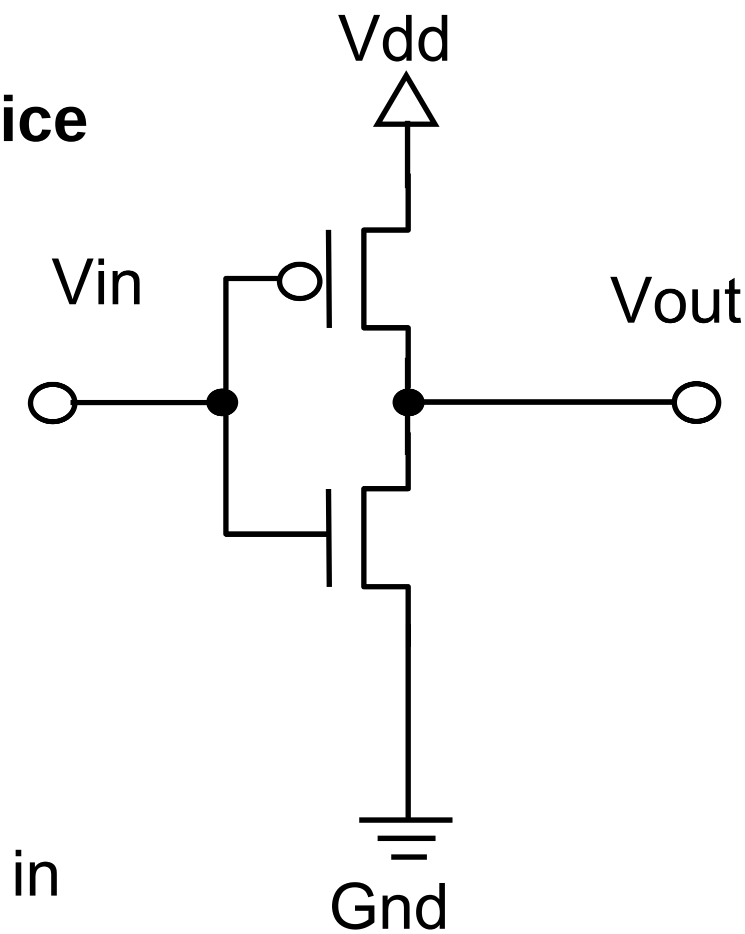
- **$NM_H$ is the difference between the lowest acceptable '1' and the highest possible '1'**

$$NM_H = V_{OH} - V_{IH}$$

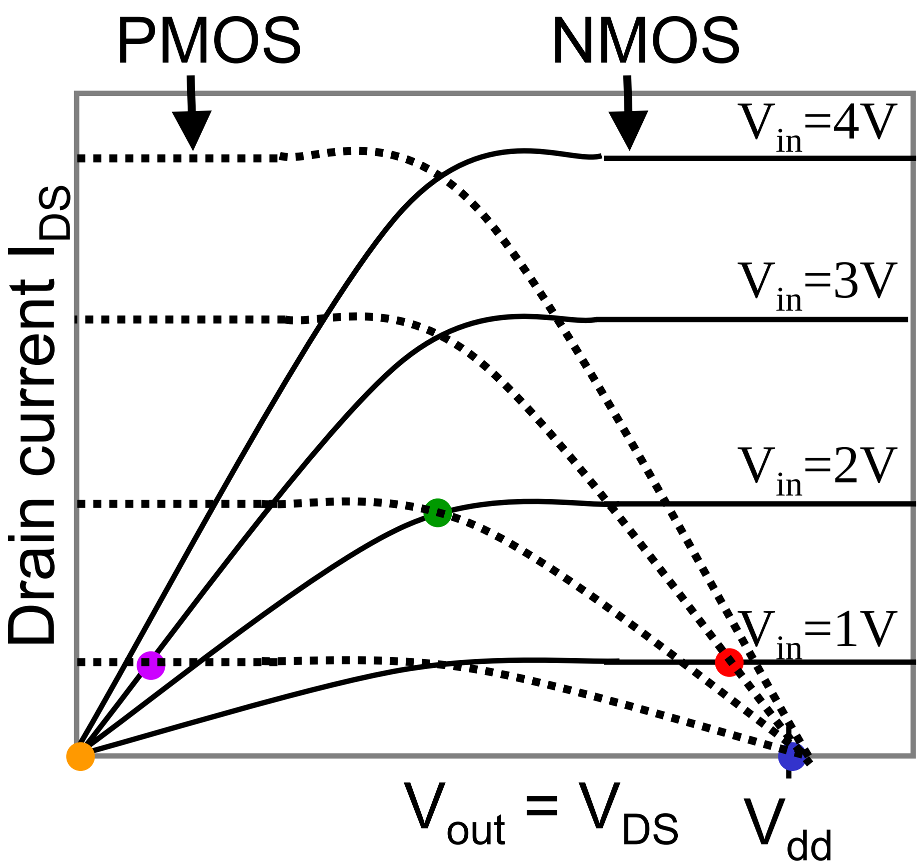
- **$t_{PHL}$ is the propagation delay from the 50% point of the input to the output when the output goes from high to low**
- **$t_{PLH}$ is the propagation delay from the 50% point of the input to the output when the output goes from low to high**
- **$t_P$ is the average propagation delay**
- **$t_R$ is the rise time (usually 10% to 90%)**
- **$t_F$ is the fall time (usually 90% to 10%)**

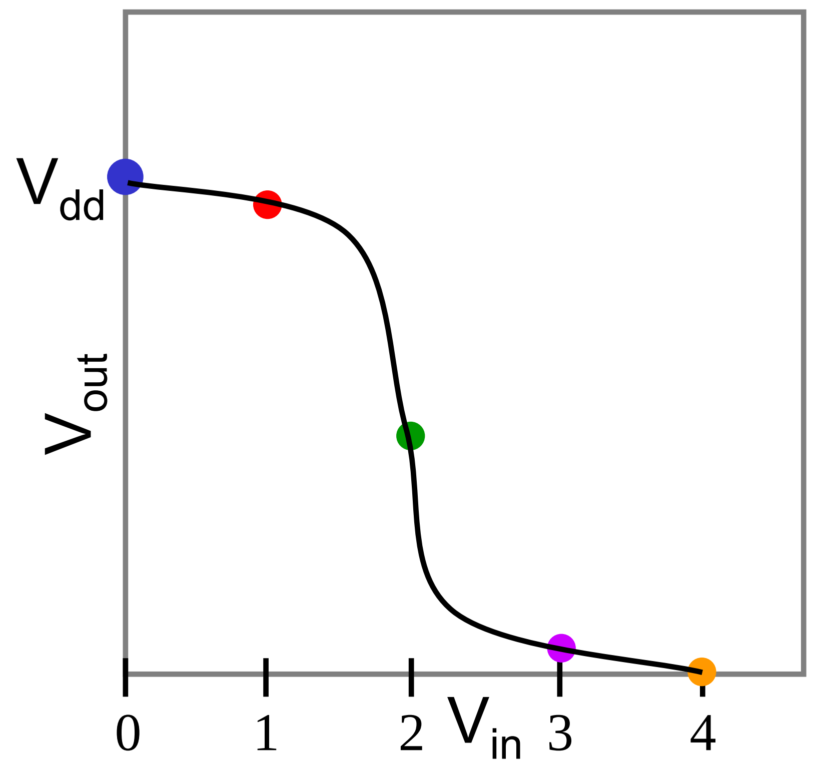
# CMOS Inverter

- **Complementary NMOS and PMOS devices**
- **In steady-state, only one device is on (no static power consumption)**
- **Vin=1: NMOS on, PMOS off**
  - Vout = $V_{OL}$ = 0
- **Vin=0: PMOS on, NMOS off**
  - Vout = $V_{OH}$ = Vdd
- **Ideal $V_{OL}$ and $V_{OH}$!**
- Ratioless logic: output is independent of transistor sizes in steady-state



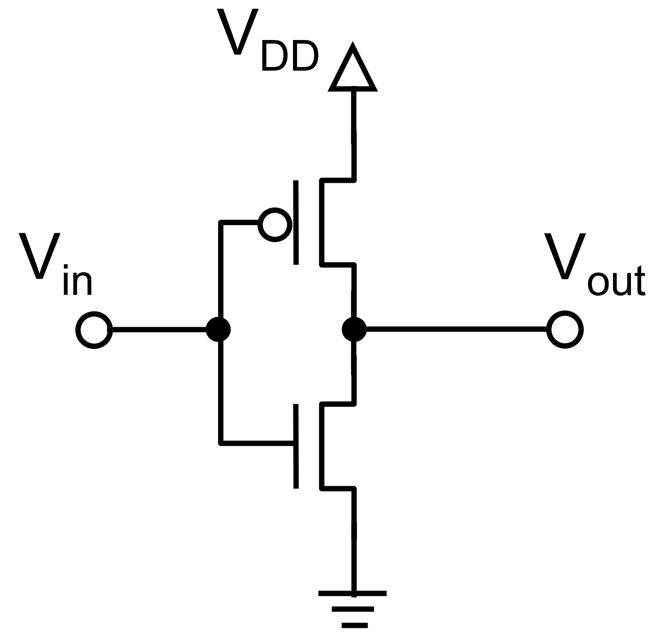
# CMOS Inverter: VTC



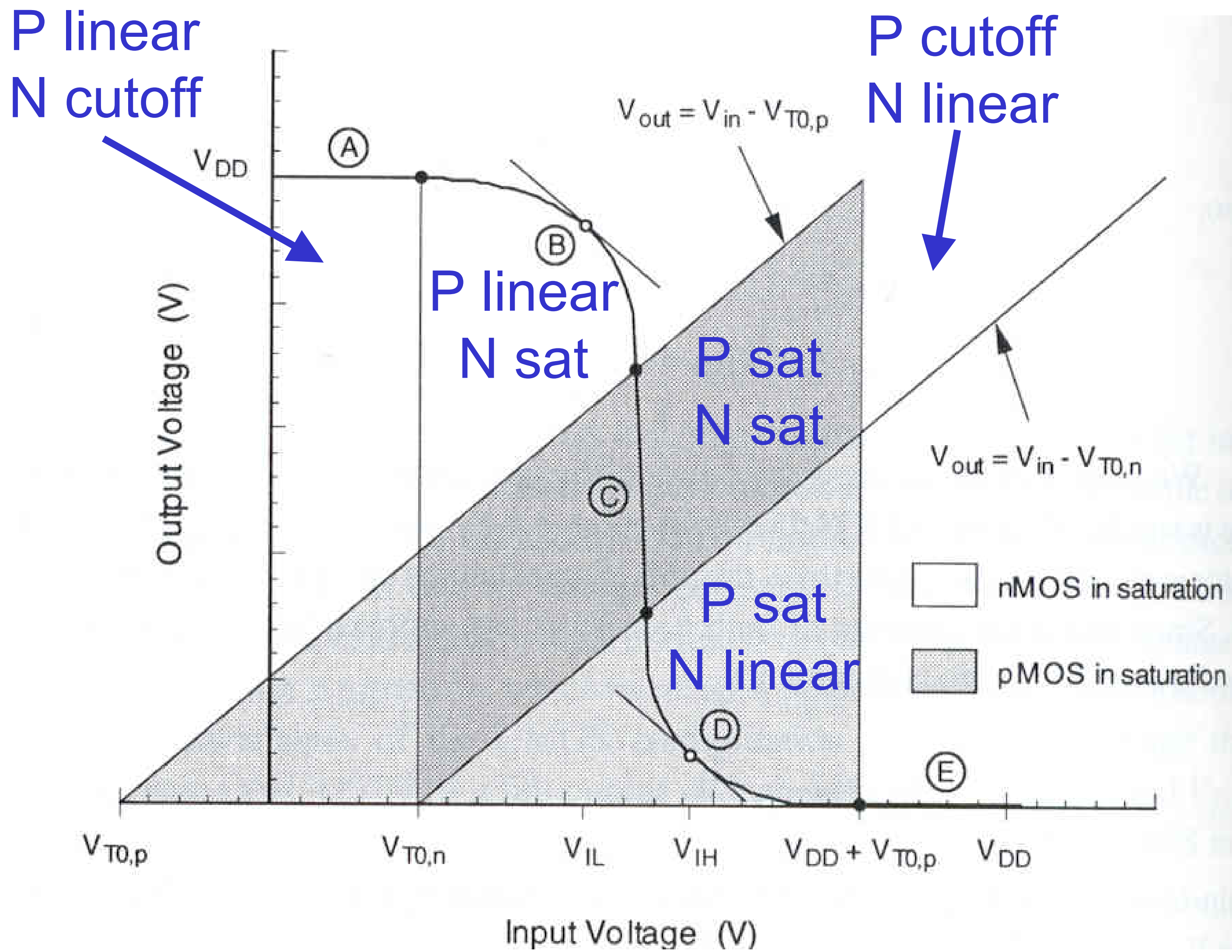

- Output goes completely to Vdd and Gnd
- Sharp transition region

# CMOS Inverter Operation

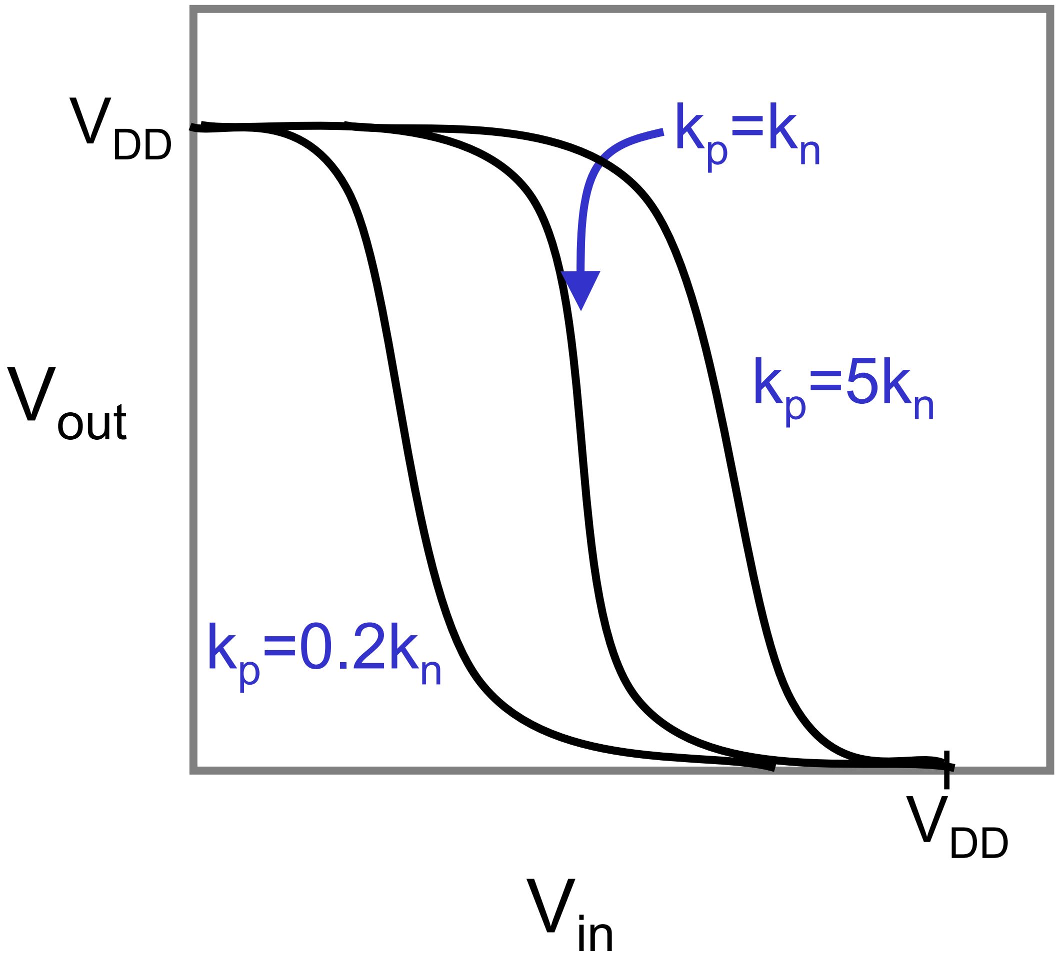



- **NMOS transistor:**
  - Cutoff if $V_{in} < V_{TN}$
  - Linear if $V_{out} < V_{in} - V_{TN}$
  - Saturated if $V_{out} > V_{in} - V_{TN}$
- **PMOS transistor**
  - Cutoff if $(V_{in}-V_{DD}) < V_{TP} \rightarrow V_{in} < V_{DD}+V_{TP}$
  - Linear if $(V_{out}-V_{DD})>V_{in}-V_{DD}-V_{TP} \rightarrow V_{out}>V_{in} - V_{TP}$
  - Sat. if $(V_{out}-V_{DD})<V_{in}-V_{DD}-V_{TP} \rightarrow V_{out} < V_{in}-V_{TP}$

# CMOS Inverter VTC: Device Operation



# CMOS Inverter VTC: Device Sizing




- Increase W of PMOS
  - $k_p$ increases
  - VTC moves to right
- Increase W of NMOS
  - $k_n$ increases
  - VTC moves to left
- For $V_M = V_{DD}/2$
  - $k_n = k_p$
  - $2W_n \approx W_p$

# Effects of $V_M$ adjustment

- **Result from changing $k_p/k_n$ ratio:**
  - Inverter threshold $V_M \neq V_{DD}/2$
  - Rise and fall delays unequal
  - Noise margins not equal
- **Reasons for changing inverter threshold**
  - Want a faster delay for one type of transition (rise/fall)
  - Remove noise from input signal: increase one noise margin at expense of the other
  - Interfacing other types of logic (with different swings)

# CMOS Inverter: $V_{IL}$ Calculation

- **KCL (NMOS saturation, PMOS linear):**

$$\frac{k_n}{2}\left(V_{GS,n}-V_{T0,n}\right)^2=\frac{k_p}{2}\left[2\left(V_{GS,p}-V_{T0,p}\right)V_{DS,p}-V_{DS,p}{}^2\right]$$

$$\frac{k_n}{2}\left(V_{in}-V_{T0,n}\right)^2=\frac{k_p}{2}\left[2\left(V_{in}-V_{DD}-V_{T0,p}\right)\left(V_{out}-V_{DD}\right)-\left(V_{out}-V_{DD}\right)^2\right]$$

- **Differentiate and set dVout/dVin to –1**

$$k_n\left(V_{in}-V_{T0,n}\right)=k_p\left[\left(V_{in}-V_{DD}-V_{T0,p}\right)\frac{dV_{out}}{dV_{in}}+\left(V_{out}-V_{DD}\right)-\left(V_{out}-V_{DD}\right)\frac{dV_{out}}{dV_{in}}\right]$$

$$k_n\left(V_{IL}-V_{T0,n}\right)=k_p\left(2V_{out}-V_{IL}+V_{T0,p}-V_{DD}\right)$$

$$\boxed{V_{IL}=\frac{2V_{out}+V_{T0,p}-V_{DD}+k_RV_{T0,n}}{1+k_R}\qquad k_R=\frac{k_n}{k_p}}$$

- **Solve simultaneously with KCL to find $V_{IL}$**

# CMOS Inverter: $V_{IH}$ Calculation

- **KCL:** $\frac{k_n}{2}\left[2\left(V_{GS,n}-V_{T0,n}\right)V_{DS,n}-V_{DS,n}{}^2\right]=\frac{k_p}{2}\left(V_{GS,p}-V_{T0,p}\right)^2$

$$\frac{k_n}{2}\left[2\left(V_{in}-V_{T0,n}\right)V_{out}-V_{out}{}^2\right]=\frac{k_p}{2}\left(V_{in}-V_{DD}-V_{T0,p}\right)^2$$

- **Differentiate and set dVout/dVin to –1**

$$k_n\left[\left(V_{in}-V_{T0,n}\right)\frac{dV_{out}}{dV_{in}}+V_{out}-V_{out}\frac{dV_{out}}{dV_{in}}\right]=k_p\left(V_{in}-V_{DD}-V_{T0,p}\right)$$

$$k_n\left(2V_{out}-V_{IH}+V_{T0,p}\right)=k_p\left(V_{IH}-V_{DD}-V_{T0,p}\right)$$

$$\boxed{V_{IH}=\frac{V_{DD}+V_{T0,p}+k_R\left(2V_{out}+V_{T0,n}\right)}{1+k_R}\qquad k_R=\frac{k_n}{k_p}}$$

- **Solve simultaneously with KCL to find $V_{IH}$**

# CMOS Inverter: $V_M$ Calculation

- **KCL (NMOS & PMOS saturated):**

$$\frac{k_n}{2}\left(V_{GS,n} - V_{T0,n}\right)^2 = \frac{k_p}{2}\left(V_{GS,p} - V_{T0,p}\right)^2$$

$$\frac{k_n}{2}\left(V_{in} - V_{T0,n}\right)^2 = \frac{k_p}{2}\left(V_{in} - V_{DD} - V_{T0,p}\right)^2$$

- **Solve for $V_M = V_{in} = V_{out}$**

$$V_M = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}}\left(V_{DD} + V_{T0,p}\right)}{1 + \sqrt{\frac{1}{k_R}}} \qquad k_R = \frac{k_n}{k_p}$$

# CMOS Inverter: Achieving Ideal $V_M$

$$V_{TH} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}}\left(V_{DD} + V_{T0,p}\right)}{1 + \sqrt{\frac{1}{k_R}}} \qquad k_R = \frac{k_n}{k_p}$$

- **Ideally, $V_M = V_{DD}/2$**

$$k_{R,ideal} = \left( \frac{V_{DD}/2 + V_{T0,p}}{V_{DD}/2 + V_{T0,n}} \right)^2$$

- **Assuming $V_{T0,n} = V_{T0,p}$,** $k_{R,ideal} = 1$

$$\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = \frac{\mu_n}{\mu_p} \approx 2.5$$

# CMOS Inverter: $V_{IL}$ and $V_{IH}$ for Ideal $V_M$

- **Assuming $V_{T0,n}$=-$V_{T0,p}$, and $k_R$ = 1,**

$$V_{IL} = \frac{1}{8}\left(3V_{DD} + 2\left|V_{T0}\right|\right)$$

$$V_{IH} = \frac{1}{8}\left(5V_{DD} - 2\left|V_{T0}\right|\right)$$

$$V_{IL} + V_{IH} = V_{DD}$$

$$NM_L = V_{IL} - V_{OL} = V_{IL}$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH} = V_{IL}$$

# Next Time: AC Characteristics & Fabrication

- **MOS Fabrication**
- **CMOS Inverters**
  - AC Characteristics: Designing for speed