## EEC 118 Lecture #3: Inverters

Rajeevan Amirtharajah University of California, Davis Jeff Parkhurst Intel Corporation

## Outline

- Review: MOSFET Regimes of Operation
- Lecture 2: Scaling, Parasitic Capacitances
- Inverter Operation: Rabaey 1.3.2, 5 (Kang & Leblebici, 5.1-5.3 and 6.1-6.2)

#### **Review: MOS Transistor Structure**

- Important transistor physical characteristics
  - Channel length  $L = L_D 2x_d$  (K&L L = Lgate 2L<sub>D</sub>)
  - Channel width W



Saturation: 
$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

Linear (Triode, Ohmic):

$$I_D = \mu C_{ox} \frac{W}{L} \left( \left( V_{GS} - V_T \right) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

Cutoff:  $I_D \approx 0$ 

#### "Classical" MOSFET model, will discuss deep submicron modifications as necessary (Rabaey, Eqs. 3.25, 3.29)

#### **MOS Transistor Symbols**



## **Note on MOS Transistor Symbols**

- All symbols appear in literature
  - Symbols with arrows are conventional in analog papers
  - PMOS with a bubble on the gate is conventional in digital circuits papers
- Sometimes bulk terminal is ignored implicitly connected to source or appropriate supply rail:



 Unlike physical bipolar devices, source and drain are usually symmetric

#### **Inverter Operation**

Inverter is simplest digital logic gate (1 input, 1 output)



- Many different circuit styles possible
  - Resistive-load
  - NMOS and Pseudo-NMOS
  - CMOS
- Important static and dynamic characteristics
  - Speed (delay through the gate)
  - Power consumption
  - Robustness (tolerance to noise)
  - Area and process cost

#### Inverter Model: Voltage Transfer Curve

Voltage transfer curve (VTC): plot of output voltage Vout vs. input voltage Vin





- V<sub>OH</sub> and V<sub>OL</sub> represent the "high" and "low" output voltages of the inverter
- V<sub>OH</sub> = output voltage when Vin = '0' (<u>V O</u>utput <u>H</u>igh)
- V<sub>OL</sub> = output voltage when Vin = '1' (<u>V O</u>utput <u>L</u>ow)
- Ideally,

$$-V_{OH} = Vdd$$

$$-V_{OL} = 0 V$$

## VOL and VOH



#### In transfer function terms:

$$- V_{OL} = f(V_{OH})$$

$$-V_{OH} = f(V_{OL})$$

- f = inverter transfer function
- Difference (V<sub>OH</sub>-V<sub>OL</sub>) is the voltage swing of the gate
  - Full-swing logic swings from ground to Vdd
  - Other families with smaller swings

## **Inverter Switching Threshold**



# Inverter switching threshold:

- Point where voltage transfer curve intersects line Vout=Vin
- Represents the point at which the inverter switches state
- Normally,  $V_M \approx Vdd/2$
- Sometimes other thresholds desirable

$$(K\&L V_{TH} = V_M)$$

## **Noise Margins**



- V<sub>IL</sub> and V<sub>IH</sub> measure effect of input voltage on inverter output
- V<sub>IL</sub> = largest input voltage recognized as logic '0'
- V<sub>IH</sub> = smallest input voltage recognized as logic '1'
- Defined as point on VTC
  where slope = -1

#### **Noise Margins and Robustness**



Ideally, noise margin should be as large as possible • Noise margin is a measure of the *robustness* of an inverter

$$- N_{ML} = V_{IL} - V_{OL}$$

$$-$$
 N<sub>MH</sub>  $=$  V<sub>OH</sub>  $-$  V<sub>IH</sub>

- Models a chain of inverters. Example:
  - First inverter output is  $V_{OH}$
  - Second inverter recognizes
    input > V<sub>IH</sub> as logic '1'
  - Difference V<sub>OH</sub>-V<sub>IH</sub> is "safety zone" for noise

#### **Noise Margin Motivation**

- Why are  $V_{IL}$ ,  $V_{IH}$  defined as unity-gain point on VTC curve?
  - Assume there is noise on input voltage V<sub>in</sub>

$$V_{out} = f\left(V_{in} + V_{noise}\right)$$

- First-order Taylor series approximation:

$$V_{out} = f(V_{in}) + \frac{dV_{out}}{dV_{in}} V_{noise}$$

- If gain  $(dV_{out}/dV_{in}) > 1$ , noise will be amplified.
- If gain < 1, noise is filtered. Therefore V<sub>IL</sub>, V<sub>IH</sub> define regions where gain < 1

#### **Inverter Time Response**



 Propagation delay measured from 50% point of Vin to 50% point of Vout

• 
$$t_{phl} = t_1 - t_0$$
,  $t_{plh} = t_3 - t_2$ ,  $t_p = \frac{1}{2}(t_{phl} + t_{plh})$ 

### **Rise and Fall Time**



- Fall time: measured from 90% point to 10% point  $t_F = t_1 t_0$
- Rise time: measured from 10% point to 90% point  $t_R = t_3 t_2$
- Alternately, can define 20%-80% rise/fall time

#### **Ring Oscillator**

- *Ring oscillator circuit*: standard method of comparing delay from one process to another
- Odd-number n of inverters connected in chain: oscillates with period T (usually n >> 5)



18

#### **Resistive Load Inverter**



• Resistor pulls up to Vdd ( $V_{OH}$ ), NMOS pulls down ( $V_{OL}$ )

#### **NMOS Inverter**



#### • Depletion NMOS always on, sourcing static current

#### **Inverter as Amplifier**



- For  $V_{in}$  between  $V_{IL}$  and  $V_{IH}$ , inverter gain > 1
- Acts as a linear amplifier (often very high gain)
- Logic levels '0' and '1' correspond to saturating amplifier output (output is pegged to high or low supply)
- Resistive load inverter same circuit as <u>common</u> <u>source amplifier</u>

#### **Next Topic: CMOS Inverters**

- CMOS Inverters
  - DC Characteristics: Sizing
  - AC Characteristics: Designing for speed