# EEC 118 Lecture #2: MOSFET Structure and Basic Operation

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- Lab 1 this week, report due next week
- Bring your breadboards to lab!
- HW 1 due this Friday at 4 PM in box, Kemper 2131
- Instructor office hours this week: Wednesday 11 AM -12 PM
- TA Office Hours: Thursdays 3:30-5 PM, Kemper 2157/2161

# Outline

- Finish Lecture 1 Slides
- Switch Example
- MOSFET Structure
- MOSFET Regimes of Operation
- Scaling
- Parasitic Capacitances

- Rabaey Ch. 3 (Kang & Leblebici Ch. 3)
- Two transistor types (analogous to bipolar NPN, PNP)
  - NMOS: p-type substrate, n<sup>+</sup> source/drain, electrons are charge carriers
  - PMOS: n-type substrate, p<sup>+</sup> source/drain, holes are charge carriers



# **MOS Transistor Symbols**



# **Note on MOS Transistor Symbols**

- All symbols appear in literature
  - Symbols with arrows are conventional in analog papers
  - PMOS with a bubble on the gate is conventional in digital circuits papers
- Sometimes bulk terminal is ignored implicitly connected to supply:



 Unlike physical bipolar devices, source and drain are usually symmetric

### **MOS Transistor Structure**

- Important transistor physical characteristics
  - Channel length  $L = L_D 2x_d$  (K&L L = Lgate 2L<sub>D</sub>)
  - Channel width W



# **NMOS Transistor I-V Characteristics I**



• I-V curve vaguely resembles bipolar transistor curves

- Quantitatively very different
- Turn-on voltage called <u>Threshold Voltage</u>  $V_T$

### **NMOS Transistor I-V Characteristics II**



Drain current varies quadratically with gate-source voltage V<sub>GS</sub> (in Saturation)

### **MOS Transistor Operation: Cutoff**

- Simple case:  $V_D = V_S = V_B = 0$ 
  - Operates as MOS capacitor (Cg = gate to channel)
  - Transistor in cutoff region
- When  $V_{GS} < V_{T0}$ , depletion region forms
  - No carriers in channel to connect S and D (Cutoff)



# **MOS Transistor Operation: Inversion**

- When  $V_{GS} > V_{T0}$ , inversion layer forms
- Source and drain connected by conducting ntype layer (for NMOS)
  - Conducting p-type layer in PMOS



# **Threshold Voltage Components**

- Four physical components of the threshold voltage
- 1. Work function difference between gate and channel (depends on metal or polysilicon gate):  $\Phi_{GC}$
- 2. Gate voltage to invert surface potential:  $-2\Phi_F$
- 3. Gate voltage to offset depletion region charge:  $Q_B/C_{ox}$
- 4. Gate voltage to offset fixed charges in the gate oxide and oxide-channel interface:  $Q_{ox}/C_{ox}$

$$C_{ox} = \frac{\mathcal{E}_{ox}}{t_{ox}}$$

: gate oxide capacitance per unit area

• If V<sub>SB</sub> = 0 (no substrate bias):

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad (K\&L \ 3.20)$$

• If  $V_{SB} \neq 0$  (non-zero substrate bias)

$$V_{T} = V_{T0} + \gamma \left( \sqrt{\left| -2\phi_{F} + V_{SB} \right|} - \sqrt{\left| 2\phi_{F} \right|} \right) \quad (3.19)$$

• Body effect (substrate-bias) coefficient:

$$\gamma = \frac{\sqrt{2qN_A \mathcal{E}_{Si}}}{C_{ox}}$$
(K&L 3.24)

Threshold voltage increases as V<sub>SB</sub> increases!

# **Threshold Voltage (NMOS vs. PMOS)**

	NMOS	PMOS
Substrate Fermi potential	φ <sub>F</sub> < 0	φ <sub>F</sub> > 0
Depletion charge density	Q <sub>B</sub> < 0	Q <sub>B</sub> > 0
Substrate bias coefficient	γ <b>&gt; 0</b>	γ <b>&lt; 0</b>
Substrate bias voltage	V <sub>SB</sub> > 0	V <sub>SB</sub> < 0

# **Body Effect**

- Body effect: Source-bulk voltage V<sub>SB</sub> affects threshold voltage of transistor
  - Body normally connected to ground for NMOS, Vdd (Vcc) for PMOS
  - Raising source voltage increases  $V_{T}$  of transistor
  - Implications on circuit design: series stacks of devices



# **MOS Transistor Regions of Operation**

- Three main regions of operation
- <u>Cutoff</u>:  $V_{GS} < V_T$ No inversion layer formed, drain and source are isolated by depleted channel.  $I_{DS} \approx 0$
- <u>Linear (Triode, Ohmic)</u>:  $V_{GS} > V_T$ ,  $V_{DS} < V_{GS} V_T$ Inversion layer connects drain and source. Current is almost linear with  $V_{DS}$  (like a resistor)
- <u>Saturation</u>: V<sub>GS</sub> > V<sub>T</sub>, V<sub>DS</sub> ≥ V<sub>GS</sub>-V<sub>T</sub>
  Channel is "pinched-off". Current saturates (becomes independent of V<sub>DS</sub>, to first order).

Saturation: 
$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

Linear (Triode, Ohmic):

$$I_D = \mu C_{ox} \frac{W}{L} \left( \left( V_{GS} - V_T \right) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

Cutoff:  $I_D \approx 0$ 

#### "Classical" MOSFET model, will discuss deep submicron modifications as necessary (Rabaey, Eqs. 3.25, 3.29)

# **Cutoff Region**



- For NMOS:  $V_{GS} < V_{TN}$
- For PMOS:  $V_{GS} > V_{TP}$
- Depletion region no inversion
- Current between drain and source is 0
  - Actually there is always some leakage (subthreshold) current

# Linear Region

- When V<sub>GS</sub>>V<sub>T</sub>, an inversion layer forms between drain and source
- Current I<sub>DS</sub> flows from drain to source (electrons travel from source to drain)
- Depth of channel depends on V between gate and channel
  - Drain end narrower due to larger drain voltage
  - Drain end depth reduces as  $V_{\text{DS}}$  is increased



# **Linear Region I/V Equation Derivation**



- Gradual Channel Approximation:
  - Assume dominant electric field in y-direction
  - Current is constant along channel

#### Integrate differential voltage drop dV<sub>c</sub> = I<sub>D</sub>dR along y

• Valid for continuous channel from Source to Drain

$$I_{D} = \mu_{n} C_{ox} \frac{W}{L} \left[ \left( V_{GS} - V_{T} \right) V_{DS} - \frac{1}{2} V_{DS}^{2} \right]$$

Device transconductance:

$$k_n = \mu_n C_{ox} \frac{W}{L}$$

Process transconductance: 
$$k_n' = \mu_n C_{ox}$$
  
$$I_D = k_n' \frac{W}{L} \left[ \left( V_{GS} - V_T \right) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

# **Saturation Region**

• When  $V_{DS} = V_{GS} - V_{T}$ :

- No longer voltage drop of  $V_T$  from gate to substrate at drain Channel is "pinched off"
- If  $V_{DS}$  is further increased, no increase in current  $I_{DS}$ 
  - As V<sub>DS</sub> increased, pinch-off point moves closer to source
  - Channel between that point and drain is depleted
  - High electric field in depleted region accelerates electrons towards drain  $V_g > V_{T0}$



# **Saturation I/V Equation**

- As drain voltage increases, channel remains pinched off
  - Channel voltage remains constant
  - Current saturates (no increase with increasing  $V_{DS}$ )
- To get saturation current, use linear equation with  $V_{DS} = V_{GS} V_T$

$$I_{D} = \frac{1}{2} \mu_{n} C_{ox} \frac{W}{L} (V_{GS} - V_{TN})^{2}$$

- I/V curve for ideal MOS device
- V<sub>GS3</sub>> V<sub>GS2</sub> > V<sub>GS1</sub>



Drain voltage V<sub>DS</sub>

- In saturation, pinch-off point moves
  - As V<sub>DS</sub> is increased, pinch-off point moves closer to source
  - Effective channel length becomes shorter
  - Current increases due to shorter channel

$$\dot{L} = L - \Delta L$$

$$I_{D} = \frac{1}{2} \mu_{n} C_{ox} \frac{W}{L} (V_{GS} - V_{TN})^{2} (1 + \lambda V_{DS})$$

 $\lambda$  = channel length modulation coefficient

#### I/V curve for non-ideal NMOS device:



### **MOS I/V Equations Summary**

$$\begin{array}{ll} \textbf{Cutoff} & V_{GS} < V_{TN} \\ & V_{GS} > V_{TP} \end{array} \Longrightarrow I_D = 0 \end{array}$$

#### Linear

$$V_{GS} \ge V_{TN}, \quad V_{DS} < V_{GS} - V_{TN} \Longrightarrow I_D = \mu C_{ox} \frac{W}{L} \Big[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \Big]$$
  
$$V_{GS} \le V_{TP}, \quad V_{DS} > V_{GS} - V_{TP} \Longrightarrow I_D = \mu C_{ox} \frac{W}{L} \Big[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \Big]$$

#### **Saturation**

$$V_{GS} \ge V_{TN}, \quad V_{DS} \ge V_{GS} - V_{TN} \Longrightarrow I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$
  
$$V_{GS} \le V_{TP}, \quad V_{DS} \le V_{GS} - V_{TP}$$

Note: if  $V_{SB} \neq 0$ , need to recalculate  $V_T$  from  $V_{T0}$ 

# **A Fourth Region: Subthreshold**

Subthreshold: 
$$I_D = I_S e^{\frac{V_{GS}}{n^{kT/q}}} \left(1 - e^{-\frac{V_{DS}}{kT/q}}\right)$$

- Sometimes called "weak inversion" region
- When V<sub>GS</sub> near V<sub>T</sub>, drain current has an exponential dependence on gate to source voltage
  - Similar to a bipolar device
- Not typically used in digital circuits
  - Sometimes used in very low power digital applications
  - Often used in low power analog circuits, e.g. quartz watches

# **MOSFET Scaling Effects**

- Rabaey Section 3.5 (Kang & Leblebici Section 3.5)
- Scaling provides enormous advantages
  - Scale linear dimension (channel length) by factor S > 1
  - Better area density, yield, performance

### Two types of scaling

- Constant field scaling (full scaling)

• 
$$A' = A/S^2$$
;  $L' = L/S$ ;  $W' = W/S$ ;  $I_D' = I_D/S$ ;  $P' = P/S^2$ ;  $V_{dd}' = V_{dd}/S$ 

• Power Density P'/A' = stays the same  $_{Change}$  these two

- Constant voltage scaling

- $A' = A/S^2$ ; L' = L/S; W' = W/S;  $I_D' = I_D^*S$ ;  $P' = P^*S$ ;  $V_{dd}' = V_{dd}$
- Power Density P'/A' =  $S_{\bullet}^{3*}P$  (Reliability issue)

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This changed as well

# **Short Channel Effects**

- As geometries are scaled down
  - $-V_T$  (effective) goes lower
  - Effective channel length decreases
  - Sub-threshold Ids occurs
    - Current goes from drain to source while Vgs < Vt
  - Tox is scaled which can cause reliability problems
    - Can't handle large Vg without hot electron effects
      - Changes the Vt when carriers imbed themselves in the oxide
  - Interconnects scale
    - Electromigration and ESD become issues

# **MOSFET Capacitances**

- Rabaey Section 3.3 (Kang & Leblebici Section 3.6)
- Oxide Capacitance
  - Gate to Source overlap
  - Gate to Drain overlap
  - Gate to Channel
- Junction Capacitance
  - Source to Bulk junction
  - Drain to Bulk junction



### **Oxide Capacitances: Overlap**



- Overlap capacitances
  - Gate electrode overlaps source and drain regions
  - $x_d$  is overlap length on each side of channel
  - $L_{eff} = L_{drawn} 2x_d$  (effective channel length)

#### - Overlap capacitance:

$$C_{GSO} = C_{GDO} = C_{ox}Wx_d$$
 Assume  $x_d$  equal on both sides

# **Total Oxide Capacitance**

- Total capacitance consists of 2 components
  - Overlap capacitance
  - Channel capacitance



- Cutoff:
  - No channel connecting to source or drain

$$-C_{GS} = C_{GD} = C_{ox}Wx_{d}$$

$$- C_{GB} = C_{ox}WL_{eff}$$

- Total Gate Capacitance =  $C_G = C_{ox}WL$ 

#### • Linear mode

- Channel spans from source to drain
- Channel Capacitance split equally between S and D

$$C_{GS} = \frac{1}{2} C_{ox} W L_{eff} C_{GD} = \frac{1}{2} C_{ox} W L_{eff} C_{GB} = 0$$

– Total Gate capacitance  $C_G = C_{ox}WL$ 

Saturation regime

- Channel is pinched off: Channel Capacitance --

$$C_{GD} = WL_D C_{ox} \quad C_{GS} = \frac{2}{3}C_{ox}WL_{eff} + C_{OX}Wx_d \quad C_{GB} = 0$$
  
- Total Gate capacitance:

$$C_G = 2/3 C_{ox}WL_{eff} + 2x_dWC_{OX}$$

#### **Oxide Capacitances: Channel**



# **Junction Capacitance**



#### Reverse-biased P-N junctions! Capacitance depends on reverse-bias voltage.

### **Junction Capacitance**

For a P-N junction:
$$C_j = \frac{A}{2} \sqrt{\frac{2q\varepsilon}{V_0 - V} \frac{N_d N_a}{N_d + N_a}}$$
If V=0, cap/area = $C_{j0} = \sqrt{\frac{q\varepsilon_{Si}}{2V_0} \frac{N_d N_a}{N_d + N_a}}$ General form: $C_j = \frac{AC_{j0}}{\left(1 - \frac{V}{V_0}\right)^m}$ 

m = grading coefficient (0.5 for abrupt junctions) (0.3 for graded junctions)

- Junction with substrate
  - Bottom area = W \* L<sub>S</sub> (length of drain/source)
  - Total cap = C<sub>i</sub>
- Junction with sidewalls
  - "Channel-stop implant"
  - Perimeter =  $2L_S + W$
  - Area = P \* X<sub>i</sub>
  - Total cap =  $C_{jsw}$
- Total junction cap C = C<sub>j</sub> + C<sub>jsw</sub>

### **Junction Capacitance**

- Voltage Equivalence Factor
  - Creates an average capacitance value for a voltage transition, defined as  $\Delta Q/\Delta V$

$$C_{eq} = \frac{-AC_{j0}V_0}{(V_2 - V_1)(1 - m)} \left( \left(1 - \frac{V_2}{V_0}\right)^{1 - m} - \left(1 - \frac{V_1}{V_0}\right)^{1 - m} \right) = AK_{eq}C_{j0}$$

 $K_{eq} = \frac{-2\sqrt{V_0}}{(V_2 - V_1)} \left( \sqrt{V_0 - V_2} - \sqrt{V_0 - V_1} \right)$  (abrupt junction only)

$$C_{db} = AK_{eq}C_{j0} + PX_{j}K_{eqsw}C_{jsw0}$$

- Consider the following NMOS device
  - Substrate doping:  $N_A = 10^{15} \text{ cm}^{-3}$
  - Source/drain doping:  $N_D = 2 \times 10^{20} \text{ cm}^{-3}$
  - Channel-stop doping: 10X substrate doping
  - Drain length  $L_D = 1$ um
  - Transistor W = 10um
  - Junction depth Xj = 0.5um, abrupt junction

• Find capacitance of drain-bulk junction when drain voltage = 3V

- Inverter Characteristics
  - Transfer functions, noise margins, resistive and nonlinear loads
- CMOS Inverters