EEC 118 Lecture #1: MOSFET Overview

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- **Slides 13-17 Adapted from CSE477 VLSI Digital Circuits Lecture Slides by Vijay Narayanan and Mary Jane Irwin, Penn State University**

Outline

- **Administrative Details**
- **Survey of Digital IC Technology**
- **MOSFET Overview**

Personnel

- **Prof. Raj Amirtharajah (Instructor)**
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  Office Hours: (TBD)
- **Labs**
  Tuesdays 5 PM – 8 PM 2157/2161 Kemper
  Wednesdays 5 PM – 8 PM 2157/2161 Kemper

Course Materials

- **Textbook**

  Digital Integrated Circuits (2nd ed.)
  by J. Rabaey, A. Chandrakasan, and B. Nikolic

- **Suggested References**

  CMOS Digital Integrated Circuits (3rd ed.) Kang and Leblebici
  CMOS VLSI Design (3rd ed.) Weste, Harris

- **Handouts**

  Labs, lab report cover sheets, slides, and lecture notes available on course web page in PDF format.

- **Web Page**

  http://www.ece.ucdavis.edu/~ramirtha/EEC118/S10/S10.html
  Linked from MyUCDavis EEC 118 page and SmartSite

Grading

- **Letter**
- **A: 100 - 90%**
- **B: 90 - 80%**
- **C: 80 - 70%**
- **D: 70 - 60%**
- **F: below 60%**

- **Expect class average to be around B- / C+**
- **Curving will only help you**

Weighting

- **Labs 15%**
- **Design Project 15%**
- **Weekly Homework 5%**

  Scale for each problem: 0 = poor effort, 1 = close, but fundamental problem, 2 = correct
- **Quizzes 10%**

  Four throughout the quarter (approx. every other week), lowest score dropped (April 12, April 26, May 19, May 26)
- **Midterm 20%**

  Monday, May 3, in class
- **Final 35%**

  Tuesday, June 8, 1:00 - 3:00 PM

  Cumulative, but emphasizes material after midterm

Labs and CAD Software Usage

- **Need to know/learn SPICE – Circuit Simulation**
- **Use same breadboard as EEC 180A**
- **<u>No unsupervised lab hours!</u>**
  - TA or instructor must be present for your safety and security of the lab equipment
  - Extra lab hours will be added only in unusual circumstances

Education Demand for Circuit Design

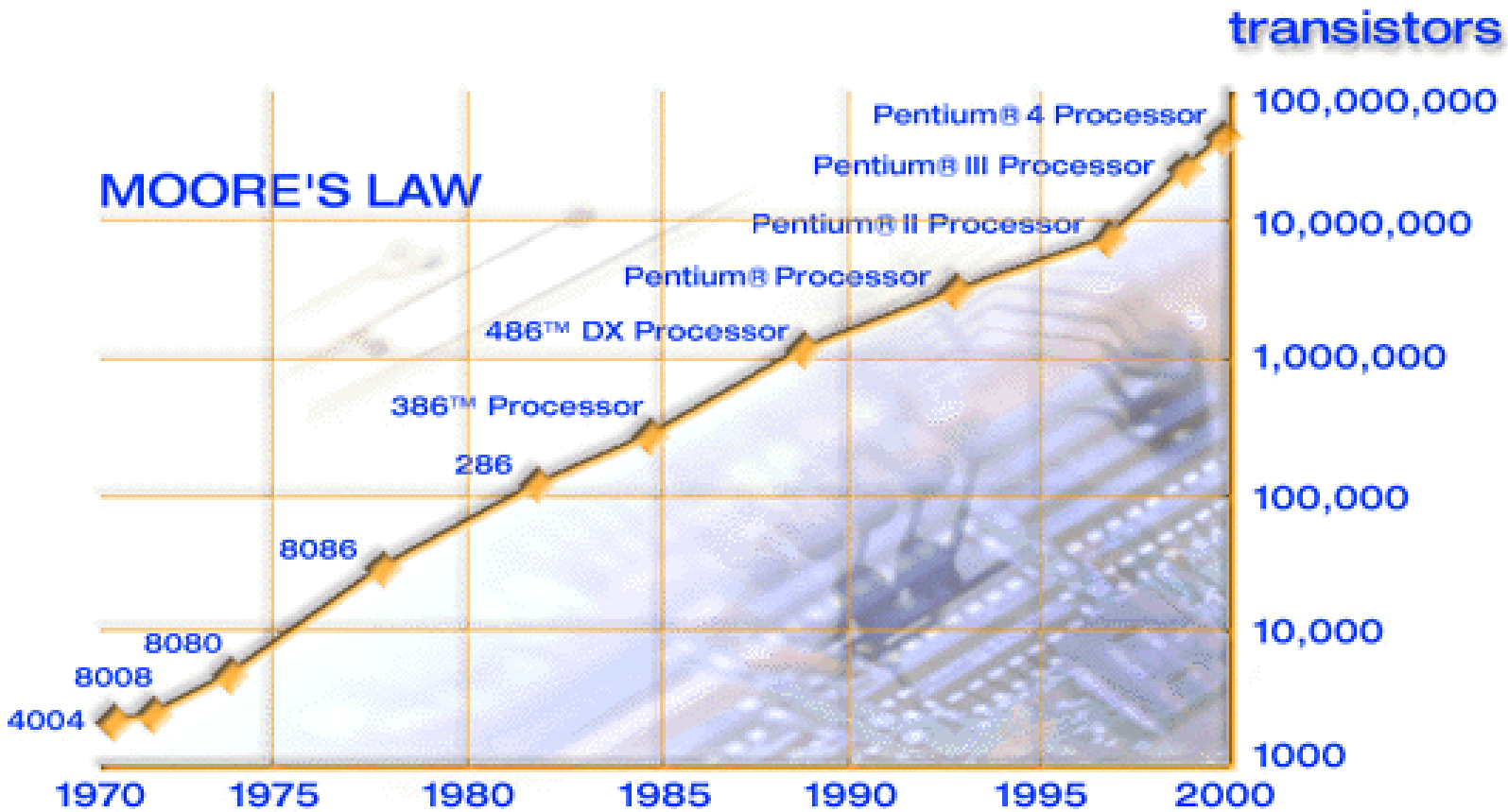
- **Industry needs circuit designers**
  - Not just logic designers
    - Must understand operation at transistor level
  - Not just digital designers
    - Must understand analog effects
  - Not just analog designers
    - Must be able to comprehend Deep Sub-Micron (DSM) effects (<0.13um)
- **Fundamental circuit knowledge critical**
  - Similar techniques for bipolar transistors, NMOS (even relays and vacuum tubes!)
  - Must be able to exploit nanoscale devices in future

Education Demand for System Design

- **Industry needs system designers**
  - Need to understand system implications of your design
    - Power Delivery, Clock Loading – What do you need
  - Need to design from the system point of view
    - Communication protocol – how to effectively talk with other blocks
    - What should be added into your block to meet system design requirements(i.e. comprehend soft block methodology for optimization of area, interconnect, etc.)

You must operate at both levels!

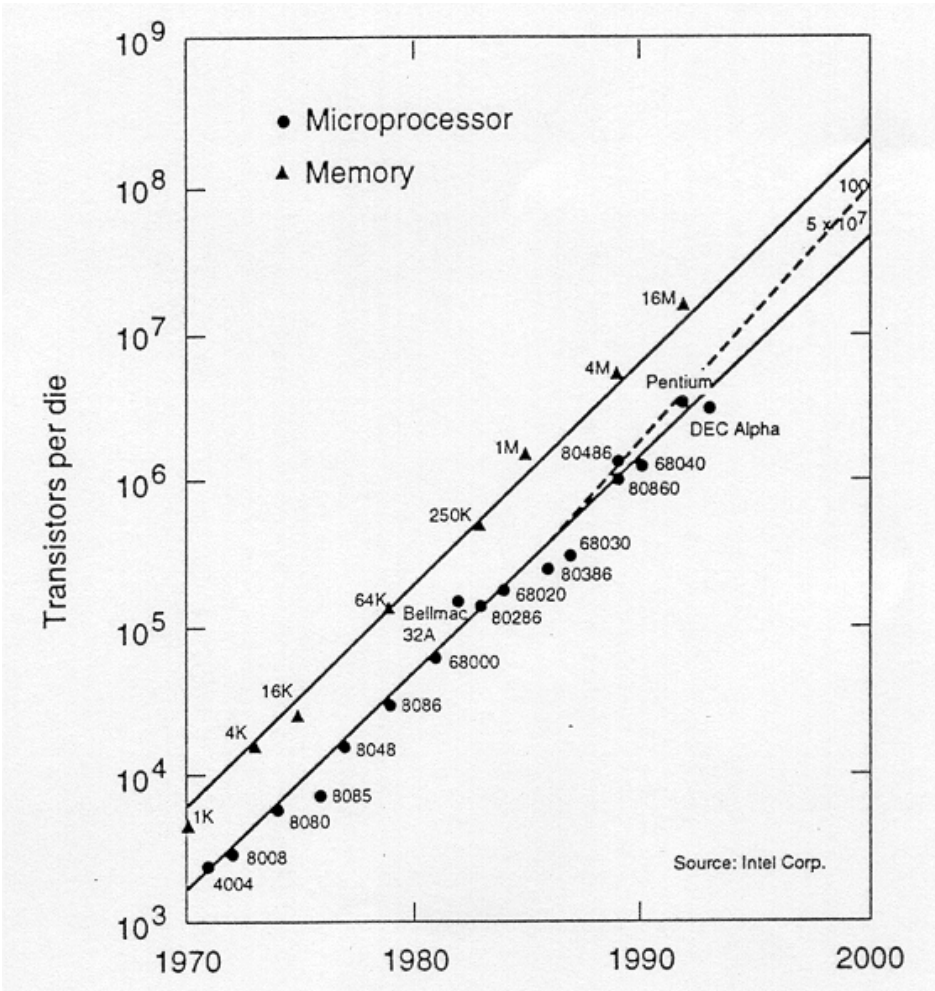
Historical Background



Graph shows the growing complexity of designing integrated circuits

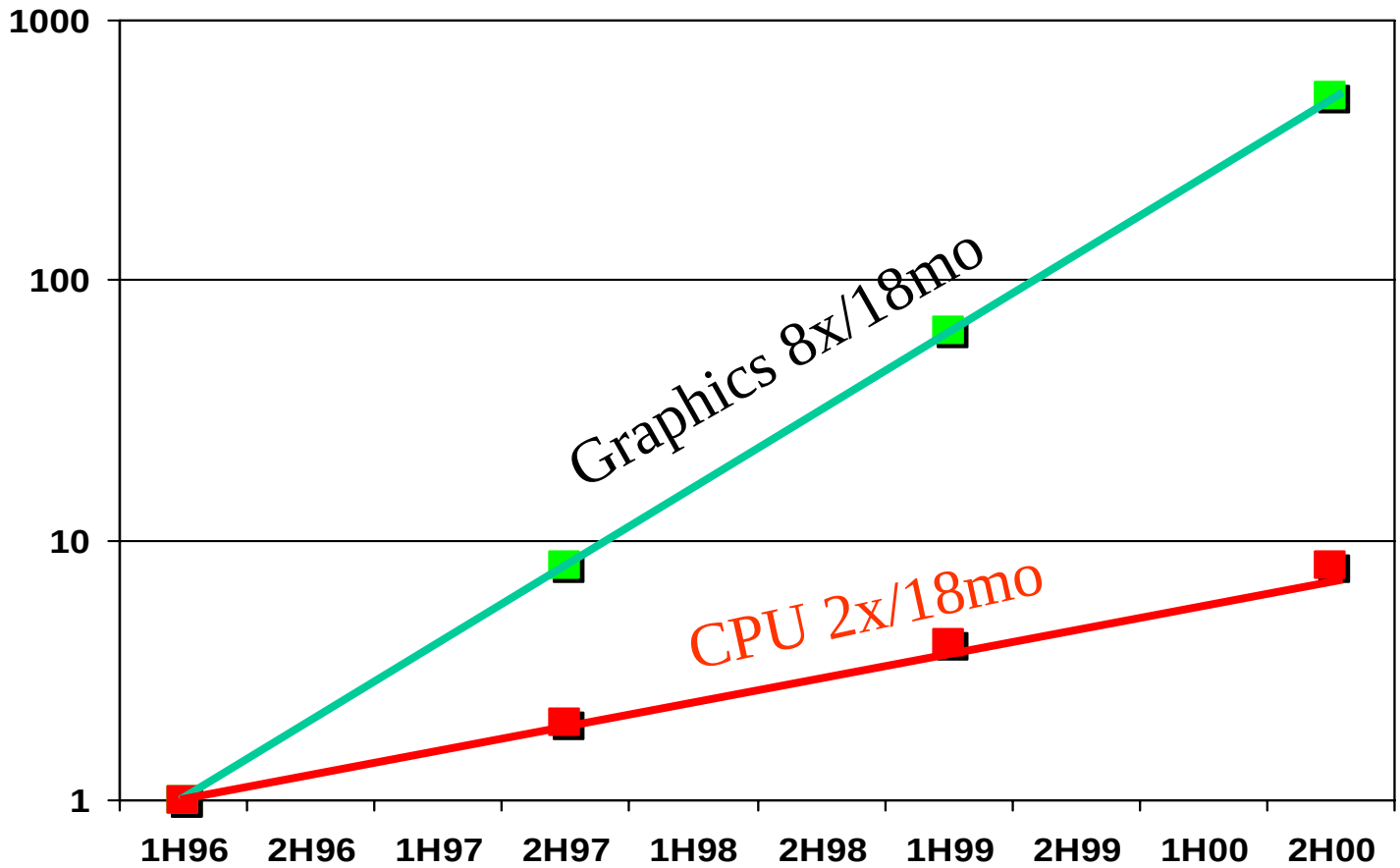
Memory, Processors and Graphics

- **Used to be that memory and processors were the two main design drivers.**



Memory, Processors and Graphics

- **We now have graphics also driving integration**



From ISPD 1999 Keynote Speech by Chris Malachowsky of NVIDIA

Hybrid to Monolithic Trend

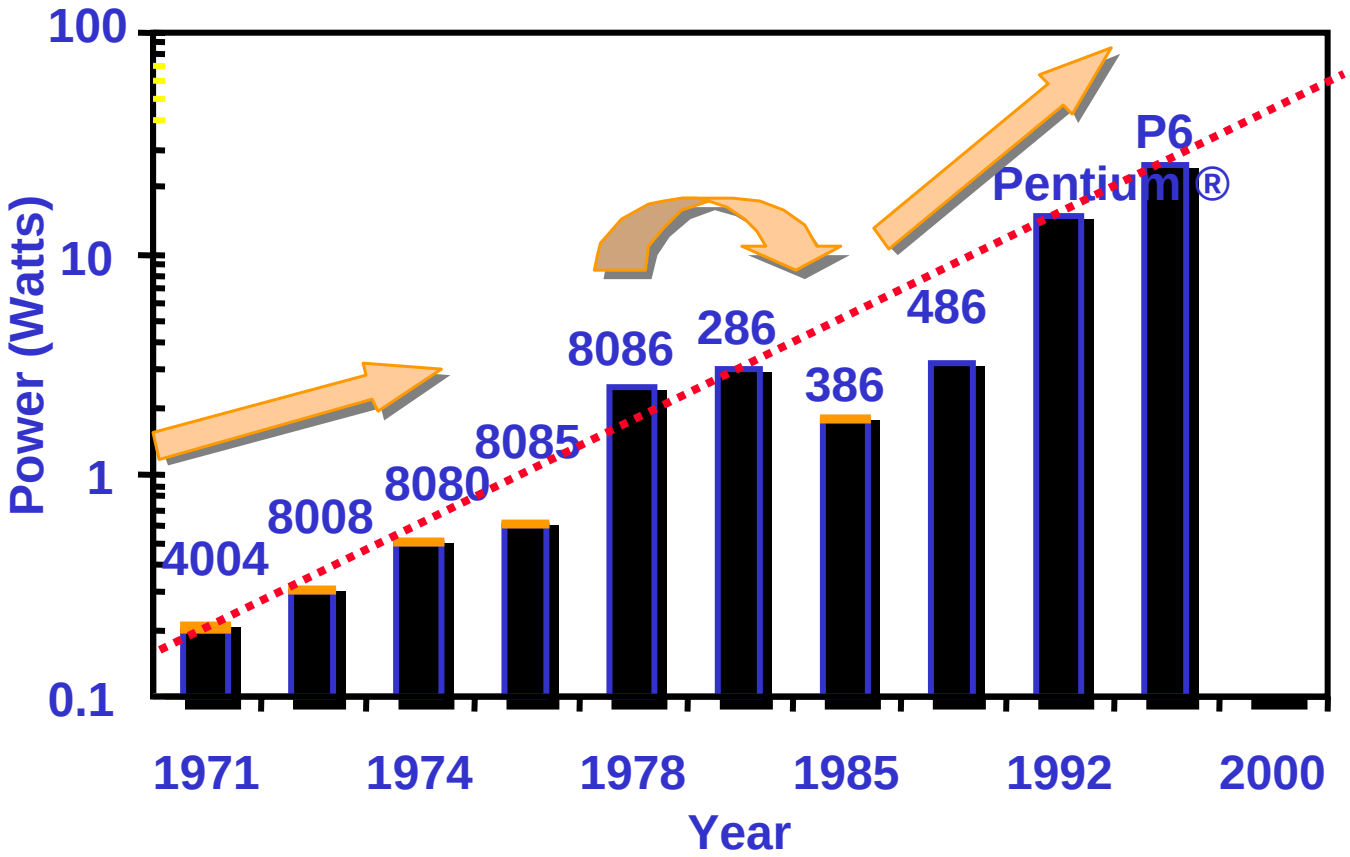
- **We continue to integrate multiple functions on a single chip**
  - Mixture of Analog, Radio Frequency (RF), Digital
  - Graphics/Motherboard chipset an example of this
- **Cost and Performance driving market**
  - Higher performance achieved on chip than off chip
  - Lower cost due to a single die versus multi-chip design
  - Saves on packaging, total area by eliminating redundant functions
- **System-on-a-Chip (SOC) concept**

What are the issues facing the industry ?

- **Growth of transistors is exponential**
- **Growth of operating frequency is (was?) exponential**
  - Reaching a limit due to power dissipation (see current generation Pentiums and Itaniums)
- **Complexity continues to grow**
  - Trend is toward multiple cores on one chip
  - Design teams cannot keep up with trend
- **Power dissipation a concern**
  - Power delivery, thermal issues, long term reliability
- **Manufacturing providing us with lots of transistors**
  - How do we use them effectively (besides large caches)?

Why worry about power? Power Dissipation

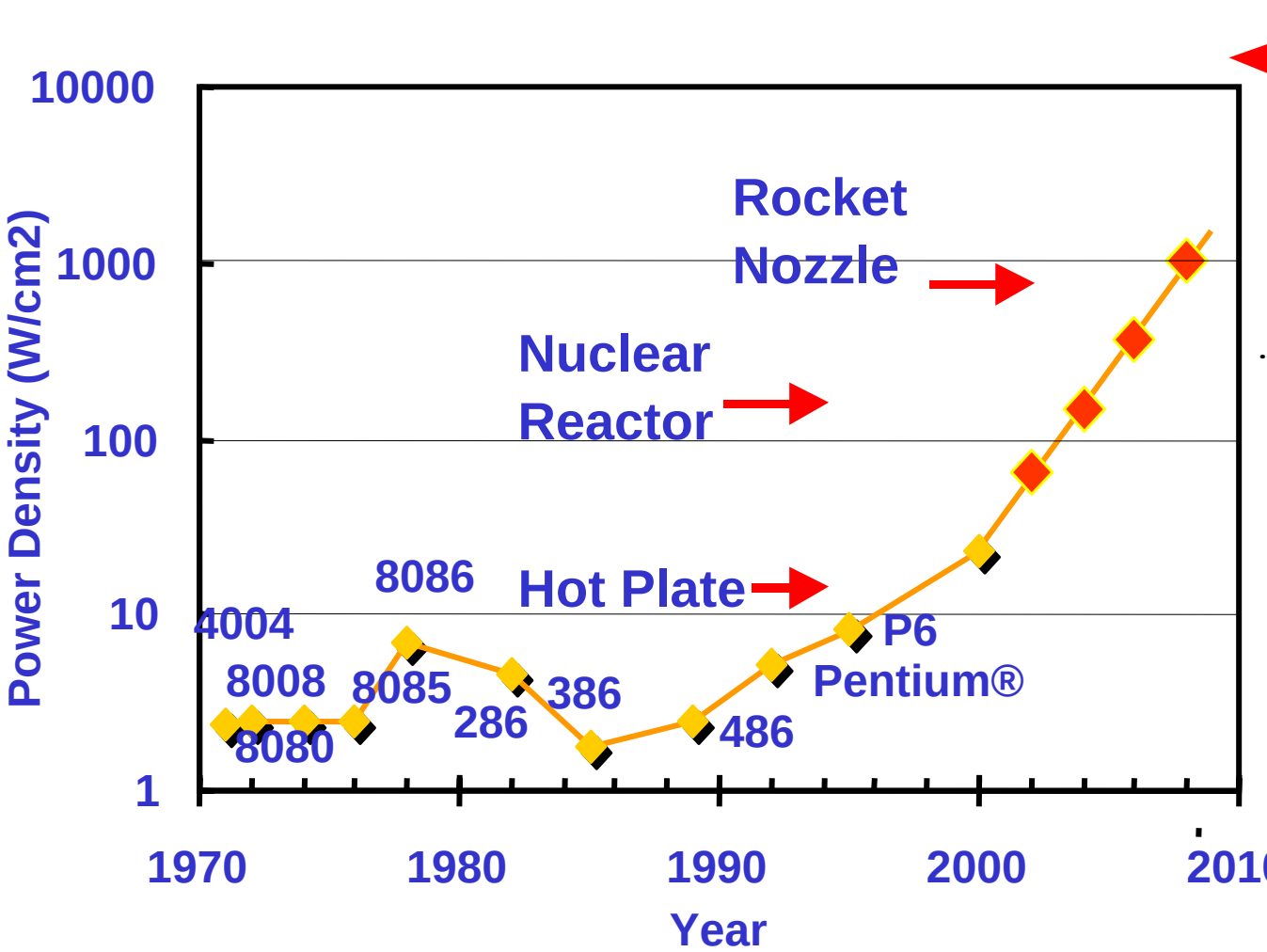
Lead microprocessors power continues to increase



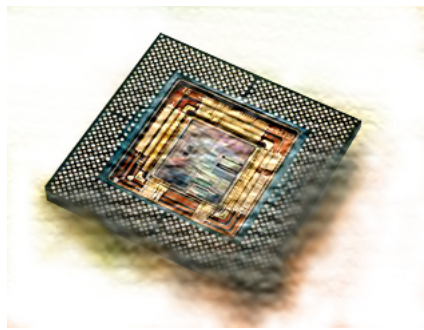
Power delivery and dissipation will be prohibitive

Source: Borkar, De Intel®

Why worry about power? Chip Power Density



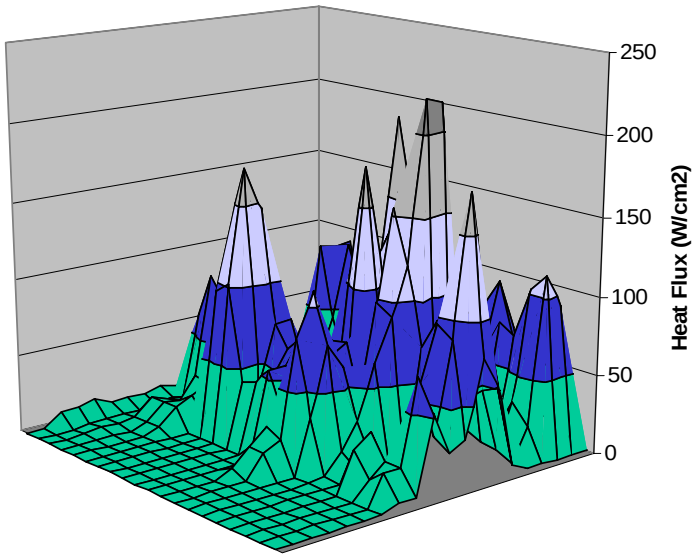
…chips might become hot…



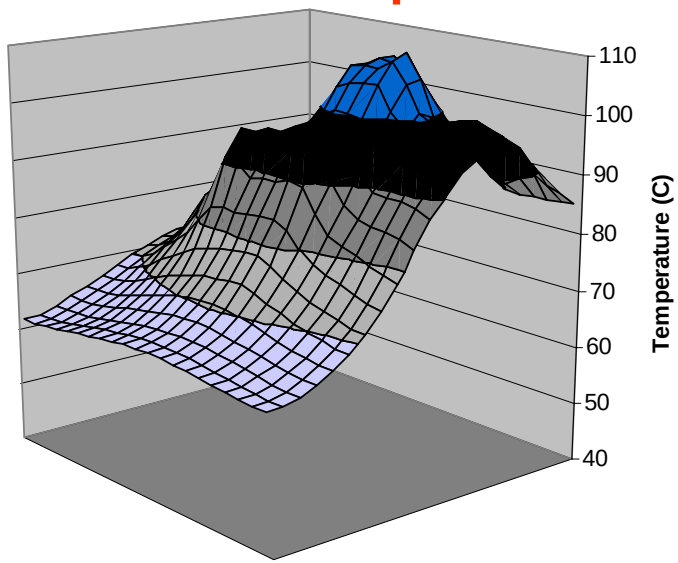
Source: Borkar, De Intel®

Chip Power Density Distribution

Power Map

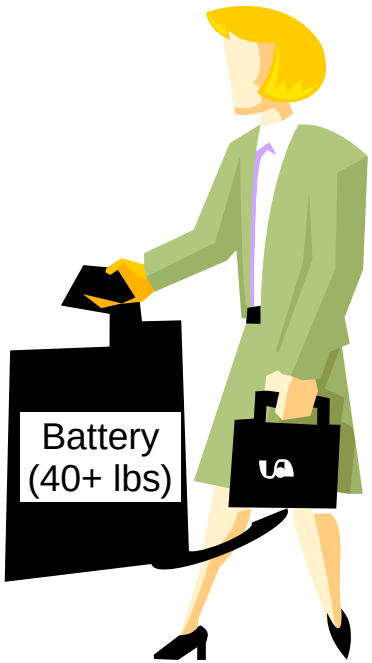


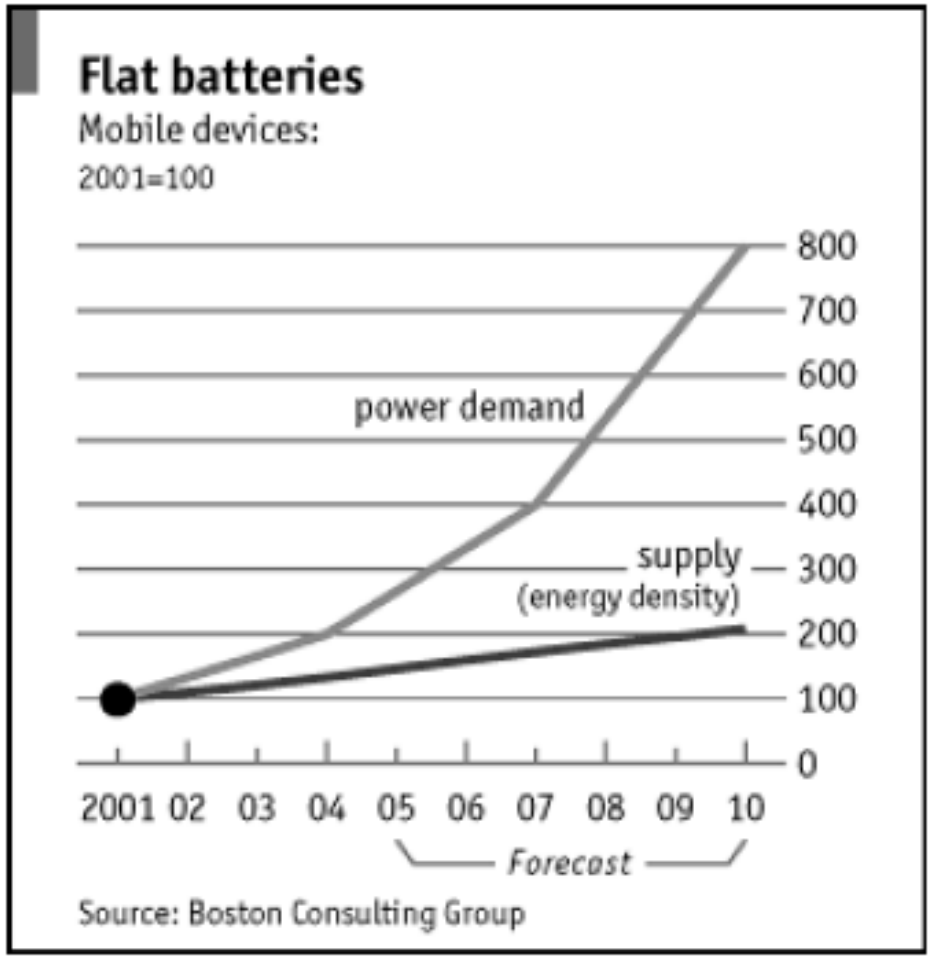
On-Die Temperature



- **Power density is not uniformly distributed across the chip**
- **Silicon not the best thermal conductor (isotopically pure diamond is)**
- **Max junction temperature is determined by hot-spots**
  - Impact on packaging, cooling

Recent Battery Scaling and Future Trends



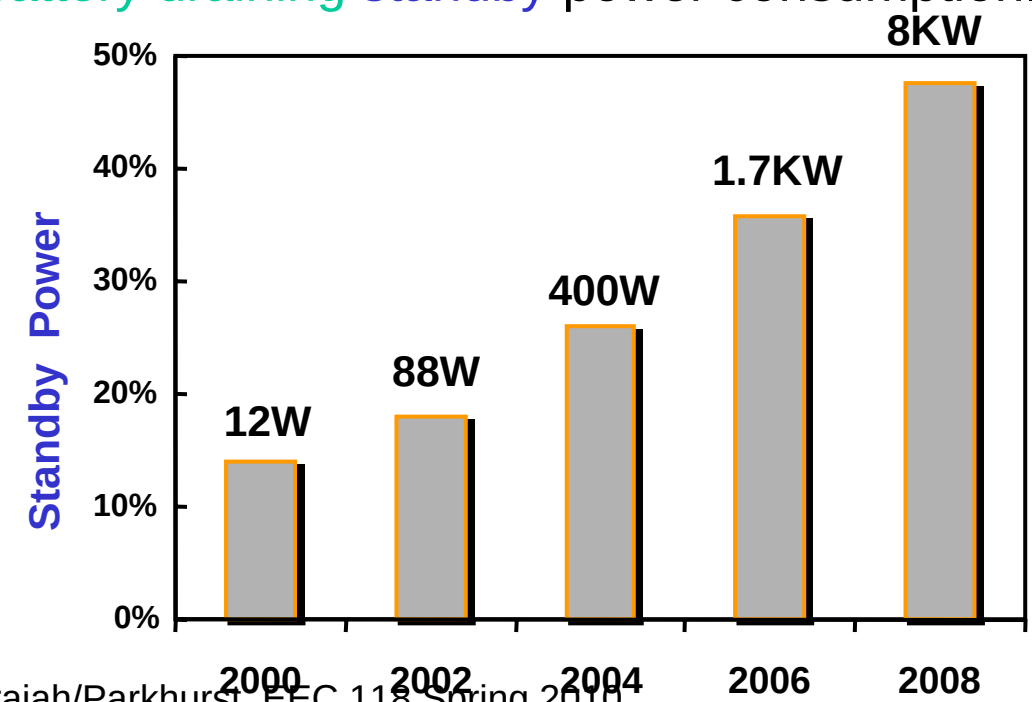


- **Battery energy density increasing 8% per year, demand increasing 24% per year (Economist, January 6, 2005)**

Why worry about power? Standby Power

Year	2002	2005	2008	2011	2014
Power supply V_{dd} (V)	**1.5**	**1.2**	**0.9**	**0.7**	**0.6**
Threshold V_T (V)	**0.4**	**0.4**	**0.35**	**0.3**	**0.25**

- Drain leakage will increase as V_T decreases to maintain noise margins and meet frequency demands, leading to excessive battery draining standby power consumption.

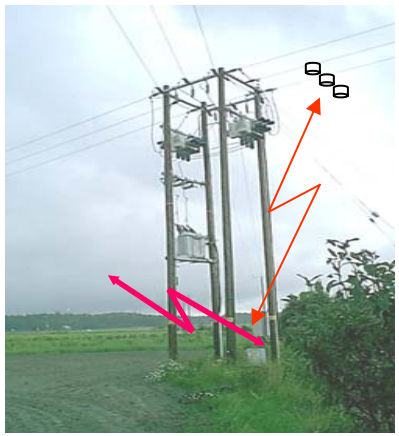


…and phones leaky!

Source: Borkar, De Intel®

Emerging Microsensor Applications

Industrial Plants and Power Line Monitoring (courtesy ABB)

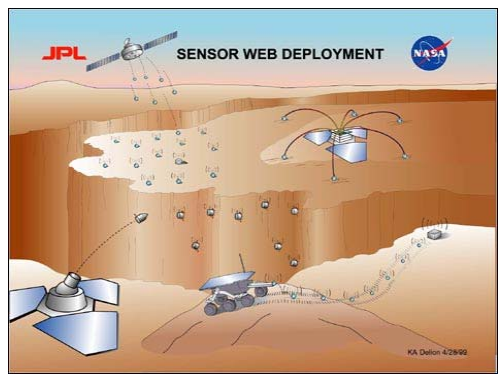


Operating Room of the Future (courtesy John Guttag)

Target Tracking & Detection (Courtesy of ARL)

Location Awareness (Courtesy of Mark Smith, HP)

NASA/JPL *sensorwebs*



Chip Design Styles

- **Field-Programmable Gate Array (FPGA)**
  - Regular structure. Not all transistors are usable.
  - Programmed via software (configurable wiring)
- **Gate Array**
  - Regular structure. Higher usage of transistors than FPGA
  - Two step manufacturing process.
    - Diffusion and poly initially. Design must be fairly stable
    - Metal layers fabricated once design is finalized
- **Cell based design**
  - All transistors used (may have spares to fill in area)
  - Each cell is fixed height so that they can be placed in rows
- **Full Custom**
  - Highest level of compactness and performance
  - Manually intensive. Not conducive to revision (ECO)

Logic Design Families

- **Static CMOS Logic**
  - Good power delay product (energy)
  - Good noise margin
  - Not as fast as dynamic
- **Dynamic Logic**
  - Very fast but inefficient in use of power
  - Domino, CPL, OPL
- **Pass Transistor Logic**
  - Poor noise margin
  - Sometimes static power dissipation
  - Less area than static CMOS

Design Parameters

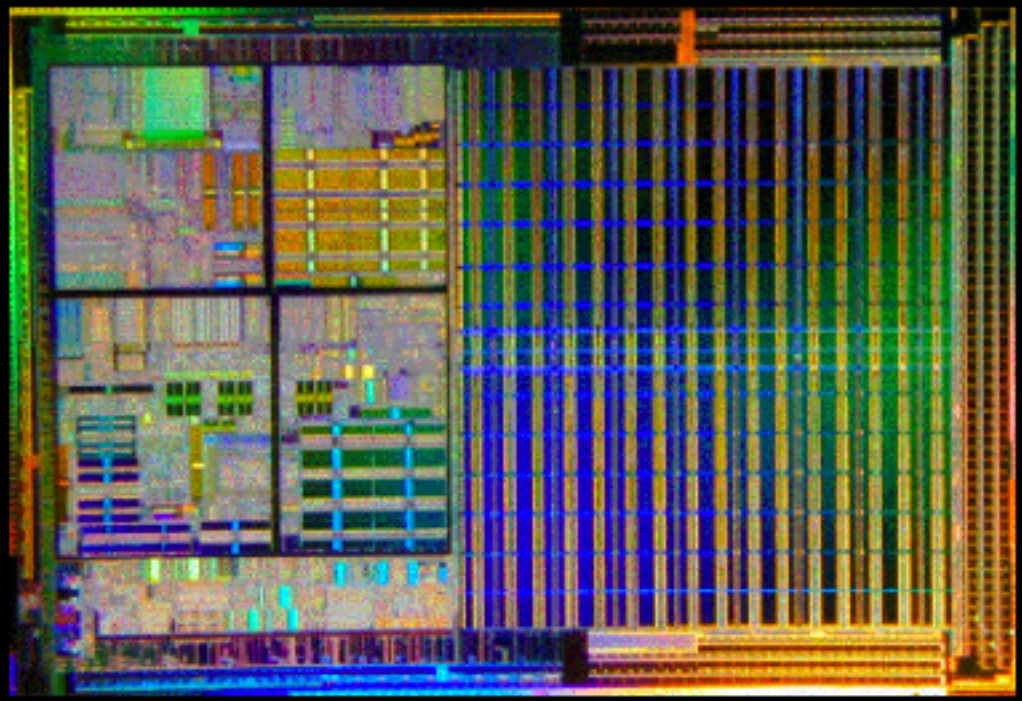
- **Reliability (Not dealt with when relating to layout)**
  - Factors that dictate reliable operation of the circuit
    - Electromigration, thermal issues, hot electrons, noise margins
- **Performance (Dealt with in this class)**
  - Not just measured in clock speed. Power-Delay Product (PDP, equivalent to energy) is a better measure
- **Area (Not dealt with when relating to layout)**
  - Directly affects cost

Current State of the Art

- **Intel Core® @ 4 GHz (1 or 2 cores/chip going to 4+)**
  - 800 - 1066 MHz system bus
  - AGP 8x graphics (533 MHz bus)
  - Memory bus at 533 MHz (DDR)
- **Complex Designs demand resources**
  - Design teams resource limited due to logistics and cost
  - Cannot afford to miss issues due to cost of product recall
  - Emphasis on pre-silicon verification as opposed to post silicon testing

Product Application: AMD's Opteron X86-64

Modern Microprocessor (> 100,000,000 transistors) 2003



One centimeter

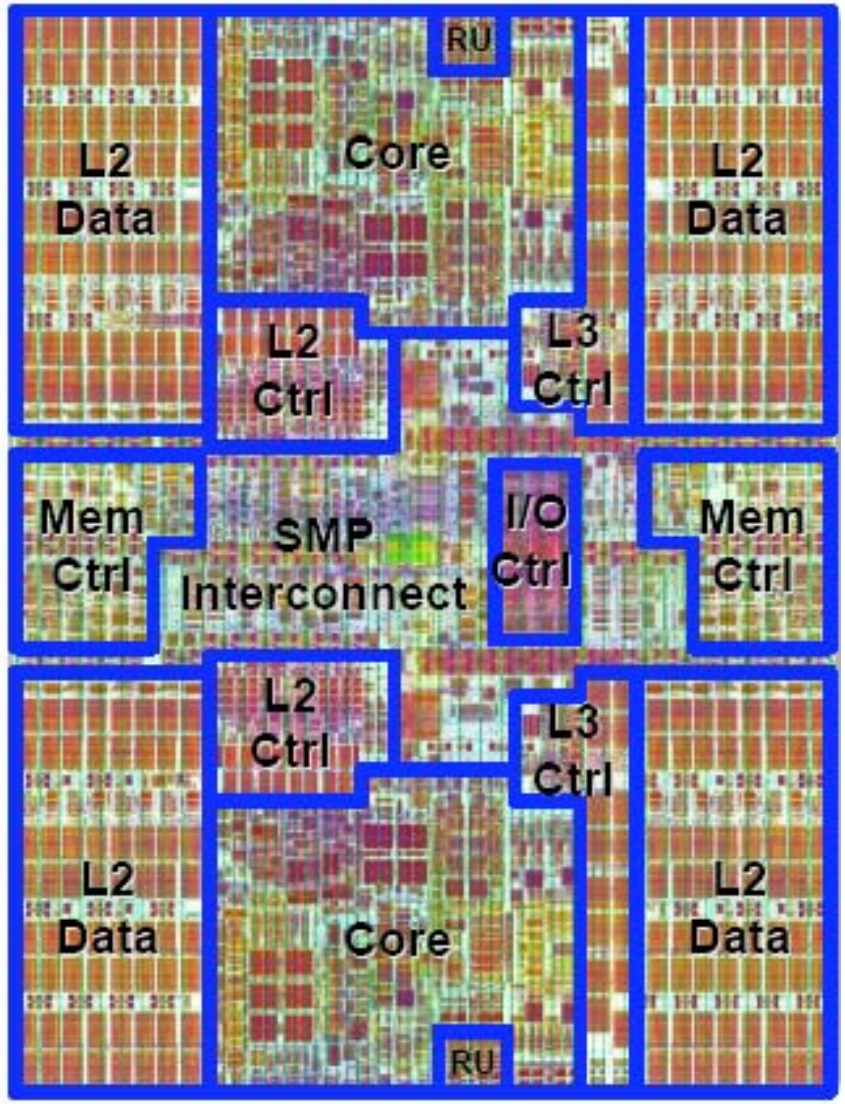
- 8th generation processor (SledgeHammer) w/ 1MB L2 Cache
- Working on 1st (SOI) silicon; > 100 million transistors
- ~180mm² on 130nm technology with Cu metallization and low k

IBM POWER6

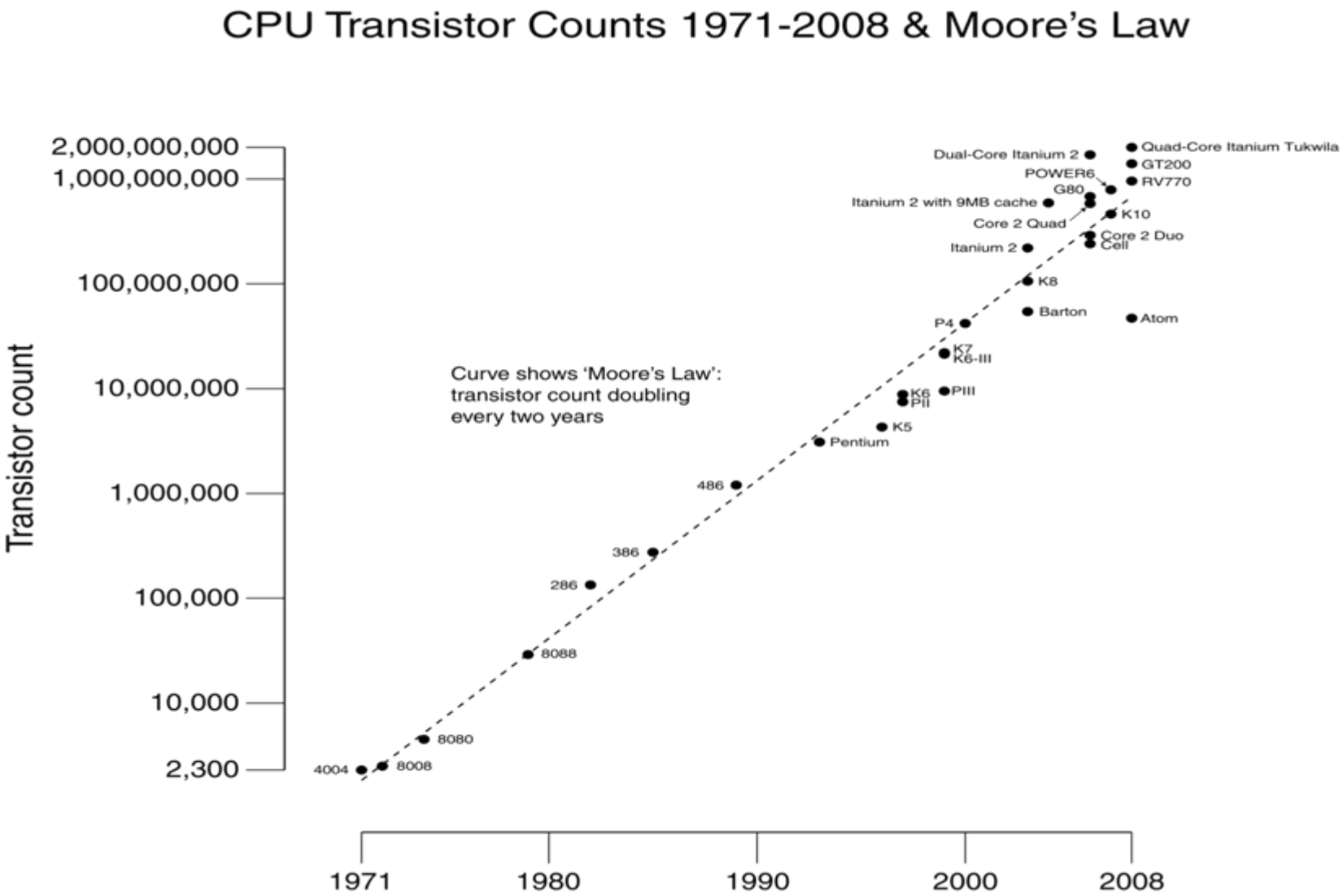
- Ultra-high frequency dual-core chip
  - 7-way superscalar, 2-way SMT core
  - 9 execution units
    - 2LS, 2FP, 2FX, 1BR, 1VMX,1DFU
  - 790M transistors
  - Up to 64-core SMP systems
  - 2x4MB on-chip L2
  - 32MB On-chip L3 directory and controller
  - Two memory controllers on-chip
  - Recovery Unit
- Technology
  - CMOS 65nm lithography, SOI
- High-speed elastic bus interface at 2:1 freq
  - I/Os: 1953 signal, 5399 Power/Gnd

Reick et al., Hot Chips 19, 2007

Modern Multicore Microprocessor (790,000,000 transistors) 2007



Moore's Law

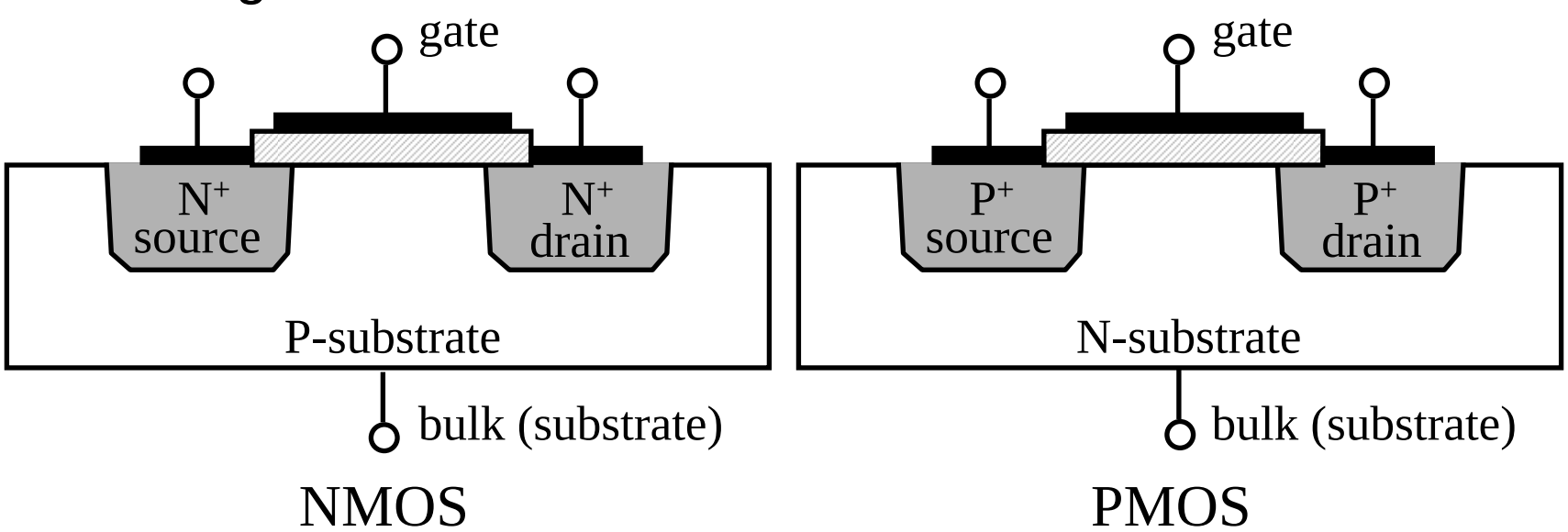

CPU Transistor Counts 1971-2008 & Moore's Law
Transistor count
2,000,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
2,300
Curve shows 'Moore's Law': transistor count doubling every two years
4004
8008
8080
8088
286
386
486
Pentium
K5
PII
K6
PIII
K7
K6-III
P4
Barton
K8
Itanium 2
Core 2 Duo
Cell
Core 2 Quad
K10
Itanium 2 with 9MB cache
G80
POWER6
GT200
RV770
Dual-Core Itanium 2
Quad-Core Itanium Tukwila
Atom
1971
1980
1990
2000
2008
Date of introduction

Expectations

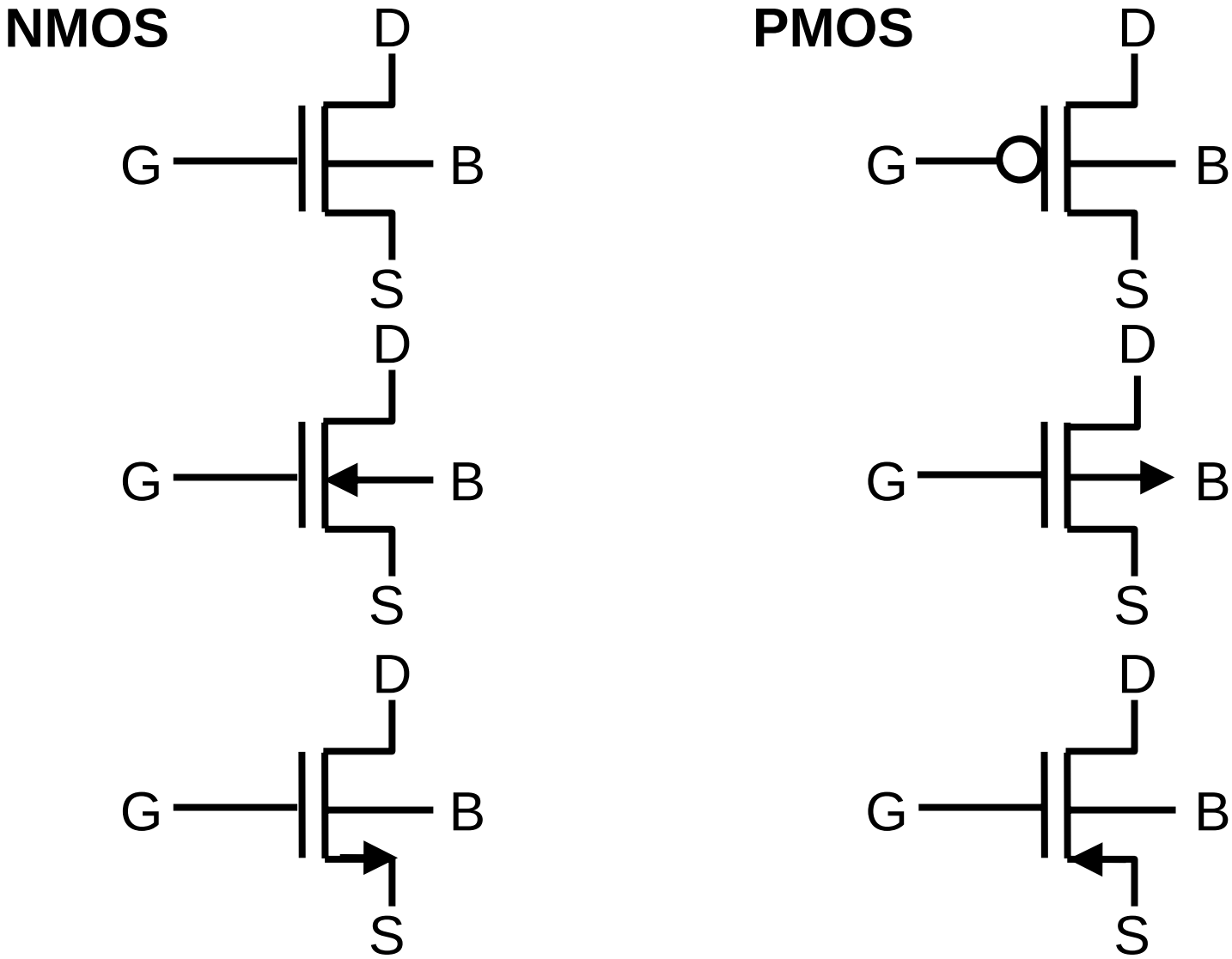
- **You should already know**
  - Solid State – (i.e. PN junctions, semiconductor physics, ..)
- **What we will cover**
  - MOS Transistors Fabrication and Equations
  - CMOS logic at the transistor level
  - Sequential logic
  - Memory
  - Arithmetic Circuits
  - Interconnect
- **Framework**
  - Course to use PowerPoint for the most part
  - Bring PowerPoint slides to class and write notes on them

MOS Transistor Types

- **Rabaey Ch. 3 (Kang & Leblebici Ch. 3)**
- **Two transistor types (analogous to bipolar NPN, PNP)**
  - NMOS: p-type substrate, n^+ source/drain, electrons are charge carriers
  - PMOS: n-type substrate, p^+ source/drain, holes are charge carriers

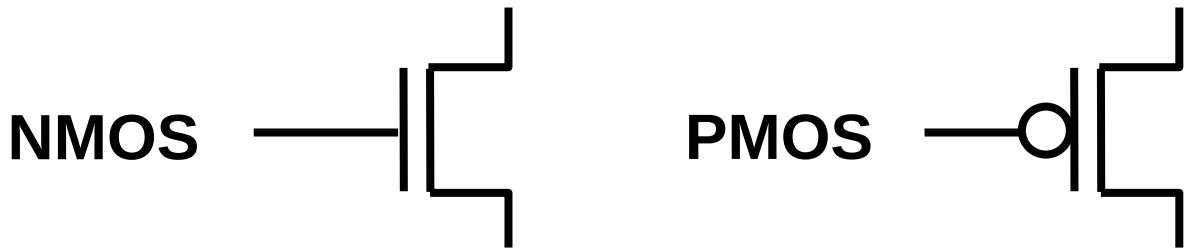


MOS Transistor Symbols



Note on MOS Transistor Symbols

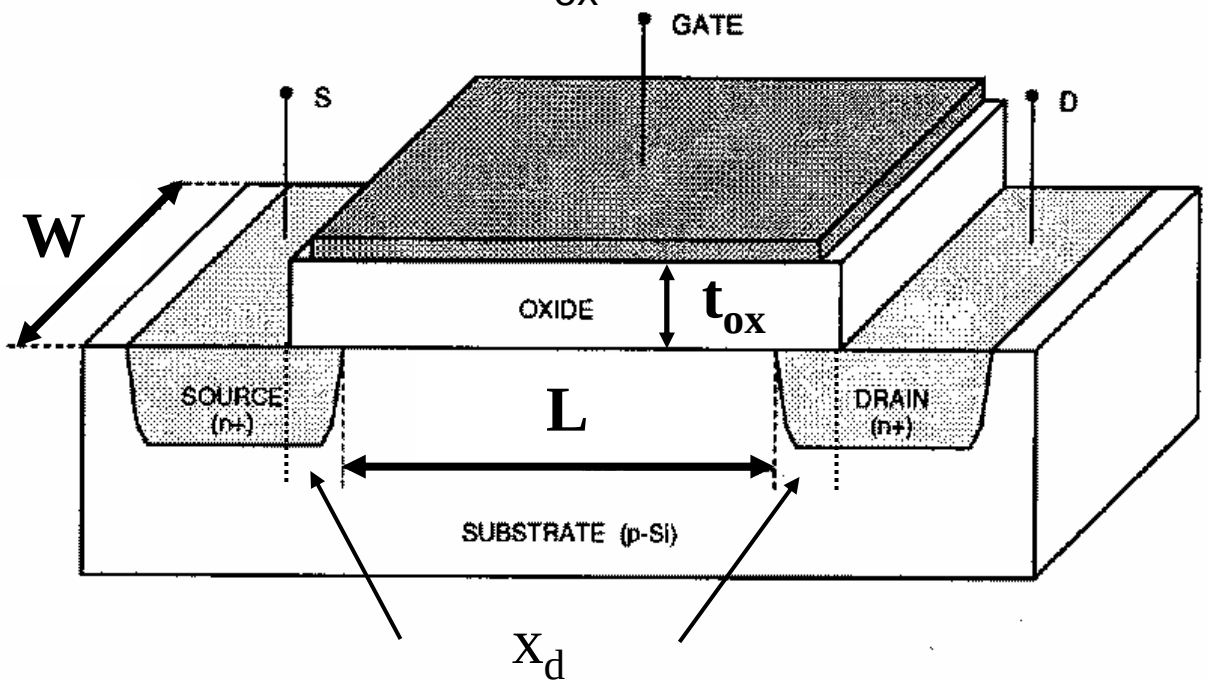
- **All symbols appear in literature**
  - Symbols with arrows are conventional in analog papers
  - PMOS with a bubble on the gate is conventional in digital circuits papers
- **Sometimes bulk terminal is ignored – implicitly connected to supply:**



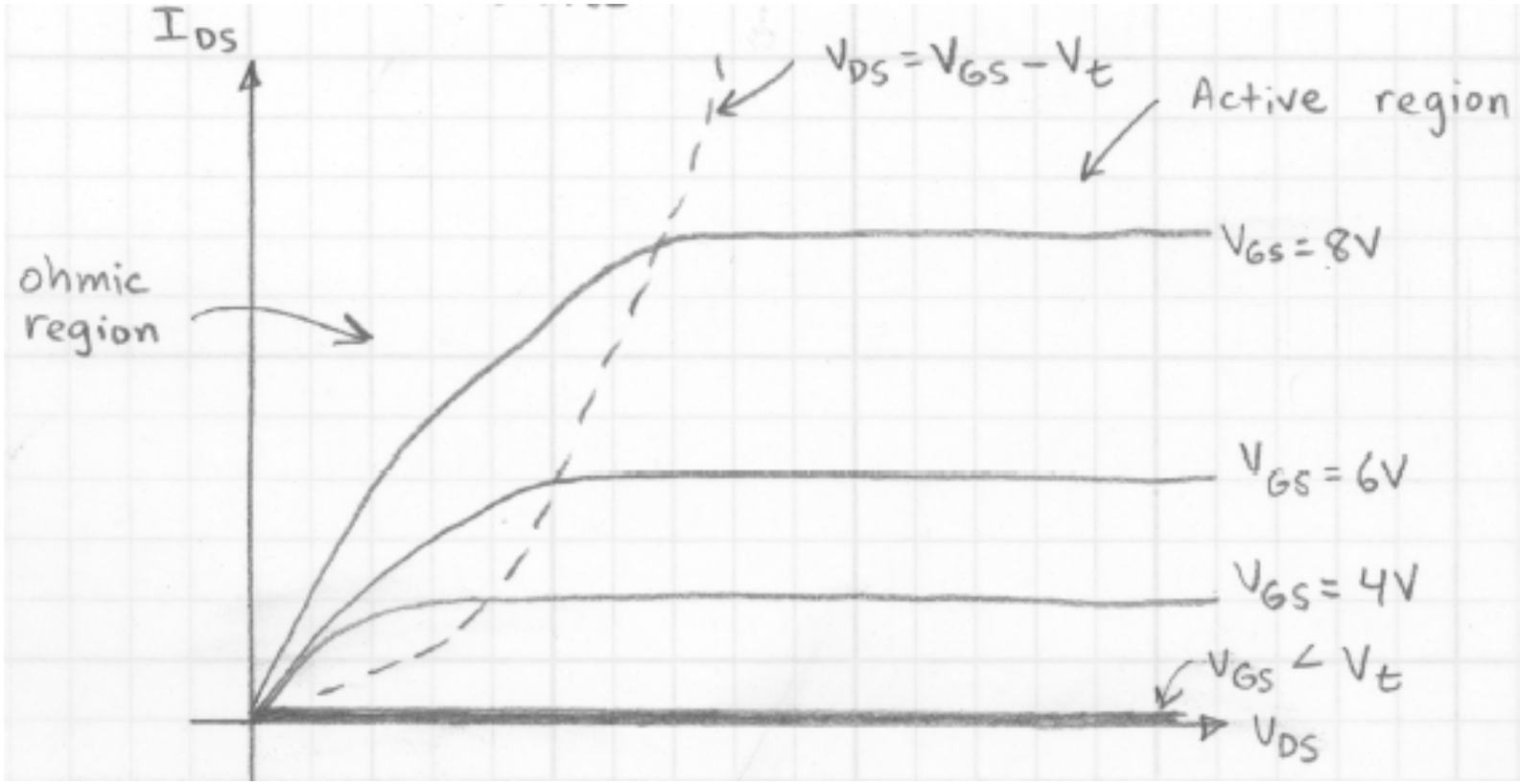
- **Unlike physical bipolar devices, source and drain are usually symmetric**

MOS Transistor Structure

- **Important transistor physical characteristics**
  - Channel length $L = L_D - 2x_d$ (K&L $L = Lgate - 2L_D$)
  - Channel width W
  - Thickness of oxide t_{ox}

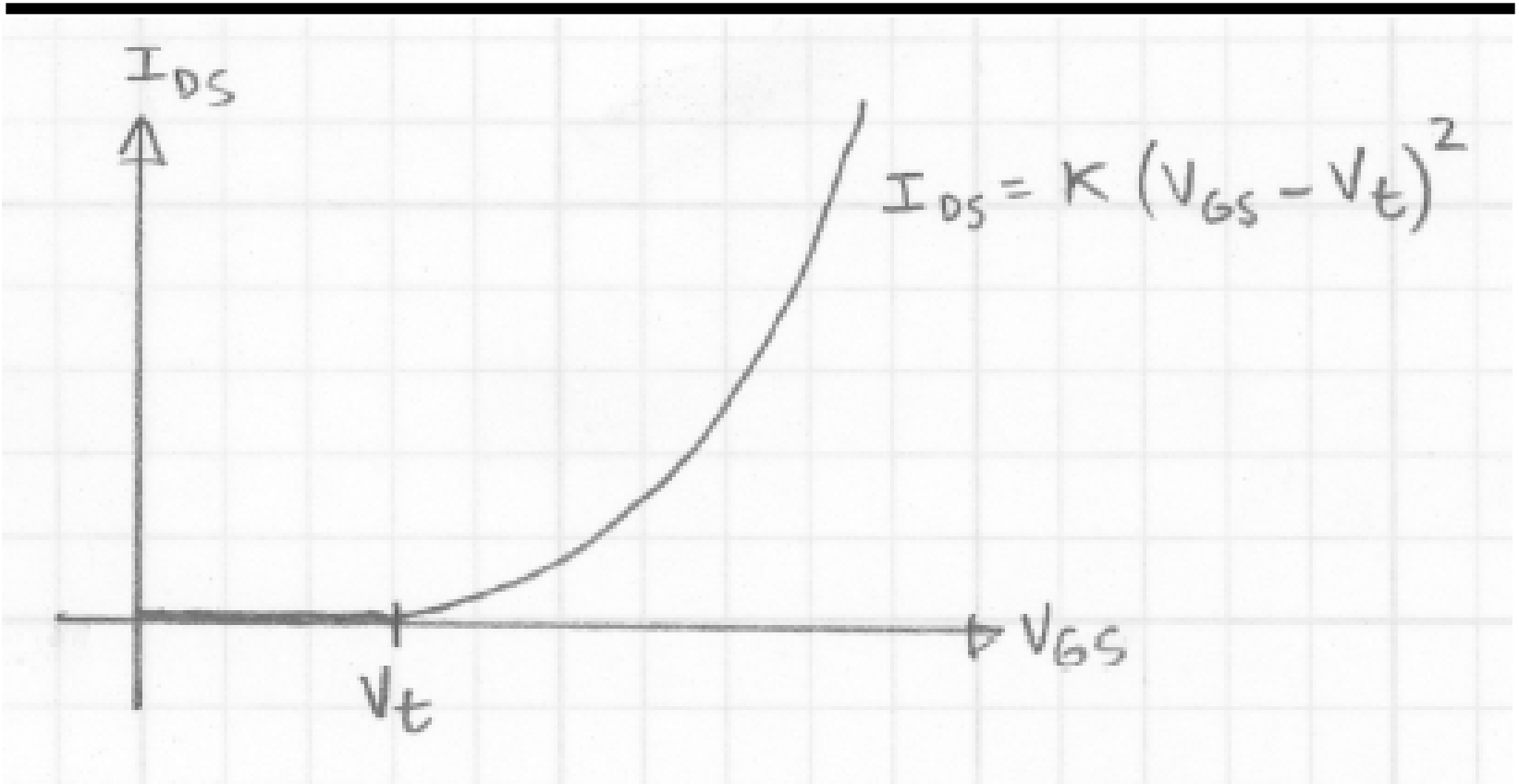


NMOS Transistor I-V Characteristics I



- **I-V curve vaguely resembles bipolar transistor curves**
  - Quantitatively very different
  - Turn-on voltage called Threshold Voltage V_T

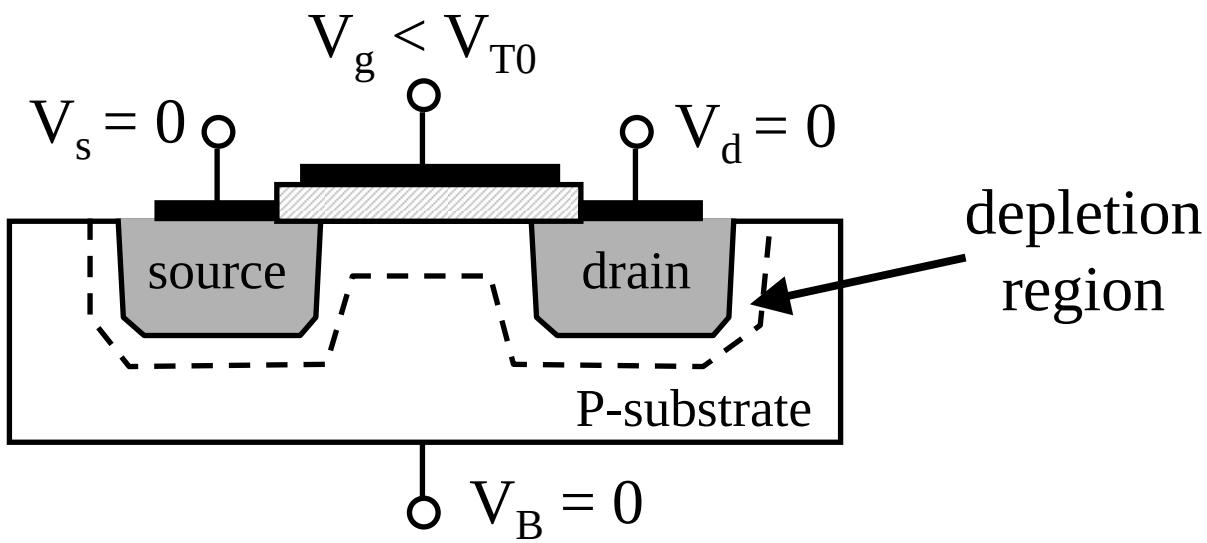
NMOS Transistor I-V Characteristics II



- **Drain current varies quadratically with gate-source voltage V_{GS}**

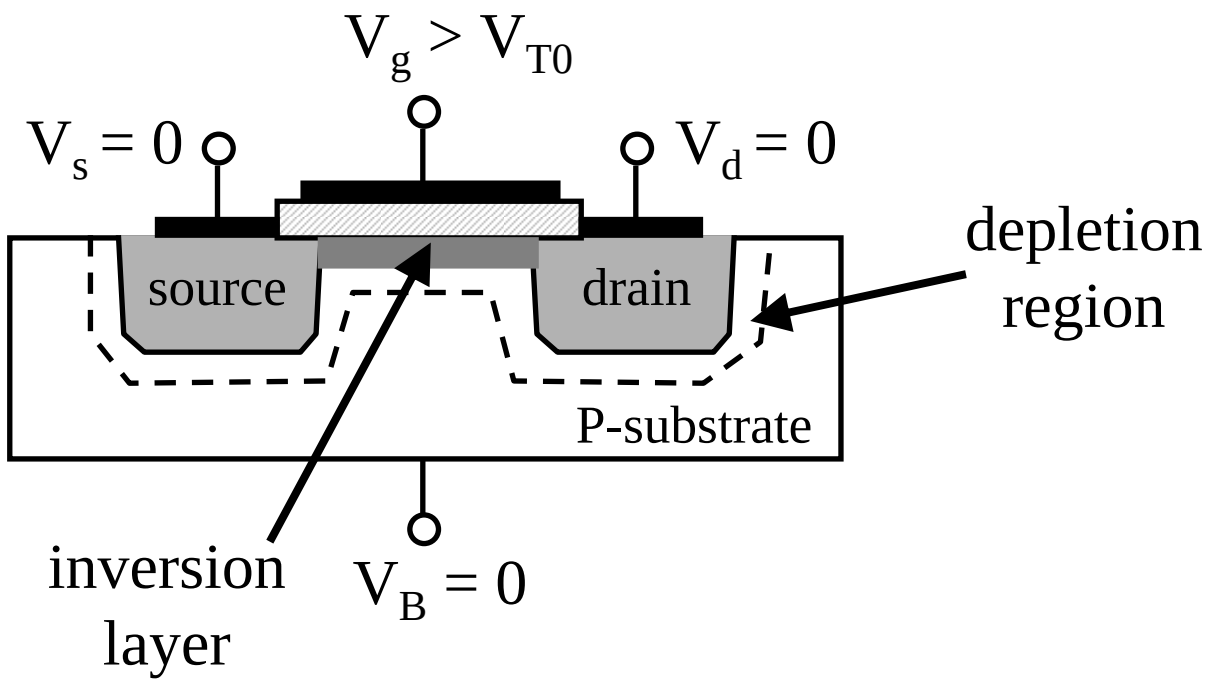
MOS Transistor Operation: Cutoff

- **Simple case: $V_D = V_S = V_B = 0$**
  - Operates as MOS capacitor (Cg = gate to channel)
  - Transistor in cutoff region
- **When $V_{GS} < V_{T0}$, depletion region forms**
  - No carriers in channel to connect S and D (Cutoff)



MOS Transistor Operation: Inversion

- **When $V_{GS} > V_{T0}$, inversion layer forms**
- **Source and drain connected by conducting n-type layer (for NMOS)**
  - Conducting p-type layer in PMOS



Threshold Voltage Components

- **Four physical components of the threshold voltage**

1. **Work function difference between gate and channel (depends on metal or polysilicon gate): Φ_{GC}**
2. **Gate voltage to invert surface potential: $-2\Phi_F$**
3. **Gate voltage to offset depletion region charge: Q_B/C_{ox}**
4. **Gate voltage to offset fixed charges in the gate oxide and oxide-channel interface: Q_{ox}/C_{ox}**

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$ **: gate oxide capacitance per unit area**

Threshold Voltage Summary

- **If $V_{SB} = 0$ (no substrate bias):**

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad \text{(K\&L 3.20)}$$

- **If $V_{SB} \neq 0$ (non-zero substrate bias)**

$$V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|2\phi_F\right|}\right) \quad (3.19)$$

- **Body effect (substrate-bias) coefficient:**

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{ox}} \quad \text{(K\&L 3.24)}$$

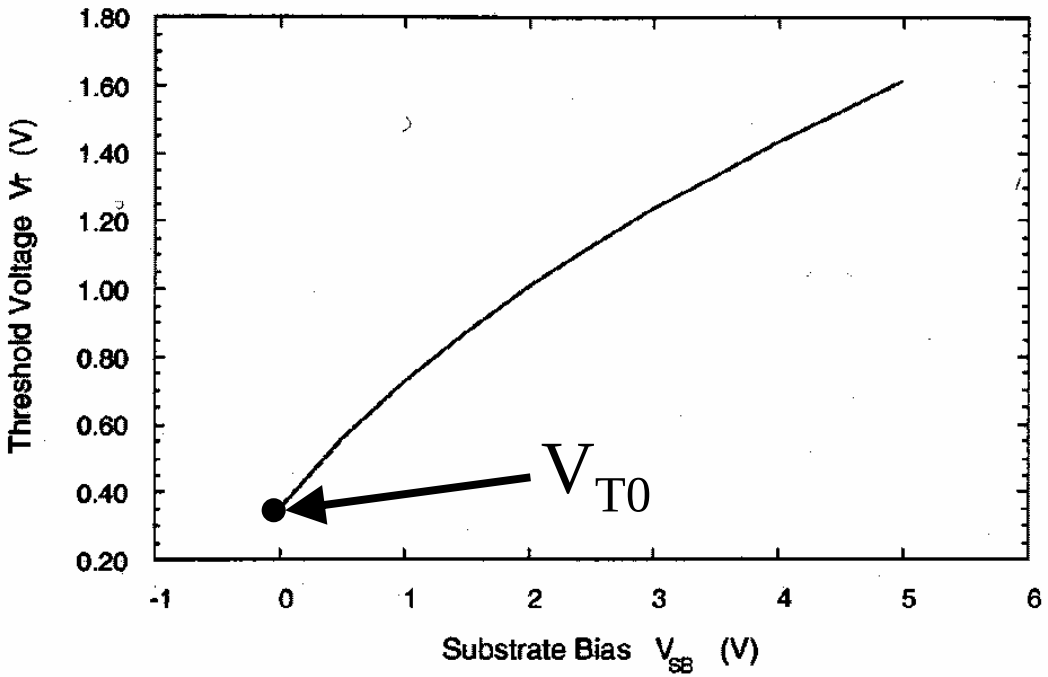
- **Threshold voltage increases as V_{SB} increases!**

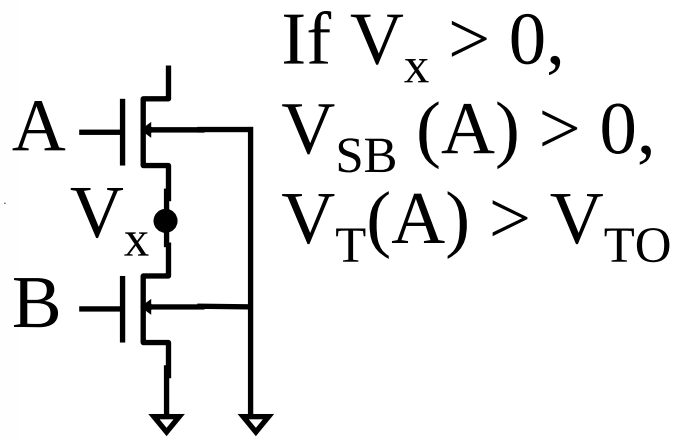
Threshold Voltage (NMOS vs. PMOS)

	NMOS	PMOS
Substrate Fermi potential	$\phi_F < 0$	$\phi_F > 0$
Depletion charge density	$Q_B < 0$	$Q_B > 0$
Substrate bias coefficient	$\gamma > 0$	$\gamma < 0$
Substrate bias voltage	$V_{SB} > 0$	$V_{SB} < 0$

Body Effect

- **Body effect: Source-bulk voltage V_{SB} affects threshold voltage of transistor**
  - Body normally connected to ground for NMOS, Vdd (Vcc) for PMOS
  - Raising source voltage increases V_T of transistor
  - Implications on circuit design: series stacks of devices





MOS Transistor Regions of Operation

- **Three main regions of operation**
- **<u>Cutoff</u>: $V_{GS} < V_T$**
  No inversion layer formed, drain and source are isolated by depleted channel. $I_{DS} \approx 0$
- **<u>Linear (Triode, Ohmic)</u>: $V_{GS} > V_T$, $V_{DS} < V_{GS}-V_T$**
  Inversion layer connects drain and source. Current is almost linear with V_{DS} (like a resistor)
- **<u>Saturation</u>: $V_{GS} > V_T$, $V_{DS} \geq V_{GS}-V_T$**
  Channel is "pinched-off". Current saturates (becomes independent of V_{DS}, to first order).

MOSFET Drain Current Overview

Saturation: $$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2\left(1 + \lambda V_{DS}\right)$$

Linear (Triode, Ohmic):

$$I_D = \mu C_{ox}\frac{W}{L}\left(\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

Cutoff: $$I_D \approx 0$$

"Classical" MOSFET model, will discuss deep submicron modifications as necessary (Rabaey, Eqs. 3.25, 3.29)

A Fourth Region: Subthreshold

Subthreshold: $$I_D = I_S e^{\frac{V_{GS}}{n\,kT/q}} \left(1 - e^{-\frac{V_{DS}}{kT/q}} \right)$$

- **Sometimes called “weak inversion” region**
- **When V_{GS} near V_T, drain current has an exponential dependence on gate to source voltage**
  - Similar to a bipolar device
- **Not typically used in digital circuits**
  - Sometimes used in very low power digital applications
  - Often used in low power analog circuits, e.g. quartz watches

Next Topic: MOSFET Details

- **MOS Structure**
  - Derivation of threshold voltage, drain current equations
- **MOSFET Scaling**
- **MOSFET Capacitances**