EEC 118 Lecture #16: Manufacturability

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Outline

- Finish interconnect discussion
- Manufacturability: Rabaey G, H (Kang & Leblebici, 14)

Design for Manufacturability

- **For class projects or university research, goal is a single working circuit or small number of prototypes**
  - Similar scale for industrial research projects
- **Production goal is usually thousands to 100s of millions of working (or at least marketable) parts**
  - Must evaluate circuit designs over a range of parameter variations to ensure correct functionality, performance
- **Design for Manufacturability or Statistical Circuit Design encompasses a variety of techniques**
  - Yield estimation and maximization, worst-case analysis, etc.

Circuit Parameter Variations

- **All circuit parameters vary some amount due to variations in process, lithography, or environment**
  - Geometric parameters: transistor W and L
  - Device parameters: V_T, t_{ox}, μ
  - Interconnect parameters: *R*, *C*
  - Operating conditions: V_{DD}, T
- **Variations occur both spatially and temporally**
  - Circuit-to-circuit on same die (spatial)
  - Die-to-die on same wafer (spatial)
  - Wafer-to-wafer in same fab (temporal)
- **Example: transistor width $W = W^0 + \Delta W$**

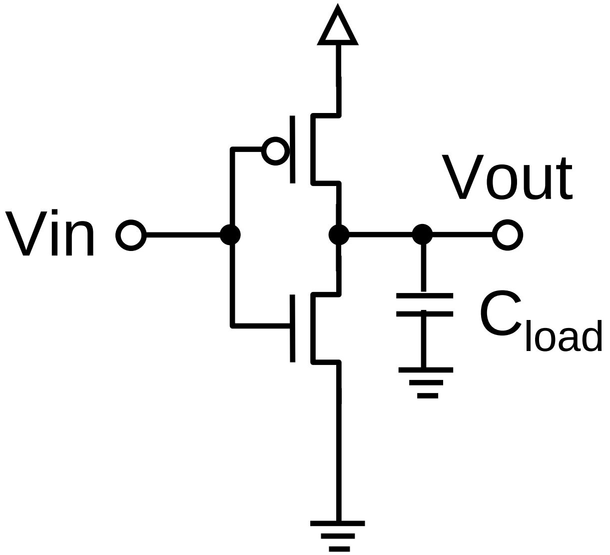
Increasing variation

Designer controls

Random

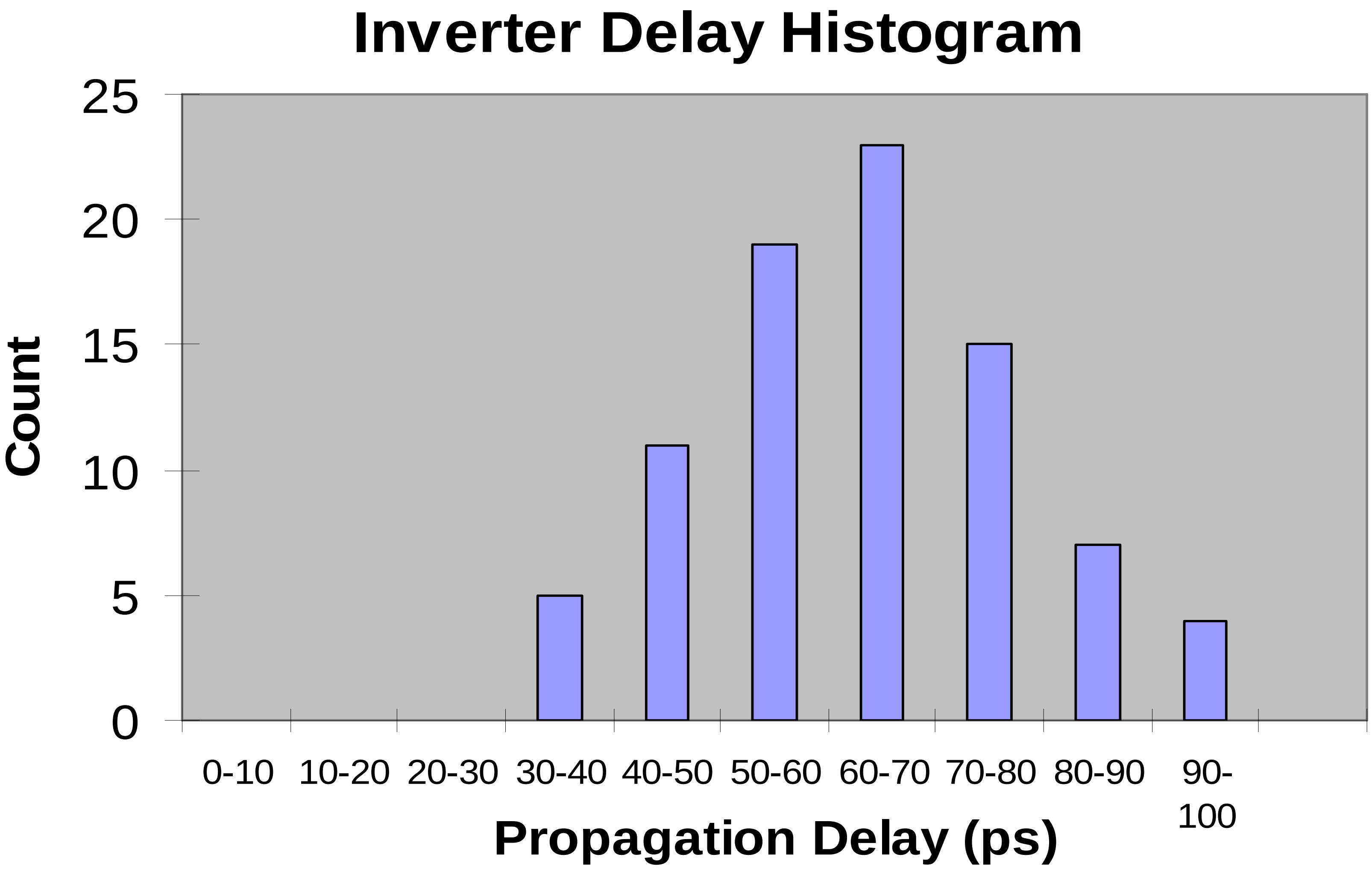
CMOS Inverter Example

- **For both NMOS and PMOS:**
  - $W = W^0 + \Delta W$
  - $L = L^0 + \Delta L$
  - $V_T = V_T{}^0 + \Delta V_T$
  - $k' = k'^0 + \Delta k'$
- **For capacitor:**
  - $C_{load} = C^0 + \Delta C$
- **For entire circuit:**
  - $T = T^0 + \Delta T$
  - $V_{DD} = V_{DD}{}^0 + \Delta V_{DD}$



- **All these parameters affect circuit performance!**

Performance Variation Example



- **Delay variations with parameters, loading, V_{DD}, and T**

Yield Estimation and Maximization

- **Parametric <u>Yield:</u> ratio of total acceptable circuits to total manufactured circuits**
  - Design for manufacturability aims to maximize yield (and $$)
- **Yield statistics are usually complicated since circuit performance is complex function of parameters**
- **Numerous methods for estimating and maximizing yield**
  - Response surface models (RSM): compact analytical model fit to circuit simulations using Design of Experiments
  - Direct Monte Carlo circuit simulations or the RSM can be used to estimate yields
  - Designer controlled parameters then adjusted to maximize yield estimates

Worst-Case Design 1

- **Given range of variations for process, voltage, temperature identify worst (best) cases for performance parameter of interest**
  - Process corner models from fab define limits of device performance
  - Labeled by NMOS-PMOS pairs, e.g. Typical NMOS-Typical PMOS (TT)
  - Usual additional corners: Fast NMOS-Fast PMOS (FF), Slow NMOS-Slow PMOS (SS), Fast NMOS-Slow PMOS (FS), Slow NMOS-Fast PMOS (SF)
  - Usual voltage corners: Nominal V_{DD} +/- 10%
  - Temperature range: 0 – 100 ^{o}C

Worst-Case Design 2

- **Identify worst (best) cases for performance parameter of interest**
- **Typical Speed Corner**
  - Typical NMOS-Typical PMOS (TT), nominal VDD, room temperature 27 ^oC
- **Slow Speed Corner**
  - Slow NMOS-Slow PMOS (SS), 0.9 x VDD, maximum temperature 100 ^oC
- **Fast Speed Corner**
  - Fast NMOS-Fast PMOS (FF), 1.1 x VDD, minimum temperature 0 ^oC

Summary

- **Design for manufacturability converts a prototype into a “real” design for large-scale production**
  - Statistical models of process, device and interconnect parameters, and operating conditions used to estimate and maximize yield (and profits)
  - Analysis is difficult because of complexity, usually numerical models and many simulations required
- **Variability trend is worsening as processes shrink**
  - For example, locations of individual dopant atoms can affect transistor performance
- **Statistical circuit design is becoming as important as performance and power!**

Next Topic: Future Directions & Final Review

- **Future directions in CMOS digital circuits**
- **Alternative logic technologies to CMOS**
- **Final exam review**