EEC 118 Lecture #15: Interconnect

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Outline

- Review and Finish: Low Power Design
- Interconnect Effects: Rabaey Ch. 4 and Ch. 9 (Kang & Leblebici, 6.5-6.6)

Interconnect Modeling

- Early days of CMOS, wires could be treated as ideal for most digital applications, not so anymore!
- On-chip wires have resistance, capacitance, and inductance
 - Similar to MOSFET charging, energy depends solely on capacitance
 - Resistance might impact low power adiabatic charging, static current dissipation, speed
 - Ignore inductance for all but highest speed designs
- Interconnect modeling is whole field of research itself!

Interconnect Models: Regions of Applicability

- For highest speed applications, wire must be treated as a transmission line
 - Includes distributed series resistance, inductance, capacitance, and shunt conductance (*RLGC*)
- Many applications it is sufficient to use lumped capacitance (*C*) or distributed series resistance-capacitance model (*RC*)
- Valid model depends on ratio of rise/fall times to timeof-flight along wire
 - *I*: wire length
 - v: propagation velocity (speed of light)
 - I/v: time-of-flight on wire

Interconnect Models: Regions of Applicability

• Transmission line modeling (inductance significant):

$$t_{rise} (t_{fall}) < 2.5 \times (l / v)$$

• Either transmission line or lumped modeling:

$$2.5 \times (I / v) < t_{rise} (t_{fall}) < 5 \times (I / v)$$

• Lumped modeling:

$$t_{rise} (t_{fall}) > 5 \times (I / v)$$

- Resistance proportional to length and inversely proportional to cross section
- Depends on material constant resistivity ρ (Ω -m)



Parallel-Plate Capacitance

 Width large compared to dielectric thickness, height small compared to width: E field lines orthogonal to substrate



$$C = \frac{\mathcal{E}_r}{h} WL$$

Fringing Field Capacitance

 When height comparable to width, must account for fringing field component as well



Total Capacitance Model

- When height comparable to width, must account for fringing field component as well
- Model as a cylindrical conductor above substrate



 Total capacitance per unit length is parallel-plate (area) term plus fringing-field term:

$$c = c_{pp} + c_{fringe} = \frac{\varepsilon_r}{h} \left(W - \frac{t}{2} \right) + \frac{2\pi\varepsilon_r}{\log(2h/t+1)}$$

- Model is simple and works fairly well (Rabaey, 2nd ed.)
 - More sophisticated numerical models also available
- Process models often give both area and fringing (also known as sidewall) capacitance numbers per unit length of wire for each interconnect layer

Alternative Total Capacitance Models

• For wide lines (w ≥ t/2) Kang & Leblebici Eq. 6.53:

$$C = \frac{\varepsilon_r}{h} \left(W - \frac{t}{2} \right) + \frac{2\pi\varepsilon_r}{\ln\left(1 + \frac{2h}{t} + \sqrt{\frac{2h}{t}\left(\frac{2h}{t} + 2\right)}\right)}$$

• For narrow lines (w ≤ t/2) Kang & Leblebici Eq. 6.54:

$$C = \frac{\varepsilon_r W}{h} + \frac{\pi \varepsilon_r \left(1 - 0.0543 \frac{t}{2h}\right)}{\ln \left(1 + \frac{2h}{t} + \sqrt{\frac{2h}{t} \left(\frac{2h}{t} + 2\right)}\right)} + 1.47\varepsilon_r$$

Capacitive Coupling

- Fringing fields can terminate on adjacent conductors as well as substrate
- Mutual capacitance between wires implies crosstalk, affects data dependency of power



Miller Capacitance

- Amount of charge moved onto mutual capacitance depends on switching of surrounding wires
- When adjacent wires move in opposite direction, capacitance is effectively doubled (Miller effect)



Data Dependent Switched Capacitance 1

• When adjacent wires move in same direction, mutual capacitance is effectively eliminated

Data Dependent Switched Capacitance 2

 When adjacent wires are static, mutual capacitance is effectively to ground

Remember: it is the *charging* of capacitance where we account for energy from supply, <u>not</u> discharging

Lumped RC Model



- Simplest model used to represent the resistive and capacitive interconnect parasitics
- Propagation delay (same as FET switch model): $t_{PLH} \approx 0.69 RC$

RC T-Model



- Significantly improves accuracy of transient behavior over the lumped RC model
- Useful if simulation time is a bottleneck, much simpler than fully distributed model

Distributed RC Model



• Elmore delay approximation for *RC* ladder network:

$$t_{DN} = \frac{RC}{2}$$

as $N \to \infty$

Repeater Insertion to Reduce Wire Delay



- Insert inverters along long wires at regular intervals
- Breaks up resistance and capacitance, reducing delay dramatically

Summary

- Many important effects to consider in interconnect design
 - Resistance, capacitance, inductance can all affect signal performance
 - Long rise/fall time signals, only resistance and capacitance needs to be considered

• Several models useful for RC interconnect delay analysis

- Simple lumped (1 R, 1 C) model: easy to analyze and/or simulate, will be pessimistic
- -T-model (2 R_{eq} = R/2, 1 C): more accurate than lumped
- Distributed model (N $R_{eq} = R/N$, N $C_{eq} = C/N$): most accurate, use Elmore delay approximation for hand analysis

Next Topic: Design for Manufacturability

- Parameter variations in CMOS digital circuits
- Yield maximization and worst-case design