EEC 118 Lecture #11: CMOS Design Guidelines Alternative Static Logic Families

Rajeevan Amirtharajah
University of California, Davis

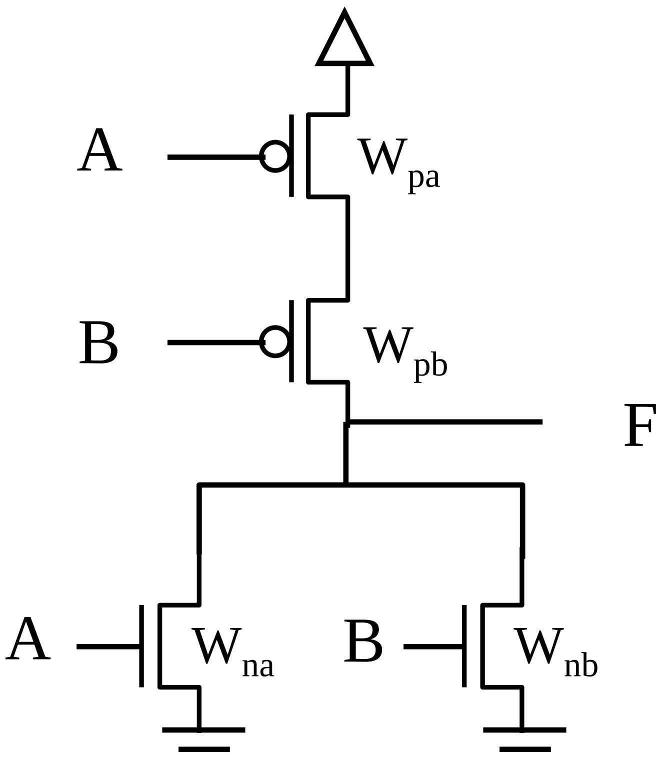
Jeff Parkhurst
Intel Corporation

Outline

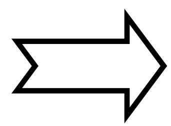
- Finish Arithmetic Discussion
- Review: Static CMOS Sizing
- Design Guidelines for CMOS
- Pseudo-NMOS Logic: Rabaey 6.2
- Pass Transistor Circuits: Rabaey 6.2 (Kang & Leblebici 9.1-9.2)

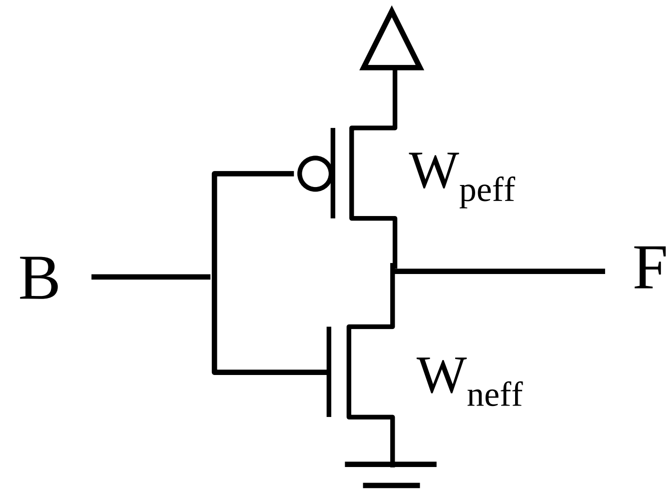
Review: CMOS Sizing

- **Equivalent inverter approach: replace transistors which are "on" with equivalent transistor**
- **Use equivalent inverter to find V_M, delays, etc.**



if A=0,
B switches:





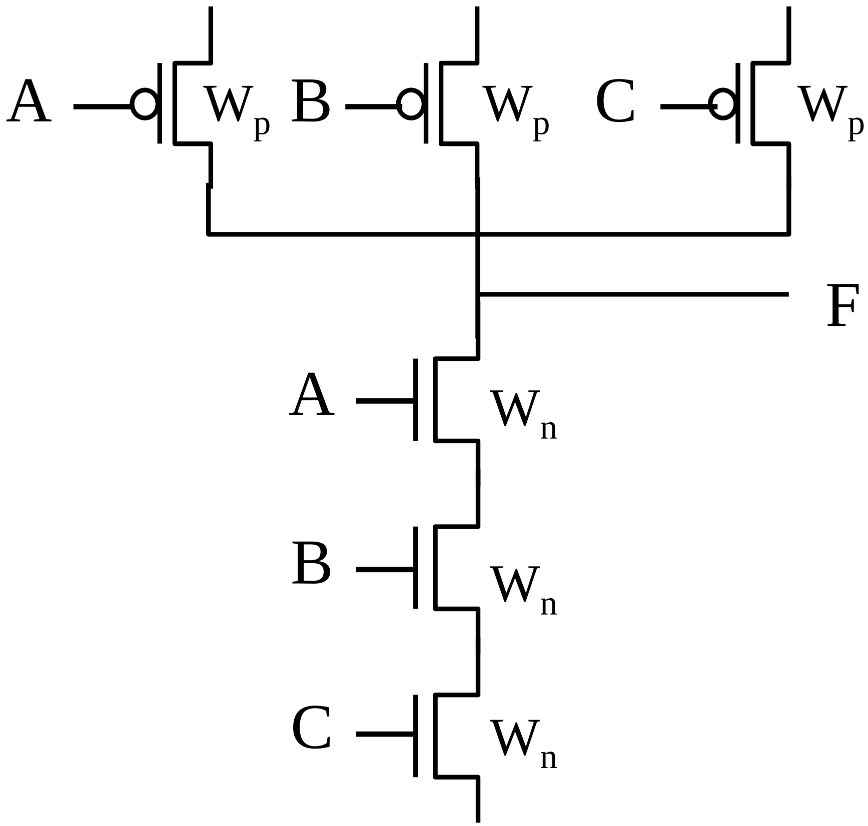
$$\frac{1}{W_{peff}} = \frac{1}{W_{pa}} + \frac{1}{W_{pb}}$$

$$W_{neff} = W_{nb}$$

Review of Sizing

- **Gate delays depend on which inputs switch**
  - Normally sized for worst-case delay
  - Best-case (fastest) delay also important due to race conditions in a pipelined datapath
- **Switching threshold V_M normally considers all inputs switching**
- **Delay estimation**
  - Combine switching transistors into equivalent inverter

Example: NAND gate



- **Circuit:**
  - Load cap C_L=400fF
  - PMOS W/L = 2
  - NMOS W/L = 1
  - k_n' = 200 mA/V^2
  - k_p' = 80 mA/V^2
  - V_T = 0.5V
- **1st: Find delay of inverter**
- **2nd: Find delay of NAND**

Equivalent Inverter

- **Problems with equivalent inverter method:**
  - Need to take into account load capacitance C_L
    - Depends on number of transistors connected to output (junction capacitances)
    - Even transistors which are off (not included in equivalent inverter) contribute to capacitance (i.e. PMOS Drain Capacitance)
  - Need to include capacitance in intermediate stack nodes (NMOS caps). Worst-case: need to charge/discharge all nodes
  - Body effect of stacked transistors

Load Capacitance

- **Output capacitance includes junction caps of all transistors on output**
- **Reducing load capacitance**
  - Minimize number of transistors on output node
  - Tapering transistor stacks:
    - Wider transistors closest to power and ground nodes, narrower at output
    - Transistors closest to power nodes carry more current

Intermediate Node Capacitances

- **Internal capacitances in CMOS gates are charged and discharged**
  – Depends on input pattern
  – Increases delay of gate
- **Simple analysis**
  – Combine internal capacitances into output load
  – Assumes all capacitances charged and discharged fully
- **Effect on delay analysis**
  – Gate delay depends on timing of inputs!

CMOS Design Guidelines I

- **Transistor sizing**
  - Size for worst-case delay, threshold, etc
  - Tapering: transistors near power supply are larger than transistors near output
- **Transistor ordering**
  - Critical signal is defined as the latest-arriving signal to input of gate of interest.
  - Put critical signals closest to output
    - Stack nodes are discharged by early signals
    - Reduced body effect on top transistor

CMOS Design Guidelines II

- **Limit *fan-in* of gate**
  - Fan-in: number of gate inputs
  - Affects size of transistor stacks
  - Normally fan-in limit is 3-4
- **Convert large multi-input gates into smaller chain of gates**
- **Limit *fanout* of gate**
  - Fanout: number of gates connected to output
  - Capacitive load: affects gate delay
- **NANDs are better than NORs**
  - Series NMOS devices less area, capacitance than equivalent series PMOS devices

CMOS Disadvantages

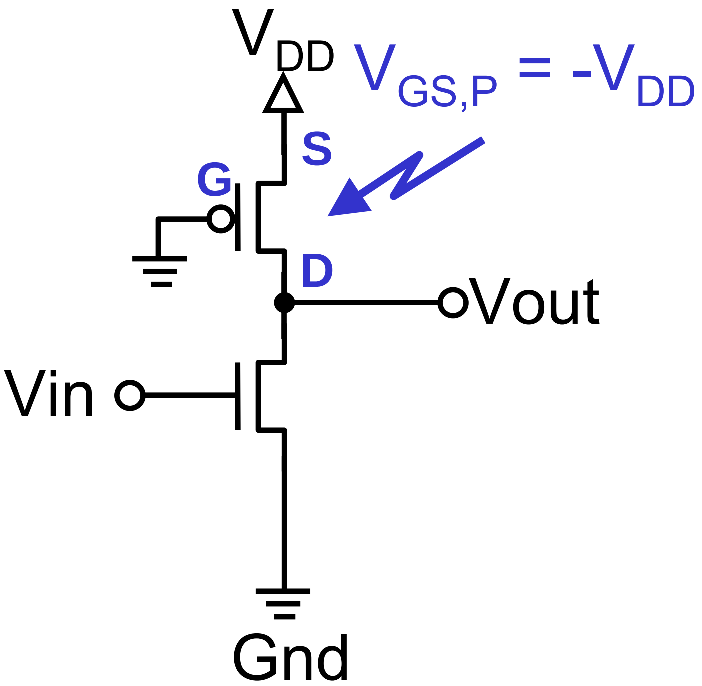
- **For N-input CMOS gate, 2N transistors required**
  - Each input connects to an NMOS and PMOS transistor
  - Large input capacitance: limits fanout
- **Large fan-in gates: always have long transistor stack in PUN or PDN**
  - Limits pullup or pulldown delay
  - Requires very large transistors
- **Single-stage gates are inverting**

Pseudo-NMOS Logic

- **Pseudo-NMOS: replace PMOS PUN with single "always-on" PMOS device (grounded gate)**
- **Same problems as true NMOS inverter:**
  - V_{OL} larger than 0 V
  - Static power dissipation when PDN is on
- **Advantages**
  - Replace large PMOS stacks with single device
  - Reduces overall gate size, input capacitance
  - Especially useful for wide-NOR structures

Pseudo-NMOS Inverter Circuit

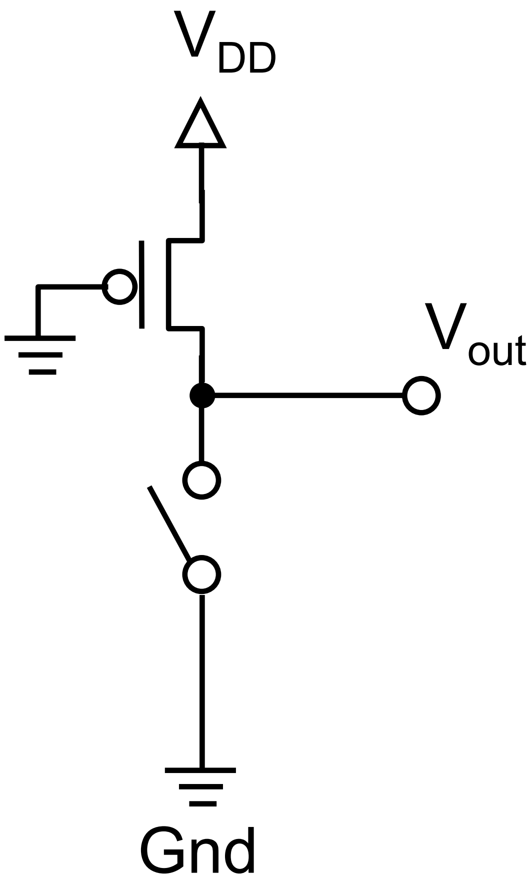
- **Replace PUN or resistor with "always-on" PMOS transistor**
- **Easier to implement in standard process than large resistance value**
- **PMOS load transistor:**
  - On when $V_{GS} < V_{TP} \rightarrow$
    $V_{GS} = -V_{DD}$: transistor always on
  - Linear when $V_{DS} > V_{GS}-V_{TP} \rightarrow$
    $V_{out}-V_{DD} > -V_{DD}-V_{TP} \rightarrow V_{out} > -V_{TP}$
  - Saturated when $V_{DS} < V_{GS}-V_{T} \rightarrow$
    $V_{out}-V_{DD} < -V_{DD}-V_{TP} \rightarrow V_{out} < -V_{TP}$



Remember:
V_T (PMOS) < 0

Pseudo-NMOS Inverter: V_{OH}

- **V_{OH} for pseudo-NMOS inverter:**
  - Vin = 0
  - NMOS in cutoff: no drain current
- **Result: V_{OH} is V_{DD} (as in resistive-load inverter or CMOS inverter case)**



Pseudo-NMOS Inverter: V_{OL}

- **Find VOL of pseudo-NMOS inverter:**
  - $V_{in} = V_{DD}$: NMOS on in linear mode (assume $V_{OL} < V_{DD} - V_{T,n}$)

$$I_{Dn} = k_n\left[\left(V_{DD} - V_{Tn}\right)V_{OL} - \tfrac{1}{2}V_{OL}^2\right]$$

  - PMOS on in saturation mode (assume)

$$I_{Dp} = \tfrac{1}{2}k_p\left(-V_{DD} - V_{Tp}\right)^2 \quad \text{(neglecting } \lambda\text{)}$$

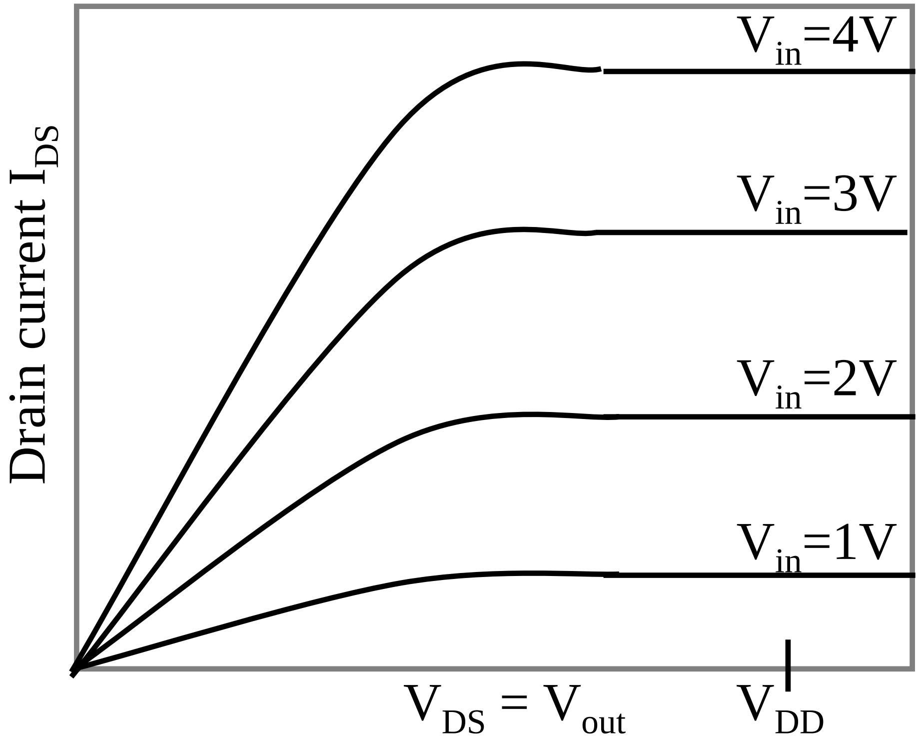
  - Setting $I_{dn} = I_{dp}$:

$$\tfrac{1}{2}k_n V_{OL}^2 - k_n\left(V_{DD} - V_{Tn}\right)V_{OL} + \tfrac{1}{2}k_p\left(-V_{DD} - V_{Tp}\right)^2 = 0$$

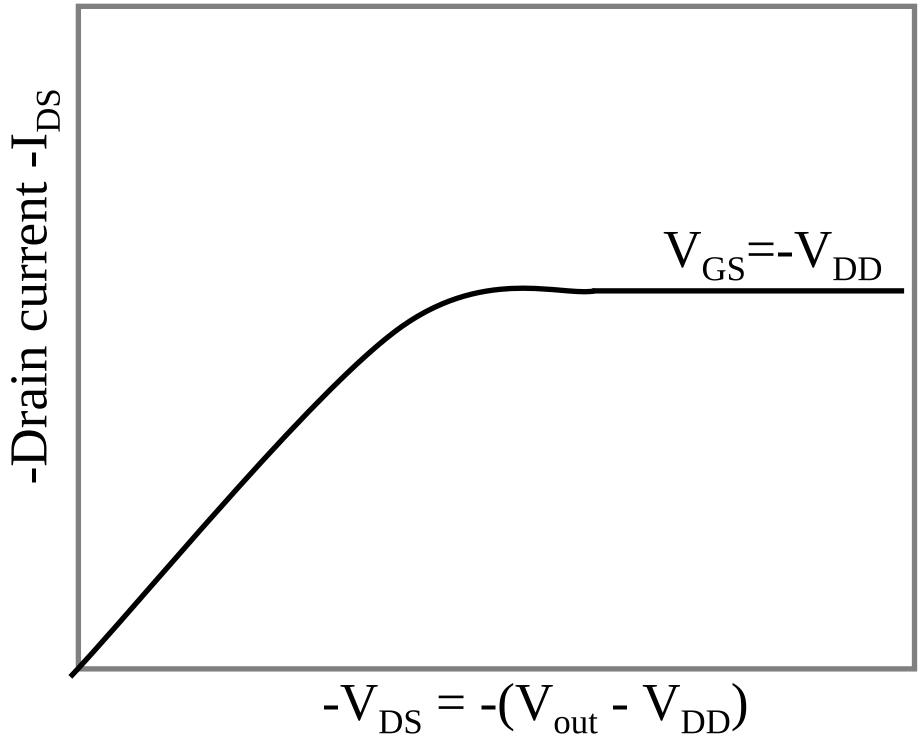
- **Key point: V_{OL} is not zero**
  - Depends on thresholds, sizes of N and P transistors

Pseudo NMOS Inverter: I/V Curves

I/V curve for NMOS:

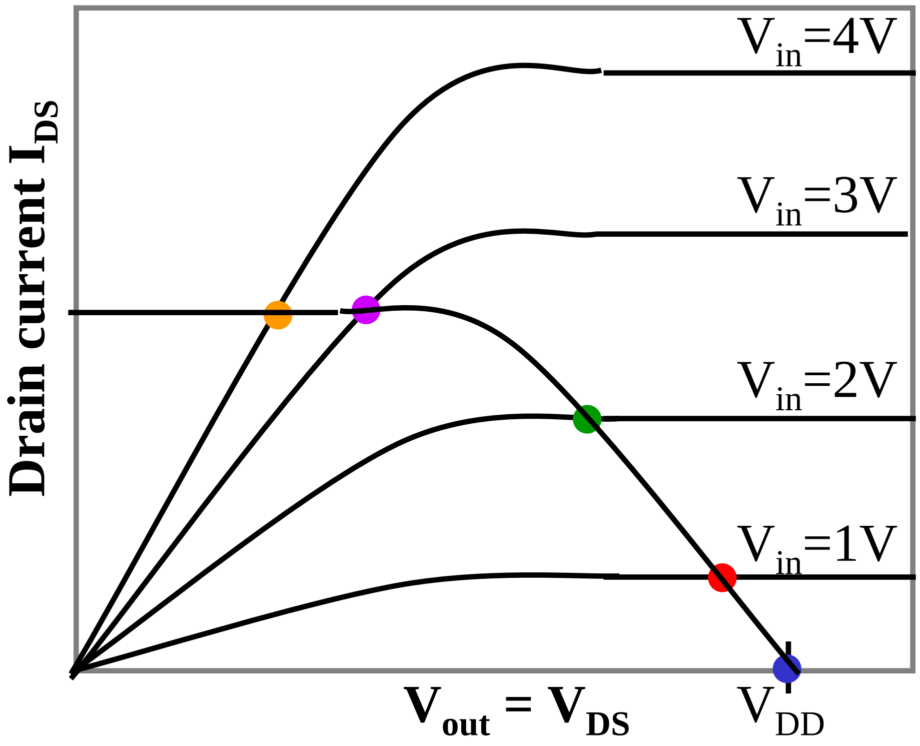


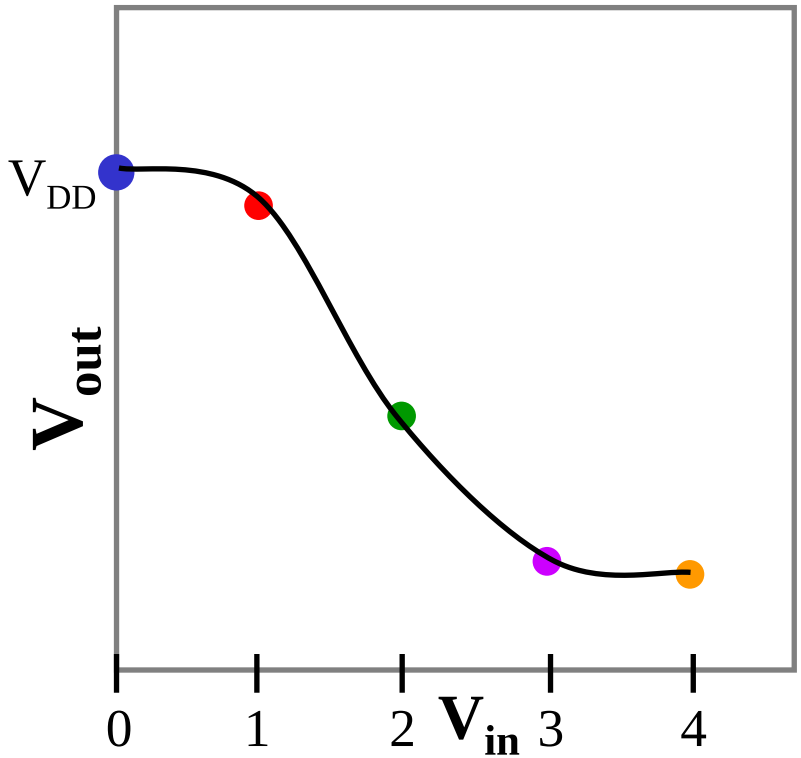
I/V curve for PMOS:



- Plot of $-I_{DS}$ vs $-V_{DS}$ since current is from source to drain
- Only one curve since V_{GS} fixed

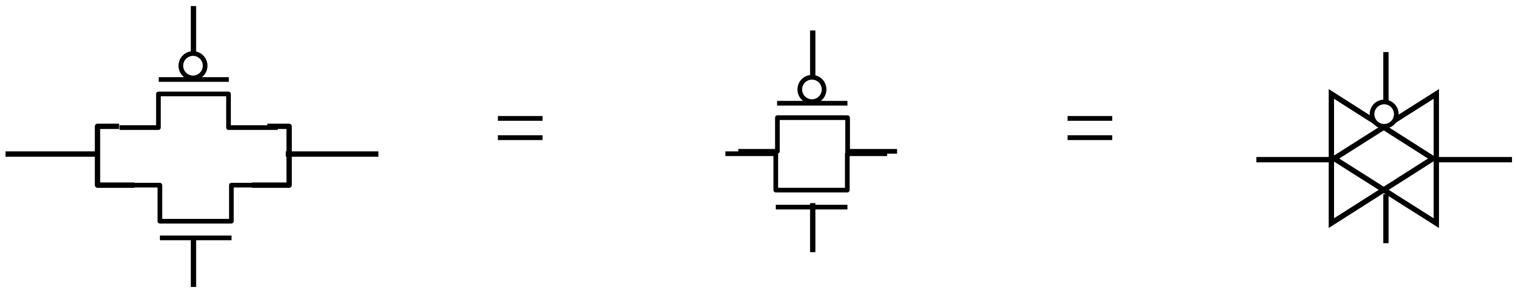
Pseudo NMOS Inverter: VTC





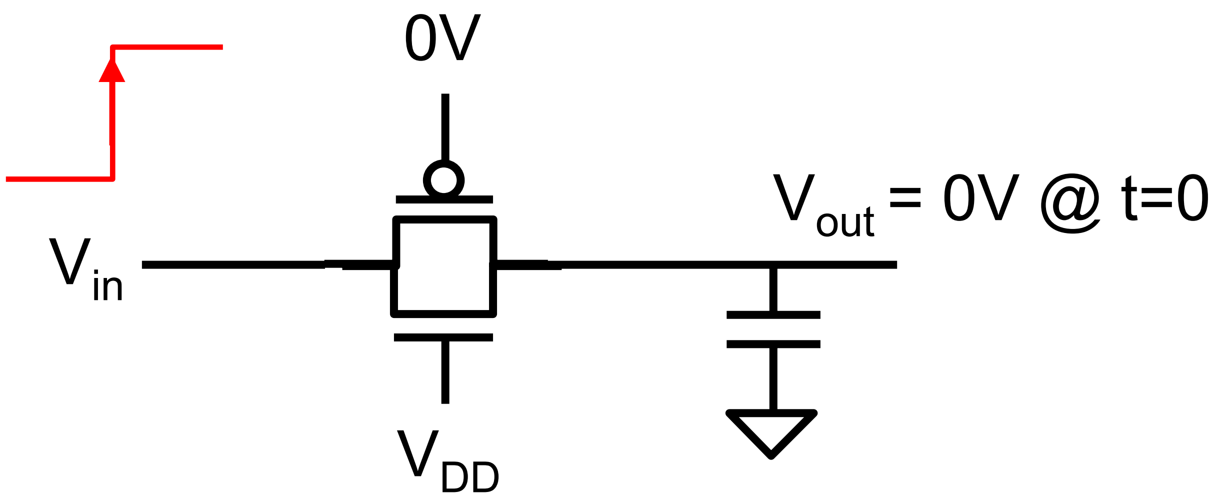
- **Similar VTC to resistive-load inverter**
  - Sharper transition region, smaller area
- **VOL worse than CMOS inverter**

Transmission Gate Logic



- **NMOS and PMOS connected in parallel**
- **Allows full rail transition – ratioless logic**
- **Equivalent resistance relatively constant during transition**
- **Complementary signals required for gates**
- **Some gates can be efficiently implemented using transmission gate logic (XOR in particular)**

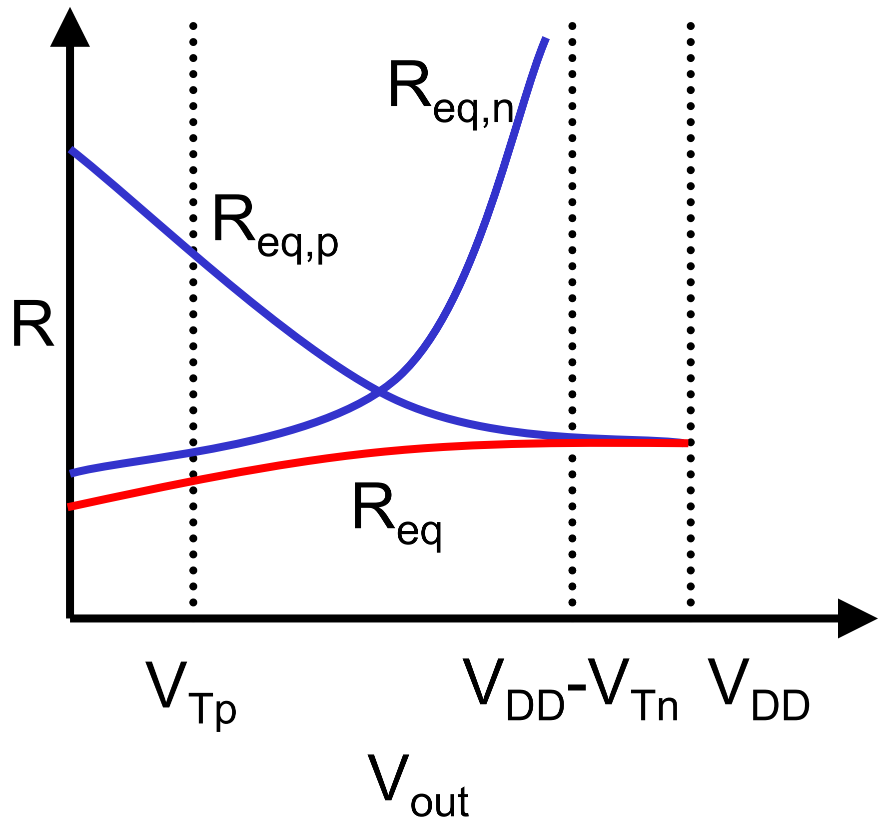
Equivalent Transmission Gate Resistance



- **For a rising transition at the output (step input)**
  - NMOS sat, PMOS sat until output reaches $|V_{TP}|$
  - NMOS sat, PMOS lin until output reaches V_{DD}-V_{TN}
  - NMOS off, PMOS lin for the final $V_{DD} – V_{TN}$ to V_{DD} voltage swing

Equivalent Resistance

- **Equivalent resistance R_{eq} is parallel combinaton of $R_{eq,n}$ and $R_{eq,p}$**
- **R_{eq} is relatively constant**



Resistance Approximations

- **To estimate equivalent resistance:**
  - Assume both transistors in linear region
  - Ignore body effect
  - Assume voltage difference (V_{DS}) is small

$$R_{eq,n} \approx \frac{1}{k_n\left(V_{DD} - V_{tn}\right)} \qquad R_{eq,p} \approx \frac{1}{k_p\left(V_{DD} - \left|V_{tp}\right|\right)}$$

$$R_{eq} \approx \frac{1}{k_n\left(V_{DD} - V_{tn}\right) + k_p\left(V_{DD} - \left|V_{tp}\right|\right)}$$

Equivalent Resistance – Region 1

- **NMOS saturation:**

$$R_{eq,n} = \frac{\left(V_{DD} - V_{out}\right)}{\frac{1}{2}k_n\left(V_{DD} - V_{out} - V_{tn}\right)^2}$$

- **PMOS saturation:**

$$R_{eq,p} = \frac{\left(V_{DD} - V_{out}\right)}{\frac{1}{2}k_p\left(-V_{DD} - V_{tp}\right)^2}$$

Equivalent Resistance – Region 2

- **NMOS saturation:**

$$R_{eq,n} = \frac{(V_{DD} - V_{out})}{\frac{1}{2} k_n (V_{DD} - V_{out} - V_{tn})^2}$$

- **PMOS linear:**

$$R_{eq,p} = \frac{2(V_{DD} - V_{out})}{k_p\left(2(V_{DD} - |V_{TP}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2\right)}$$

$$= \frac{2}{k_p\left[2(V_{DD} - |V_{TP}|) - (V_{DD} - V_{out})\right]}$$

Equivalent Resistance – Region 3

- **NMOS cut off:**

$$\boldsymbol{R_{eq,n} = \infty}$$

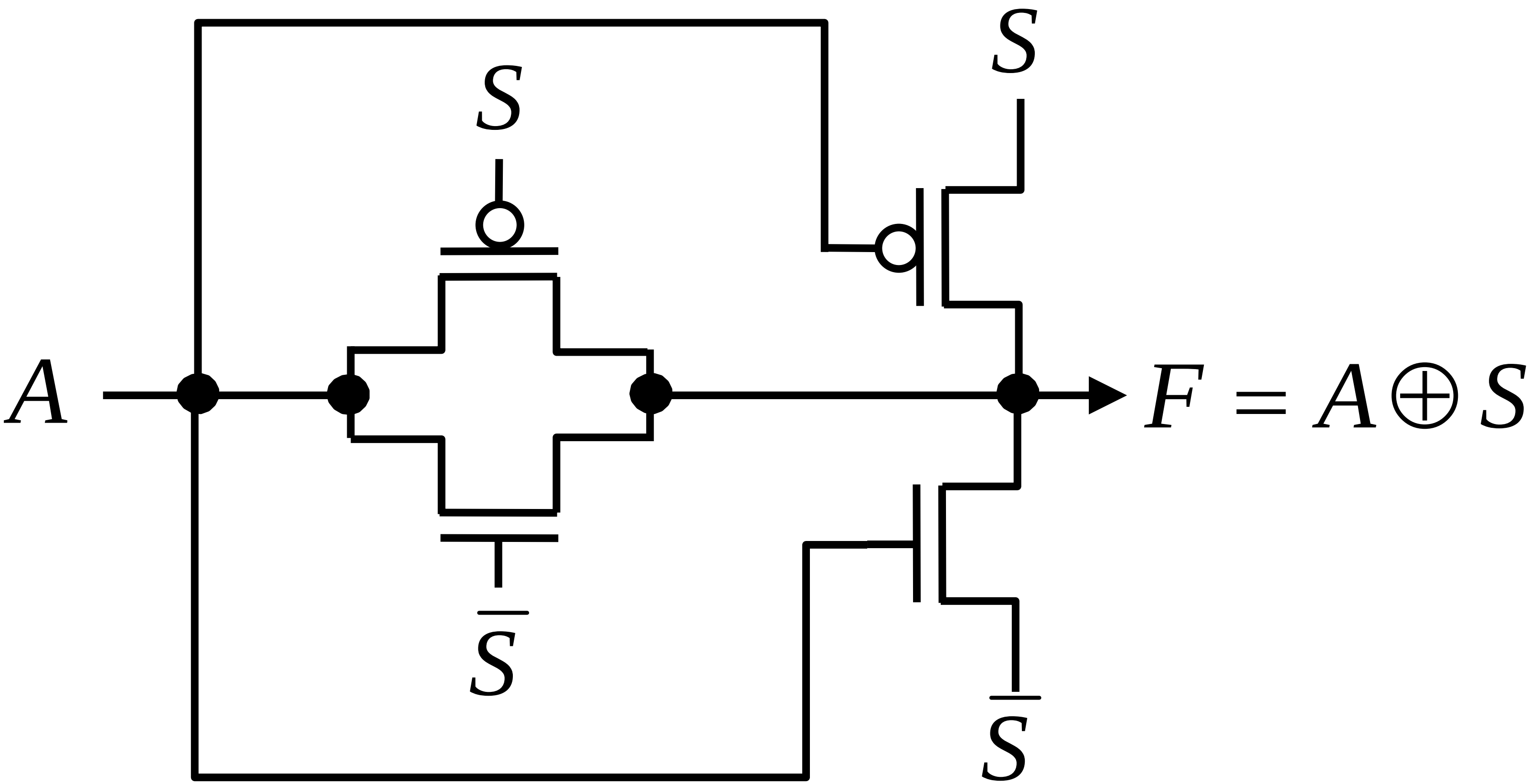
- **PMOS linear:**

$$R_{eq,p} = \frac{2}{k_p\left[2\left(V_{DD} - |V_{TP}|\right) - \left(V_{DD} - V_{out}\right)\right]}$$

Transmission Gate Logic

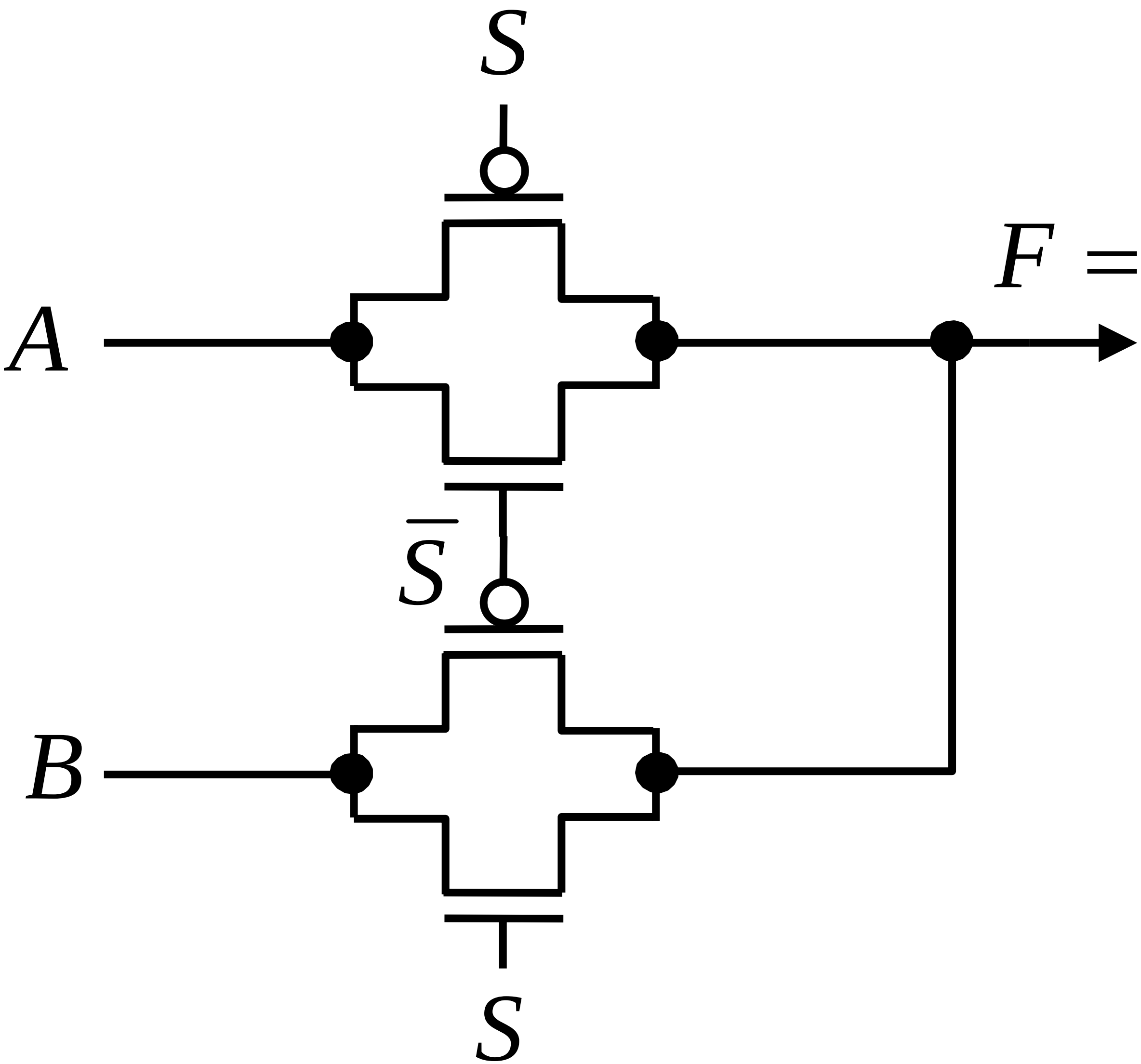
- **Useful for multiplexers (select between multiple inputs) and XORs**
- **Transmission gate implements logic function F = A if S**
  - If S is 0, output is floating, which should be avoided
  - Always make sure one path is conducting from input to output
- **Only two transmission gates needed to implement $A\overline{S} + \overline{A}S$**
  - Transmission Gate 1: A if $\overline{S}$
  - Transmission Gate 2: $\overline{A}$ if S

Transmission Gate XOR



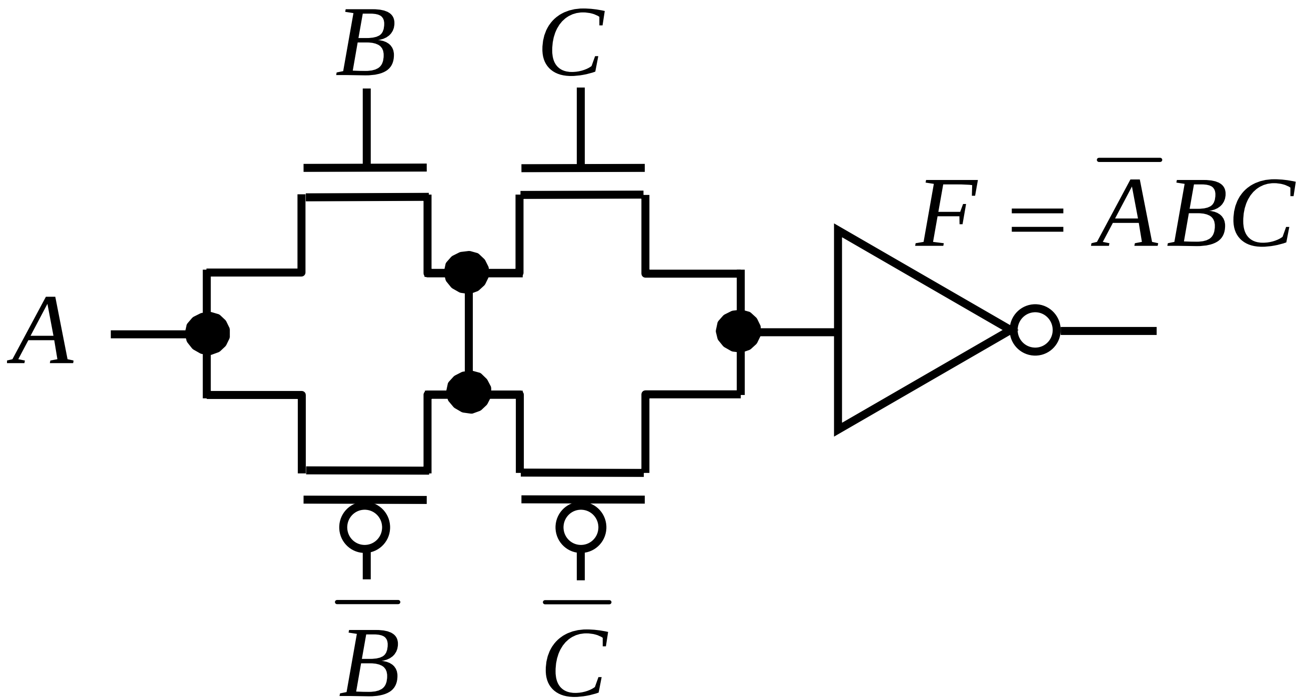
- **If S = 0, F = A and when S = 1, F = ~A**

Transmission Gate Multiplexer



$F = A\overline{S} + BS$

Full Transmission Gate Logic



- PMOS devices in parallel with NMOS transistors pass full V_{DD} (only one logic path shown above)
- Requires more devices, but each can be sized smaller than static CMOS
- Output inverter reduces impact of fanout

Next Topic: Dynamic Circuits

- **Extend dynamic sequential circuit idea to logic circuits**
  - Improved speed
  - Reduced area
  - Challenging to design: timing and noise issues, charge sharing, leakage
  - Preferred design style for high performance circuits