

# EEC 118 Spring 2010 Lab #3 Part 2:

## D Flip-Flops

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**Reading:** Rabaey 7.1-7.3 [1].

**Reference:** Kang and Leblebici Chapters 4, 5, and 8 [2].

## I OBJECTIVE

In this experiment, you will build a dynamic and a static D-type flip-flop out of inverters and transistors. Due to the high threshold voltage of the CD4007 transistors, a 15V power supply is used.

## II DYNAMIC MOS FLIP-FLOP

**Step 1** Build the circuit in Figure 1 using the pin connections shown (the pin numbers are circled). Use  $C=1000$  pF,  $V_{DD} = 15V$ , and  $V_{SS} = 0V$ . Be sure to connect pin 14 of the CD4007 to +15V and pin 7 to GND.

Construction tip: A suggested board layout is shown in Figure 2. Place an extra 4007 below the 4049; it will be used in Section III. You will eventually have on your protoboard a 4007, 4049, and 4007, preferably in that order (to simplify wiring). For Section II, use the upper 4007 (U1) and the 4049 (U2) to build the dynamic flip-flop. The lower 4007 (U3) will be used in Section III.

**Step 2 (20 points)** Verify that the circuit operates as a flip-flop by connecting the  $D$  input to the  $\overline{Q}$  output. With this connection, the circuit operates as a T flip-flop, and the output of the flip-flop will be the clock divided by 2. Try using a 10 kHz square wave that goes from 0 to 15 V for the clock (CLK). If the circuit does not work as expected, try increasing the clock voltage (why does increasing the voltage help?) until it starts working. Use  $C=1000$  pF. Sketch the CLK,  $\overline{M}$ , and  $Q$  waveforms. At what part of the clock waveform is the  $D$  input latched? Increase the CLK frequency to determine the maximum clock frequency for which the T flip-flop operates. (**NOTE:** If your clock generator can only output a 10 V square wave, you can connect the 10 V square wave to the input of a 4049 inverter with  $V_{DD} = 15$  V. It should output a 15 V or higher voltage square wave that you can use as



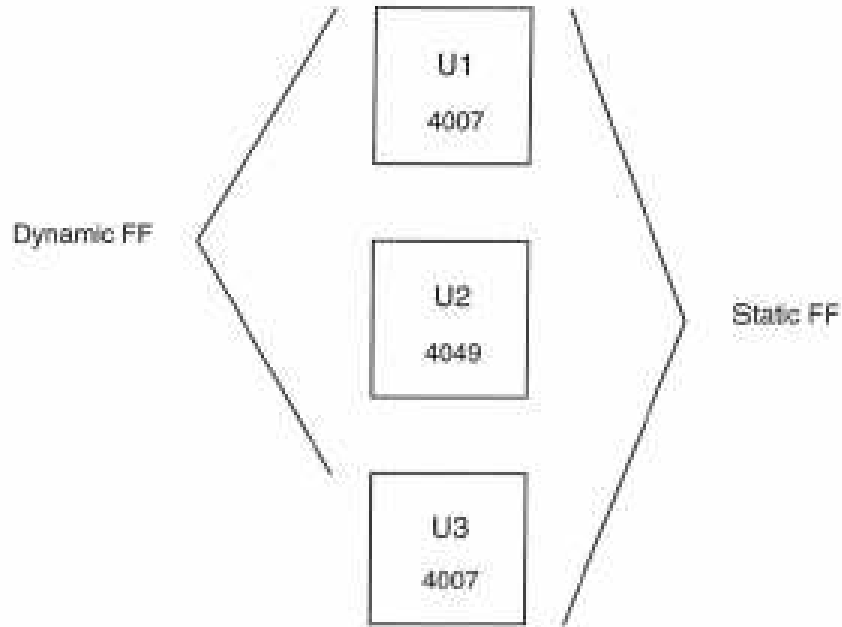


Figure 2: Suggested board layout.

the clock. If necessary, increase the DC voltage of the 10 V square wave to improve the symmetry of the output square wave.)

**Step 3 (10 points)** Tie the  $D$  input high (connect it to  $V_{DD}$ ). Sketch the clock CLK and the waveforms at nodes  $D$ ,  $Q$ ,  $X$ , and  $Y$ . Use the clock as the trigger signal for observing these waveforms. Explain the waveforms and voltage levels.

**Step 4 (10 points)** Repeat Step 3 with the  $D$  input low (connect it to GND).

**Step 5 (10 points)** With the  $D$  input grounded, reduce the clock frequency until you see significant droop in the voltage at node  $Y$ . (This clock frequency should be on the order of 1 kHz). Continue to decrease the clock frequency until the droop is large enough to cause 'glitches' in the  $Q$  output. Sketch the CLK,  $Y$ , and  $Q$  waveforms.

**Step 6 (10 points)** Change  $C$  at nodes  $X$  and  $Y$  from 1000 pF to 100 pF. Record the clock frequency at which significant droop appears at node  $Y$  (and glitches appear in the  $Q$  output). Repeat this measurement with  $C=10$  pF.

### III STATIC MOS D FLIP-FLOP

**Step 7** Add the extra circuit shown in Figure 3 that will convert the dynamic flip-flop in Figure 1 to a static flip-flop. Use the available inverters in U2. Add U3, another CD4007, and connect its pin 14 to +15 V and pin 7 to GND.

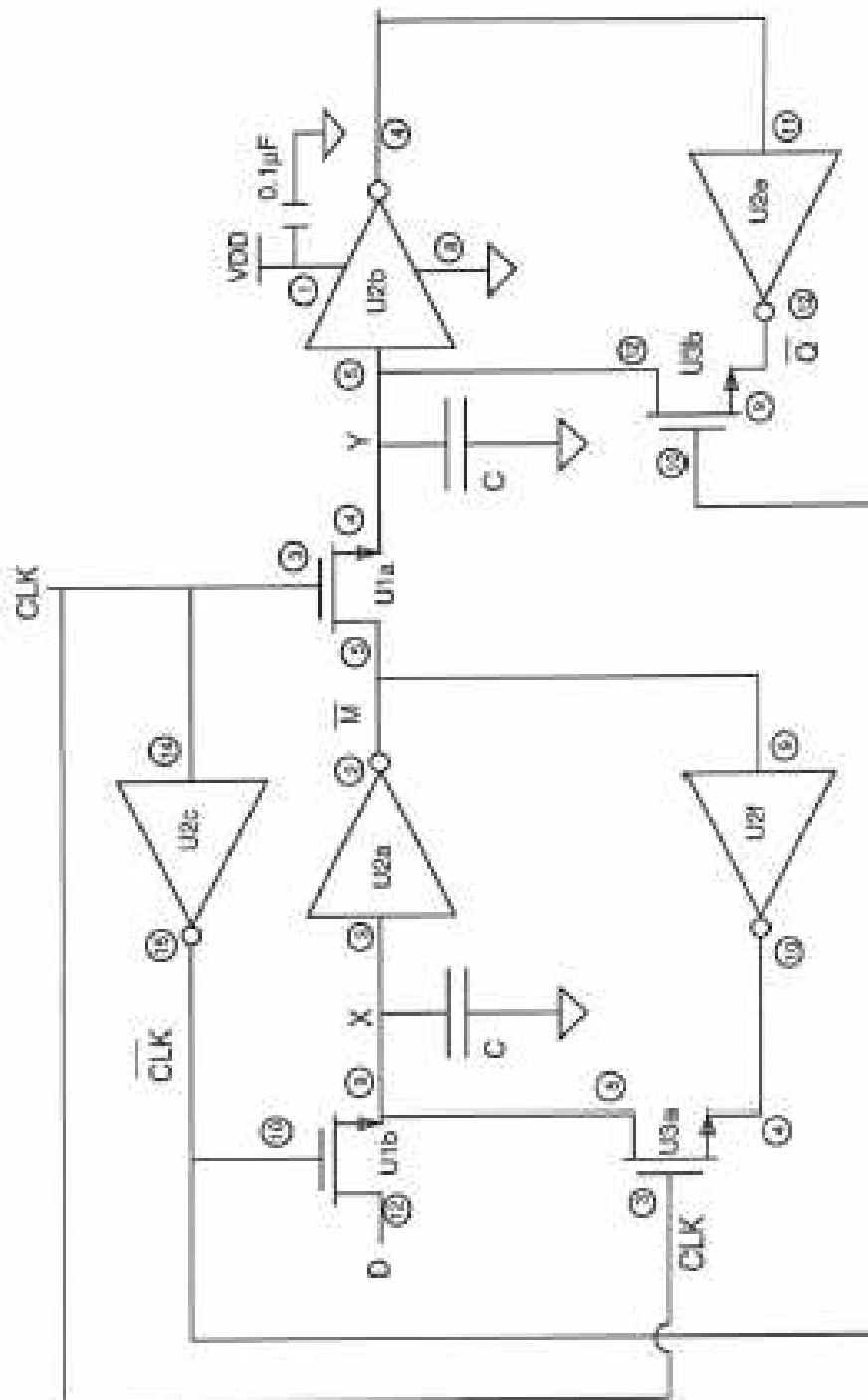


Figure 3: Static MOS D Flip-Flop schematic diagram.

**Step 8 (20 points)** Verify that the circuit operates as a flip-flop by connecting the  $D$  input to the  $\overline{Q}$  output to build a T flip-flop. Use a 10 kHz square wave that goes from 0 to 10 V for the clock (CLK). If the circuit does not work as expected, try increasing the clock voltage again until it starts working. Use  $C=1000$  pF. Sketch the CLK,  $\overline{M}$ , and  $Q$  waveforms. At what part of the clock waveform is the  $D$  input latched? Increase the CLK frequency to determine the maximum CLK frequency for which the T flip-flop operates.

**Step 9 (10 points)** Tie the  $D$  input low. Use  $C=1000$  pF. Slow the clock to the same frequency recorded in Step 5 above. Do you see the droop at node  $Y$ ? Try a lower frequency. Do you see droop at node  $Y$ ? Try  $C=10$  pF. Do you see droop at node  $Y$ ? Why or why not?

**Step 10 (10 points)** What are the advantages and disadvantages of the static D flip-flop?

## References

- [1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.
- [2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.