EEC 118 Spring 2010 Lab #3 Part 1: Simulating D Flip-Flops

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Reading: Rabaey 7.1-7.3 [1].
Reference: Kang and Leblebici Chapters 4, 5, and 8 [2].

Simulation: This lab requires extensive use of HSPICE. For information on running HSPICE on the UCD ECE department network, follow this URL:

`http://www.ece.ucdavis.edu/support/software/hspice/`

If you want to use another version of Spice (e.g. PSpice, Berkeley Spice, Spectre), you must get permission from the instructor first.

Device Models: This lab relies on freeware models from the Berkeley Device Group [3, 4]. Download the model file `130nm_nominal.sp` from the course web site and include it in your Spice deck.

I OBJECTIVE

The objective of this experiment is to gain experience with Hspice by simulating the Voltage Transfer Characteristic (VTC) of a CMOS inverter and to build and simulate CMOS circuits for sequential elements.

II PRELAB

Problem 1 (10 points) Draw a circuit schematic for a CMOS inverter, labeling the input **in** and the output **out**. Download and edit the spice deck template `lab3pt1.sp` from the course web page to implement the inverter. You may use the template for the inverter macro if you need to instantiate the inverter multiple times for this lab. Choose a width for the PMOS and NMOS to yield a switching threshold of $V_M = V_{DD}/2$ for the inverter, based on what you typically assume for carrier mobilities μ_n and μ_p. Be sure to include tha source/drain area and perimeter junction capacitances in your code. Use the layout for a

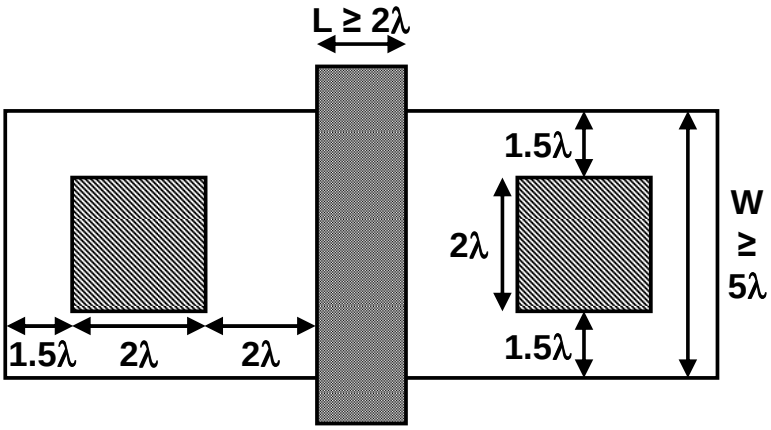

Figure 1: Minimum sized transistor layout with minimum length L and width W labeled.

minimum size transistor in Figure 1 as a guide. λ equals 65 nm for a 130 nm process and $V_{DD} = 1.2$V.

III VOLTAGE TRANSFER CHARACTERISTIC

Part 1 (20 points) Simulate the Voltage Transfer Characteristic for the inverter you design from the Prelab, using a DC sweep analysis for v_{in}, the inverter input voltage. Confirm that $V_M = V_{DD}/2$, as specified in the Prelab. If it doesn't, adjust the transistor widths until the design satisfies the specification. Record the device W/L ratios for your lab report. Turn in a plot of the VTC from your simulation, with V_M labeled, along with a printout of your Hspice code.

Part 2 (20 points) Resize the transistors in your inverter to achieve $V_M = 0.4V_{DD}$ and $V_M = 0.6V_{DD}$. Record the device W/L ratios for your lab report. Turn in a plot of the two additional VTCs from your simulation, with V_M labeled, along with a printout of your Hspice code.

IV DYNAMIC MOS FLIP-FLOP

Part 3 (10 points) The dynamic D Flip-Flop configuration shown in Figure 2 is often used in high speed digital circuits to store data. Implement the circuit in Hspice using the inverter with $V_M = V_{DD}/2$ designed above in Step 1. Use the 130 nm transistor models from above, $V_{DD} = 1.2$V, and $C_0 = C_1 = 1$ fF for the capacitors. Try to minimize the total area of the transmission gate transistors in your implementation.

Part 4 (20 points) Verify the operation of the flip-flop by wiring the $\overline{Q}$ output to the input D. In this configuration, the flip-flop acts as a T flip-flop, and the output Q will be the clock divided by 2. To accurately simulate the flip-flop under realistic loading conditions, connect the inputs of 4 inverters to each of the Q and $\overline{Q}$ flip-flop outputs. This loading condition

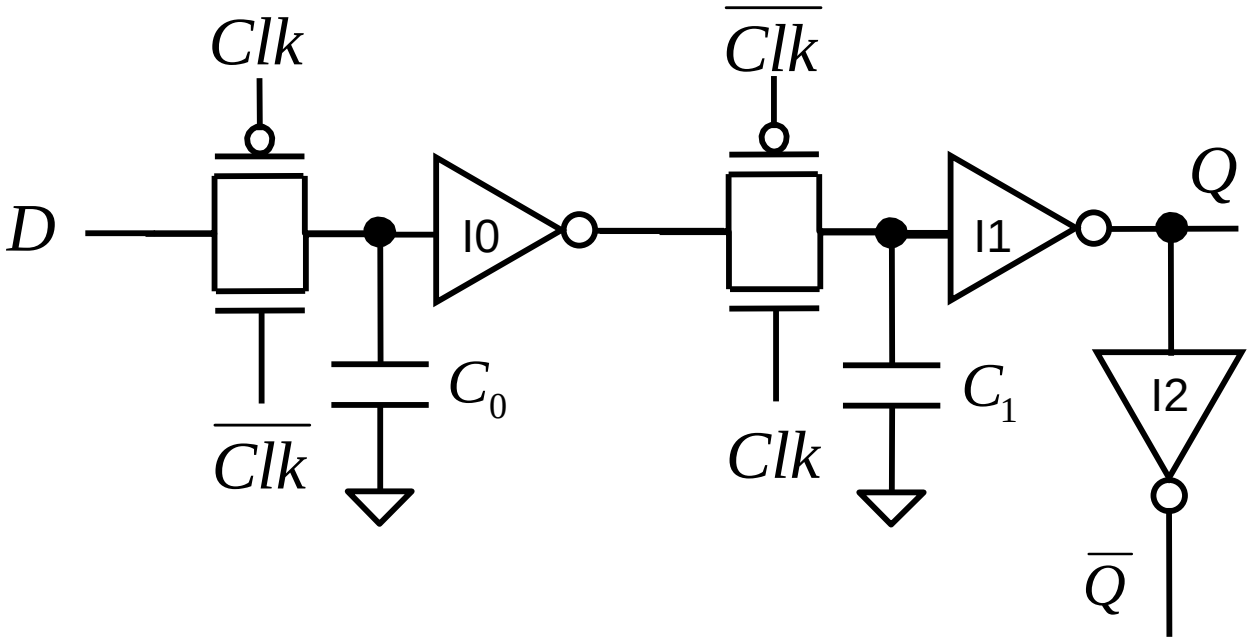

Figure 2: Dynamic D Flip-Flop with Complementary Outputs.

is called a **fanout** of four (**FO4**) and is often used as a standard load to measure transient parameters such as rise and fall times. Also, make sure that both the Clk and $\overline{Clk}$ inputs are driven by inverters instead of voltage sources, to accurately reflect the output impedance of a realistic clock buffer. Simulate the flip-flop with a clock frequency of 1 GHz. Turn in a plot of 10 clock cycles showing your flip-flop operating correctly, along with your Hspice code.

Part 5 (20 points) Increase the size of the internal load capacitances from 1 fF to 10 fF and 25 fF. How does increasing the capacitances affect the output voltage levels and timing? What are the advantages and disadvantages of increasing the capacitance? Turn in a plot of 10 clock cycles showing the flip-flop operation for these two values of capacitance, along with your Hspice code.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.

[3] Device Group at UC Berkeley. (2002, July) Predictive technology model: Mosfet. download.html. [Online]. Available: http://www-device.eecs.berkeley.edu/ ptm/

[4] Y. Cao, T. Sato, D. Sylvester, M. Orshansky, and C. Hu, "New paradigm of predictive MOSFET and interconnect modeling for early circuit design," in *Proc. of the IEEE CICC*, June 2000, pp. 201–4.