EEC 118 Final Project Spring 2010
Design a 5x4 bit Pipelined Multiplier

The purpose of this project is to have you design a small project and familiarize yourself with circuit design issues such as speed and performance.

Parameters/Goals:

Minimum Clock Frequency: 1.0 GHz

Objective: Design a 5x4 bit multiplier. You should work in groups of 2 (or 3 if given permission). Assume a 100 ps rise and fall time at the input and a fanout of four (FO4) minimum-sized inverters load on the output register signal lines. Use the transistor models for the 130 nm CMOS example process from Lab 3 Part 1, with V_{DD} = 1.2 V.

Design Parameter	Goal	Actual
Max Clock Frequency	> 1.0 GHz	
Noise Margin	> 1V	
Rise/Fall Time	< 250 ps	
Power	< 20 mW	
Area	N/A	

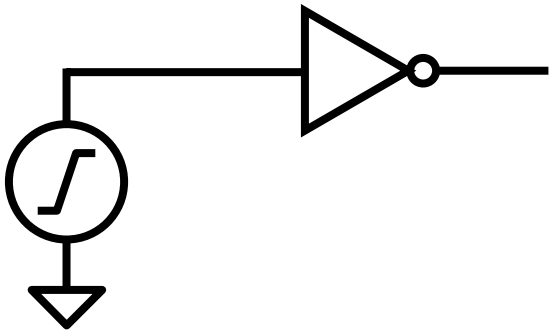
PROJECT SPECIFICS: The pipelined multiplier sits between two pipeline register stages. It is strongly suggested that you should use static CMOS logic.

POWER SUPPLY: A power supply of 1.2 V should be used. Measure and report the power consumption from Hspice simulations.

PERFORMANCE METRIC: Maximum clock frequency can be determined by decreasing the clock period to the point that the multiplier begins to skip incrementing every clock cycle. You can use this method to find the smallest clock period or maximum clock frequency.

V_{OH}, V_{OL}, NOISE MARGINS: The noise margins should be at least be 1V. Test this by running VTC curves for the register as well as any full and half adder circuits. Hint: You can do this by testing the master and slave latches of the flip-flops independently while the clock input is set to make the latch transparent.

INPUT BUFFERS: To realistically simulate input waveforms, input signals and clocks from voltage sources in Hspice should be buffered by passing through a CMOS inverter with V_{TH} = $V_{DD}/2$, as shown in the figure below. All inputs and clocks to the multiplier should have rise and fall times of 100 ps or less, which may require larger than minimum sizes for the CMOS inverter if it is driving a large capacitive load such as the clock line.



RISE AND FALL TIMES: All input signals and clocks at the output of the CMOS inverter driver have rise and fall times of 100 psec. The rise and fall times of the output signals (10% to 90%) should not exceed 250 psec.

LOAD CAPACITANCE: Each output bit of the register should have a **fanout of four (FO4) minimum-sized inverters load.**

NETLIST: Email your SPICE netlist to the the TA and turn in a hardcopy when you hand in your design project report. You must use the subcircuit templates (finalproject.sp) from the web page so that a consistent interface is presented to the test bench. Name your file <last name #1>_<last name #2>_finalproject.sp, with the last names in alphabetical order.

QUESTIONS: In addition to the usual sections, be sure to answer the following in your final project report:

1. How does the **highest** clock frequency your multiplier runs at compare to the clock frequency you calculated in Design Project Part 2? Explain any discrepancies between the calculated and simulated numbers.

2. Most modern digital chips have very wide datapaths (64 or 128 bits). Is your multiplier design (scaled up) a good choice for a 128 bit multiplier? Why or why not?

I cannot overemphasize the importance of tabulating your results. It is very difficult to grade when I have to look all over the report to find data.