EEC 118 Spring 2010 Homework #7

Rajeevan Amirtharajah
Dept. of Electrical and Computer Engineering
University of California, Davis

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Due: N/A.

Reading: Rabaey Chapters 12.1-12.2 [1].
Reference: Kang and Leblebici Chapters 10.1-10.5 [2].

1 Single Transistor DRAM

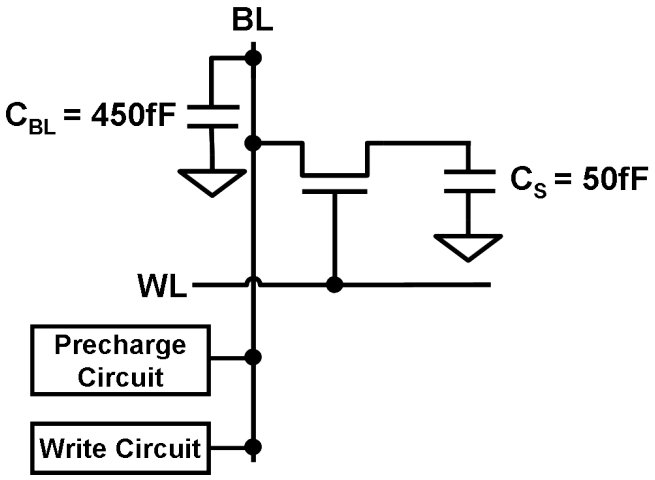

Figure 1: Two input domino-style dynamic logic NAND gate.

Consider the single transistor (1T) DRAM cell circuit shown in Figure 1 that includes peripheral circuits which precharge the bitline **BL** during read operations and drive the bitline to 0V or V_{DD} during write operations. Assume the following parameters for the NMOS access transistor:

- $W/L = 1$
- $V_{T0,n} = 1.0$V

- $\mu_n C_{ox} = 100\mu\text{A/V}^2$
- $\gamma = 0.3\text{V}^{\frac{1}{2}}$
- $\lambda = 0.0\text{V}^{-1}$
- $|2\Phi_F| = 0.6\text{V}$

Problem 1.1 When writing a logical 1 into the DRAM cell, assume that the Write Circuit maintains the bitline at $V_{DD} = 5\text{V}$ when the wordline **WL** is asserted and driven to V_{DD}. What is the final voltage written onto the DRAM cell storage capacitor?

Problem 1.2 When reading a logical 1 from the DRAM cell, assume that the Precharge Circuit precharges the bitline to $V_{DD}/2$ where $V_{DD} = 5\text{V}$. When the wordline **WL** is asserted and driven to V_{DD} during the read, what is the final voltage driven onto the bitline?

2 SRAM Cell Design

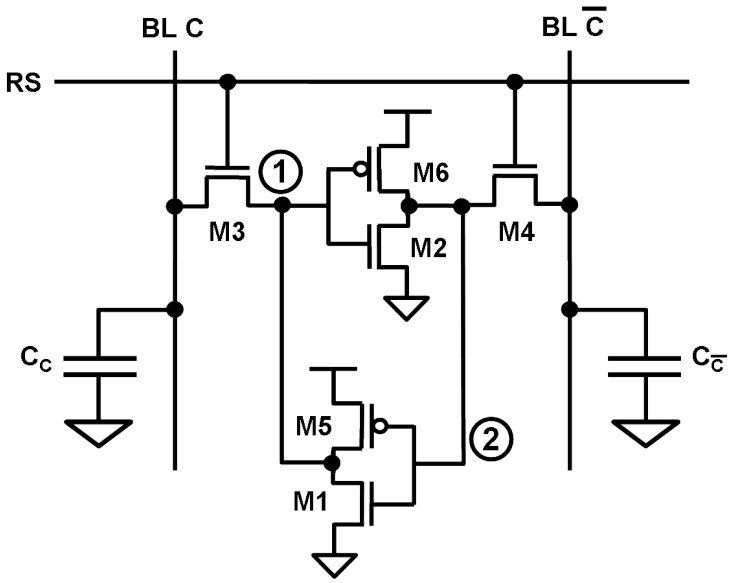

Figure 2: SRAM circuit.

Consider the SRAM cell circuit shown in Figure 2. Assume the following parameters for the transistors and other elements in the circuit:

- $V_{DD} = 5\text{V}$
- $V_{T0,n} = 0.7\text{V}$
- $\mu_n C_{ox} = 50\mu\text{A/V}^2$

- $V_{T0,p} = -0.7\text{V}$
- $\mu_p C_{ox} = 25\mu\text{A/V}^2$
- $\gamma = 0.4\text{V}^{\frac{1}{2}}$
- $\lambda = 0.0\text{V}^{-1}$
- $|2\Phi_F| = 0.6\text{V}$
- For M1 and M2: $W/L = 4/4$
- For M3 and M4: $W/L = 2/4$

Problem 2.1 During a write operation, we want to ensure that the state of the SRAM cell can be changed when the voltage on the bitline $V_C \leq 0.5\text{V}$. Choose W/L ratios for transistors M5 and M6 to guarantee this write condition assuming that both PMOS devices must have the same W/L ratio.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.