EEC 118 Spring 2010 Homework #6

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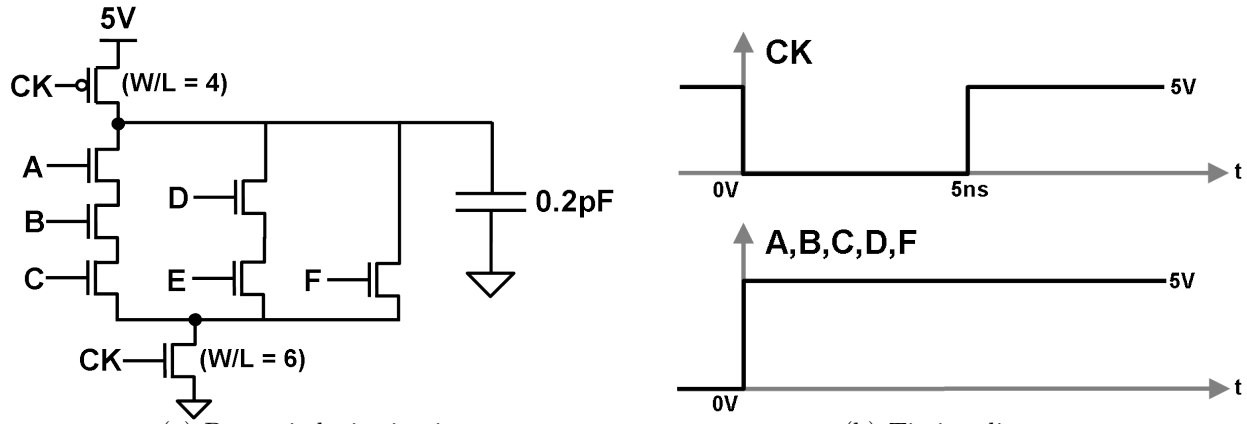
Reading: Rabaey Chapters 6.3 [1].
Reference: Kang and Leblebici Chapters 9.4-9.6 [2].

1 Dynamic Logic Circuit



(a) Dynamic logic circuit. (b) Timing diagram.

Figure 1: (a) Five input dynamic logic circuit and load capacitance. (b) Input and clock waveforms.

Consider the CMOS circuit shown in Figure 1(a) that was designed to drive a total capacitive load of $C_L = 0.2$pF. For the n-channel and p-channel transistors, assume the parameters below and the dimensions shown in the figure:

- Pull-down transistors $W/L = 9$
- $V_{T0,n} = 1.0$V
- $\mu_n C_{ox} = 50\mu$A/V^2

- $V_{T0,p} = -1.0\text{V}$
- $\mu_p C_{ox} = 25\mu\text{A/V}^2$
- $\lambda = 0.0\text{V}^{-1}$

Problem 1.1 The initial voltage across the load capacitor C_L is 0V. The waveform at input E is 0V for all time. For the clock CK and the rest of the inputs, the waveforms are shown in Figure 1(b). Sketch the voltage waveform across the load capacitor C_L and provide clear marking of the 50% crossings along the time axis in nanoseconds for both rise and fall transitions. Hint: Approximate the entire pull-down network by a single equivalent n-channel transistor and use the average current method at the initial and 50% voltage points to compute the required delay times.

2 Domino Two Input NAND Gate

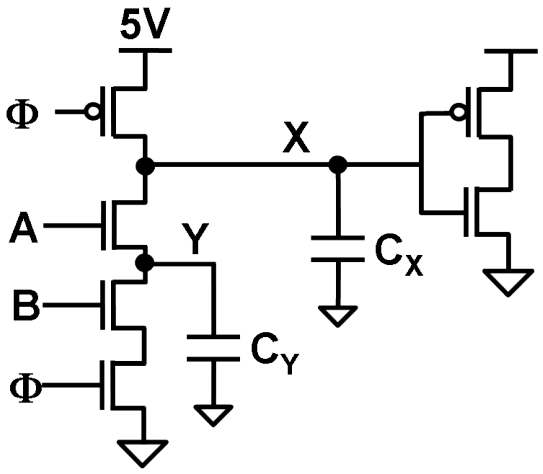


Figure 2: Two input domino-style dynamic logic NAND gate.

Consider the CMOS dynamic logic circuit shown in Figure 2, which is a simple domino circuit. Node X is connected to a CMOS inverter so that the output of the inverter can be directly fed to the next stage of the domino circuit.

Problem 2.1 Explain how the voltage level at node X, after it is precharged to 5V, can be affected by the charge sharing between node X and node Y if their node capacitances are the same. Express the final voltage at node X in terms of the initial voltage at node Y when the charge sharing is completed, following the full precharge operation when input B is fixed at 0V.

Problem 2.2 Determine the ratio between device transconductance parameters, k_p and k_n, of the inverter to prevent any logic error due to charge sharing between nodes X and Y under all circumstances. Assume that the magnitudes of the threshold voltages in the inverter are equal to 1.0V.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.