EEC 118 Spring 2009 Homework #5

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Reading: Rabaey Chapters 6.2 and 7.1-7.3 [1].
Reference: Kang and Leblebici Chapters 7 and 8 [2].

1 Enhancement Load Logic Circuit

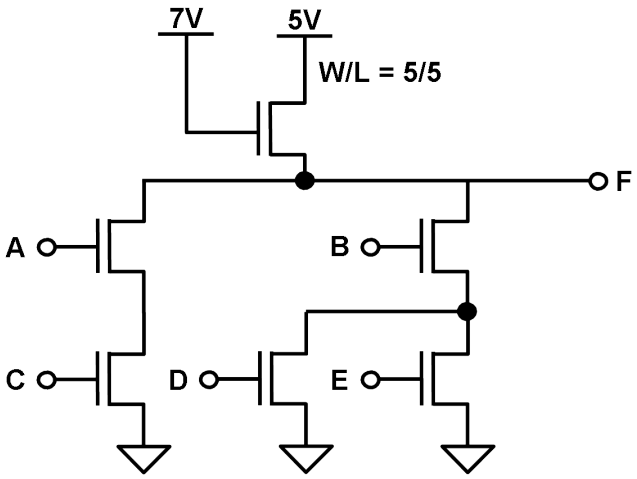

Figure 1: NMOS enhancement load complex gate.

For the enhancement load logic gate shown in Figure 1,

- Pull-up transistor $W/L = 5/5$
- Pull-down transistors $W/L = 100/5$
- $V_{T0,n} = 1.0\text{V}$
- $\lambda = 0.0\text{V}^{-1}$

- $\mu_n C_{ox} = 100\mu\text{A/V}^2$
- $\gamma = 0.4\text{V}^{1/2}$
- $|2\phi_F| = 0.6\text{V}$

Problem 1.1 Write a Boolean expression for the output F as a function of the inputs.

Problem 1.2 Identify the worst-case input combination(s) for V_{OL}.

Problem 1.3 Calculate the worst-case value of V_{OL}. Assume that all pull-down transistors have the same body bias and that, initially, $V_{OL} \approx 5\%$ of $V_{DD} = 5\text{V}$.

Problem 1.4 Does the value of V_{OL} depend on $k_n = \mu_n C_{ox}$? Explain why or why not.

2 Two Input CMOS NOR Gate

Problem 2.1 Calculate V_{OL}, V_{OH}, V_{IL}, V_{IH}, NM_L, and NM_H for a two input CMOS NOR gate. Assume for the transistors the following parameters: $V_{T0,n} = 0.7\text{V}$, $V_{T0,p} = -0.7\text{V}$, $(W/L)_n = 1/1$, $(W/L)_p = 4/1$, $\mu_n C_{ox} = 40\ \mu\text{A/V}^2$, $\mu_p C_{ox} = 20\ \mu\text{A/V}^2$. Neglect γ and λ. $V_{DD} = 5\text{V}$. Assume that all inputs switch simultaneously.

3 Two Input CMOS NAND Gate

Problem 3.1 Assume that a two input CMOS NAND gate drives a total load capacitance of 0.1pF. All devices have $W = 10\mu\text{m}$, but the effective length for NMOS devices $L_{eff} = 1\mu\text{m}$ while for the PMOS devices $L_{eff} = 2\mu\text{m}$. Given that $k_n' = 20\mu\text{A/V}^2$, $k_p' = 10\mu\text{A/V}^2$, $V_{T,n} = 1.0\text{V}$, $V_{T,p} = -1.0\text{V}$, and $V_{DD} = 5\text{V}$, approximate t_{pLH} and t_{pHL}.

4 Mixed Combinational and Sequential Logic

Problem 4.1 A useful trick for highly optimized logic design is to fold a combinational CMOS circuit into a sequential circuit such as a latch. Modify the master stage latch circuit shown in Figure 7-26 in Rabaey to incorporate the logic function $F = A \cdot (B + C)$. Size the transistors such that the pullup and pulldown networks for the equivalent inverter have equal rise and fall times. Assume the mobility ratio $\mu_n/\mu_p = 2.5$, $V_{T0,n} = |V_{t0,p}|$, and a minimum sized device has $W/L = 5/1$. Write your answer in terms of the W/L ratios for the PMOS and NMOS devices. Hint: See Figure 7-31.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.