EEC 118 Spring 2010 Homework #3

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Reading: Rabaey Chapter 5 [1].
Reference: Kang and Leblebici Chapter 5 [2].

1 Pseudo NMOS Inverter

Problem 1.1 Sizing. Figure 1 shows a circuit known as a pseudo-NMOS inverter since the depletion-mode NMOS device has been replaced with a grounded-gate PMOS. Using the following device parameters for the transistors:

- NMOS: $V_{T0} = 0.6\text{V}$, $L = 0.8\mu\text{m}$, $\lambda = 0.0\text{V}^{-1}$, $\mu C_{ox} = 60\mu\text{A/V}^2$
- PMOS: $V_{T0} = -0.7\text{V}$, $L = 0.8\mu\text{m}$, $\lambda = 0.0\text{V}^{-1}$, $\mu C_{ox} = 25\mu\text{A/V}^2$

and assuming the power supply voltage V_{DD} is 3.3 V, find the (W_n/W_p) ratio so that the switching (inversion) threshold voltage of the circuit is $V_M = 1.4\text{V}$. How does the (W_n/W_p) ratio differ from the ratio you found for the CMOS inverter in Homework #2, Problem 3.1?

Problem 1.2 Noise Margins. Calculate the noise margins for the circuit you designed in Problem 1.1.

Problem 1.3 V_{in} Overdrive. Calculate the required input voltage V_{in} to force the output voltage to 0.6V for the circuit you designed in Problem 1.1.

2 Circuit X

Problem 2.1 Function. Sketch the Voltage Transfer Curve for the circuit drawn in Figure 2. Label the values of V_{OH} and V_{OL}. What is the logical function performed by the circuit?

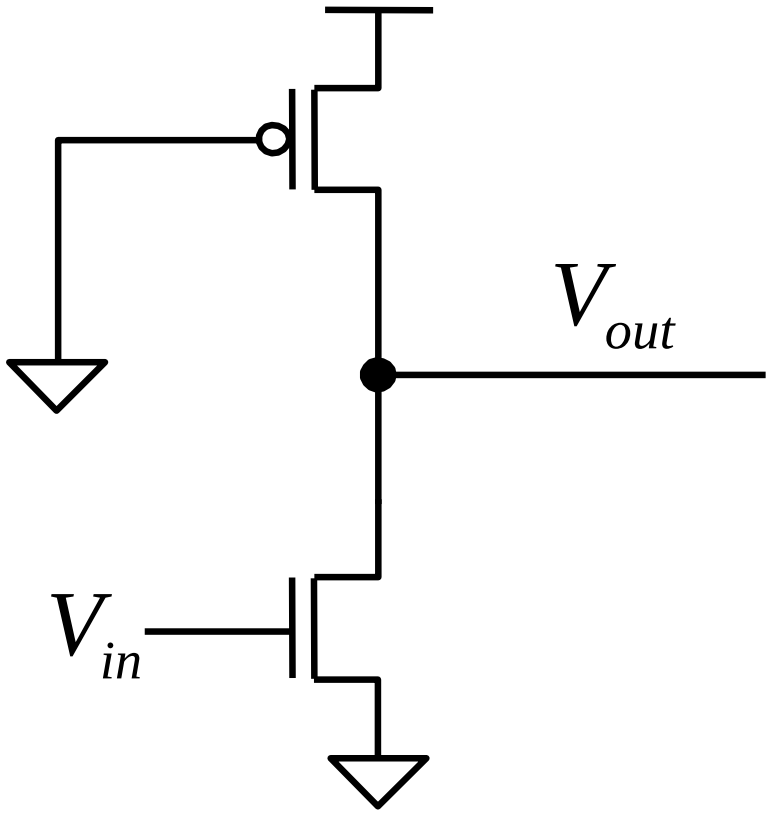

Figure 1: Pseudo NMOS inverter.

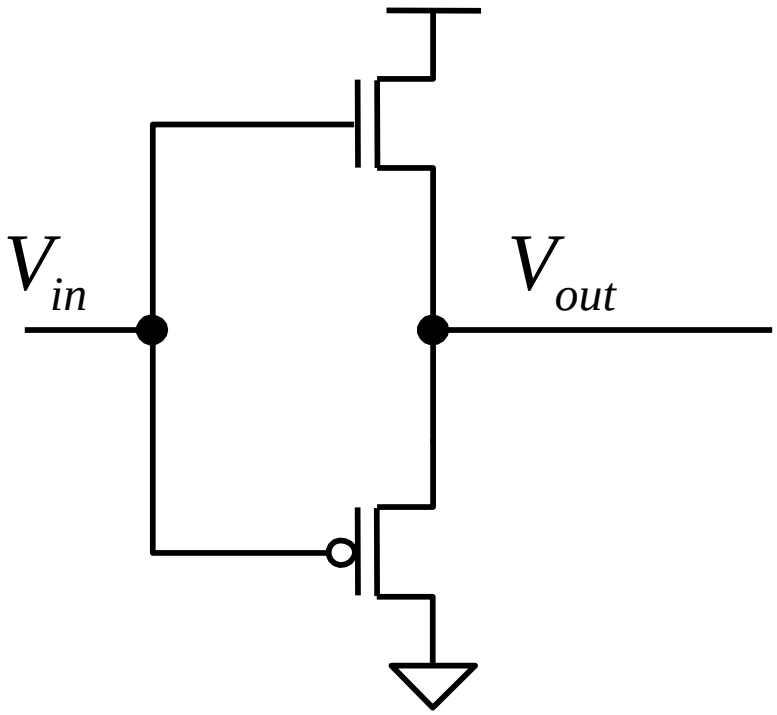

Figure 2: Circuit X.

Problem 2.2 Switching Threshold. Consider the switching threshold V_M for the circuit drawn in Figure 2. Does the definition stated in class make sense for this circuit? Why or why not?

Problem 2.3 Switching Threshold. Determine the switching threshold V_M for the circuit drawn in Figure 2 making any reasonable assumptions about how to properly define it.

Problem 2.4 Discussion. Is the circuit drawn in Figure 2 suitable for use as a logic gate? Why or why not? *Hint: Consider the voltage swing of the circuit.*

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.