EEC 118 Spring 2010 Design Project Part 2:
Circuit Design of Multiplier Cells
Week of May 10-12, 2010

Create SPICE models for modules used in your final project design. These modules include:

A) Flip-flops and Registers
B) Half Adder (if you use one)
C) Full Adder (both polarities if you use the inversion property)
D) Miscellaneous Logic Gates

For each of these modules, you must supply the following:

i) SPICE Netlist including control cards so that it can be run as is. This netlist should provide the correct input waveforms to demonstrate correct circuit operation of the modules you designed. You must use the subcircuit templates (designpt2.sp) from the web page so that a consistent cell interface is presented to the test bench.
ii) Schematic
iii) Table with propagation delays for each major unit, including t_{PHL}, t_{PLH}, t_r, t_f for the combinational circuits and the clock-to-Q, setup, and hold times for the register. Assume that each cell input is driven by a minimum-sized inverter (no ideal voltage sources should touch a cell input) and each cell output drives a fanout of 4 minimum-sized inverters. This is similar to the testbench you used in Lab 3, Part 1. You may reuse any of your SPICE code from that lab for this project.

Answer the following questions in your lab report for the Design Project, Part 2:

1. Based on the table of delays you computed above, what is the **highest** clock frequency you expect your multiplier design to run at? Justify your answer quantitatively.
2. What is the **lowest** clock frequency you expect your design to be functionally correct at (i.e., do you expect your circuit to work all the way down to DC)? Justify your answer.

This work will be incorporated into your final project report.